Physics And Technology Of Submicron Polysilicon Thin Film Transistors (tfts).

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Physics and technology of submicron polysilicon thin-film-transistors (TFTs)

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PHYSICS AND TECHNOLOGY OF SUBMICRON POLYSILICON THIN-FILM-TRANSISTORS (TFTs)

by

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I dedicate this Dissertation to my parents Salawu Olasupo Ibijuwon and Muniratu Olasupo

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ABSTRACT

The polysilicon thin film transistor (TFT) has been actively studied as the switching element of active matrix liquid crystal displays and as the load resistor in static random access memories. Due to low effective carrier mobility in polysilicon, the circuit speed is limited. Since the circuit delay time is directly proportional to the square of the channel length, short channel TFTs will be advantageous for high speed applications. Unfortunately, reducing the channel length results in high leakage current that complicates the application of submicron TFT devices.

This dissertation investigated the fabrication characteristics of sub micron polysilicon thin-film-transistors (TFTs). Several studies of polysilicon TFTs have reported increasingly anomalous leakage current characteristics as channel dimensions are reduced. As such, more emphasis was devoted to understanding the causes of off state leakage current in submicron thin-film-transistors, and to understand how drain offset lengths can be used to reduce it..

In order to achieve these goals, P-channel TFTs devices with several drain offset lengths were examined, polysilicon TFTs with channel length ranging from 1.0μm to 0.35μm and channel width from 0.6μm to 0.35μm were fabricated on a 50nm crystallized amorphous silicon. To study the impact of drain offset on the

leakage current and the drive current, TFTs with drain offset lengths ranging from 0.0μm to 1.0μm were fabricated.

The leakage current and the on current were found to be in the pico-amp and micro-amp range respectively for devices having channel length in the range of 1.0μm to 0.35μm. Even very small devices having W = L = 0.35μm exhibited characteristics similar to wider devices. The devices exhibited a broad switching characteristics averaging 700 mV/decade, a low drive currents (average 2.0μA), a high leakage current ranging from 1.0pA to 100 pA and low effective mobility ranging from 0.086 to 0.54 $cm^2/V.s$. The on/off current ratio was in the order of 10^5 for the symmetric drain offset structure and 10^3 for the asymmetric drain offset structure before hydrogenation.

It was found that the drain offsets behave like a series resistance. As a result, the drain current (both drive and leakage) were reduced because of the potential drop across the drain offset region. The reduction is proportional to the length of the drain offset. For the device studied, the optimum drain offset length is between 0.3μm to 0.5μm. Within this range, the drive current and the leakage current were optima. Although the introduction of drain offset reduced the leakage current, it also reduced the drive current. Fortunately however, the conduction properties of the offset region can be modified by changing its doping concentration. It was found that doping dosage ranging from 1E12 cm^{-2} to 1E14 cm^{-2} provided high drive current while leakage currents remain low.

The temperature dependence of the drain current revealed that drain current activation energy in the on state decreases as the gate bias becomes more negative. This is an indication that the Fermi level gradually move towards the valence band. In the off state, the leakage current activation energy was 0.5eV at a low drain bias (-0.1 volts). This suggest that the carrier emission from traps in the drain depletion region is dominated by thermionic emission at low field. Further increase of drain bias (-6.1 volts) showed that leakage current is dominated by thermionic field emission and tunneling of carriers from the traps. At this bias, the barrier that carrier (holes) must overcome dropped to 0.1 eV from 0.5 eV. Thus, the leakage current is a result of generation recombination processes that is dominated by thermionic emission at low drain bias, thermionic field emission and tunneling at high drain biases.

Chapter 1 OVERVIEW

1.1 Introduction to Polysilicon Thin-Film-Transistor

This dissertation investigated the fabrication characteristics of sub-micron polysilicon thin-film-transistors (TFTs). Several studies of polysilicon TFTs have reported increasingly anomalous leakage current characteristics[1],[2] as channel dimensions are reduced. As such, more emphasis was devoted to understanding the causes of off state leakage current in submicron thin-film-transistors, and to understand how drain offset lengths can be used to reduce it. To achieve these goals, both P and N channel TFTs with several drain offset lengths were examined .

Before discussing the application of polysilicon TFTs, it is noted that polysilicon or polycrystalline silicon (poly-Si) material usage in the fabrication of advanced integrated circuits has increased over the last several years. The fact that poly-Si could be easily grown or deposited more economically than single-crystal silicon has been the driving force. Much more significant is that the deposited polysilicon can be doped with impurities, thermally oxidized like single-crystal silicon and can be patterned using photolithography. Other pertinent advantages include the convenience of using polysilicon as an impurity diffusion source, as gate material for self-aligned bulk-silicon Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs), and innovative devices like TFTs, whose

fabrication would have been impossible without the ability to deposit polysilicon. Despite the advantages polysilicon has to offer, its main drawback is that the grain boundaries (figure 1.1 and 1.2) in the film often reduce device performance.

Considerable effort [3],[4],[5],[6] has been devoted to investigating the effects that these grain boundaries have on carrier transport. However, these effects is not well understood, particularly when the material is used to fabricate devices with dimensions smaller or equivalent to the grain sizes. To reduce the effect of the grain boundary, several grain enlargement[7],[8],[9] and grain boundaries passivation techniques[10],[11],[12],[13] have been investigated. A few of these techniques will be reviewed in chapter 2.

Polysilicon TFTs are used to build peripheral drive circuitry that interfaces with active matrix liquid crystal display (AMLCD) in display applications, and as a load resistor in static random access memory (SRAM) applications. The requirements are different for each application. This is reflected in the structure of the TFT, which is the subject of next section.

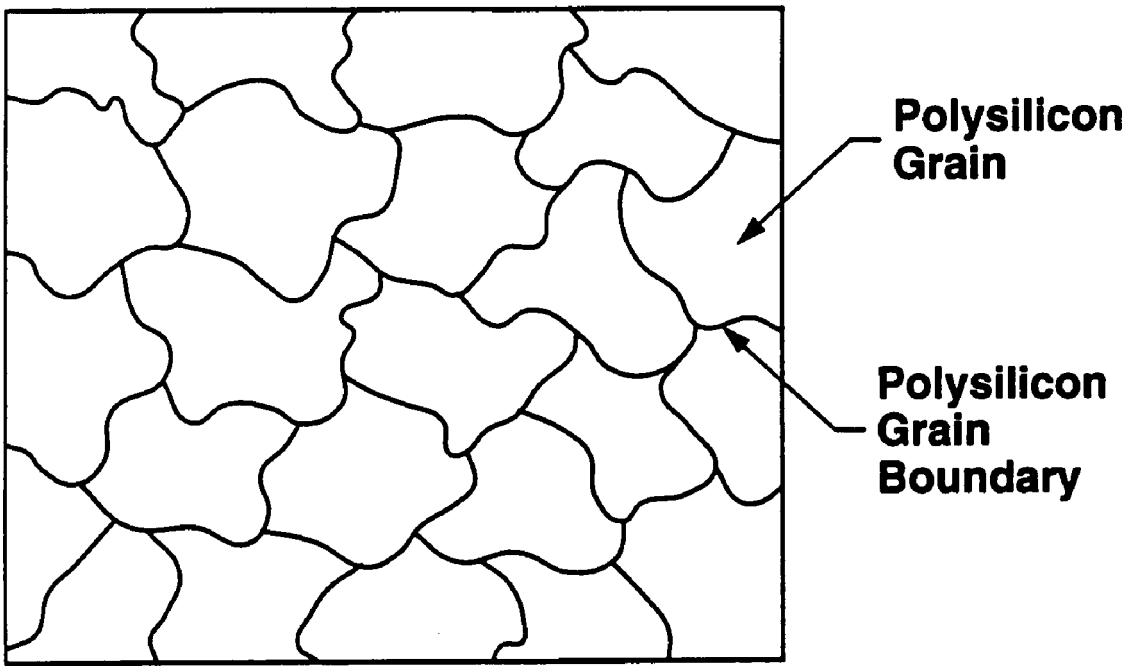


Figure 1-1. Figurative Illustration showing the grain boundaries

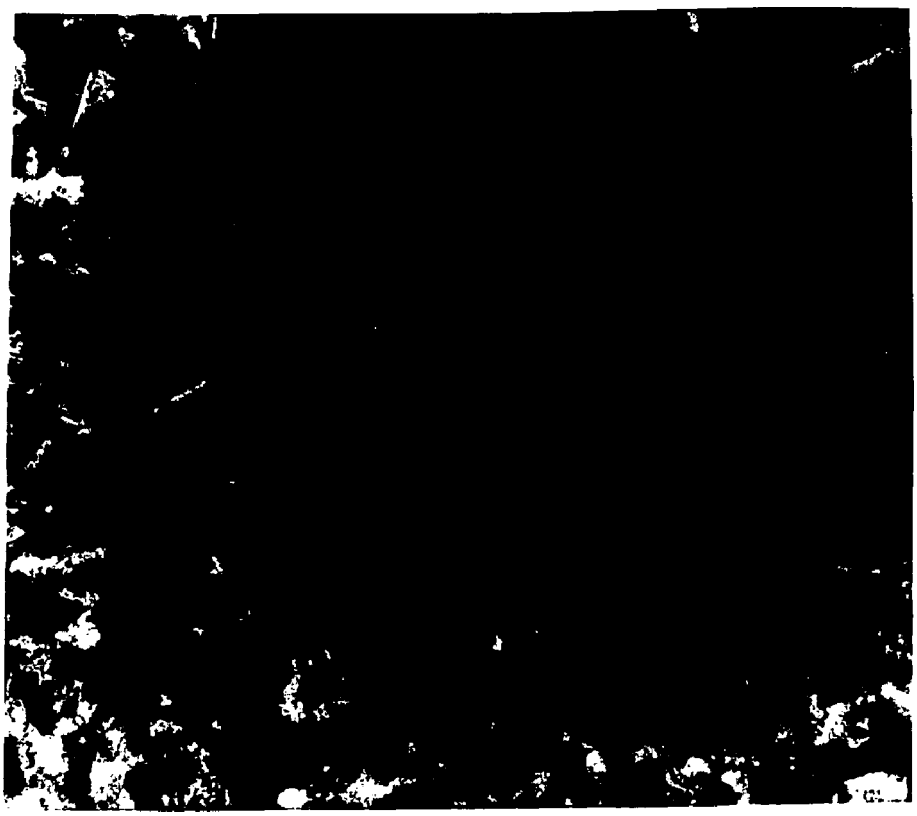
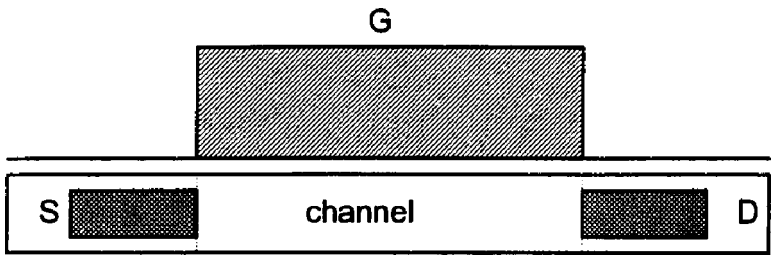


Figure 1-2. Transmission electron micrograph of polysilicon film used in this study.

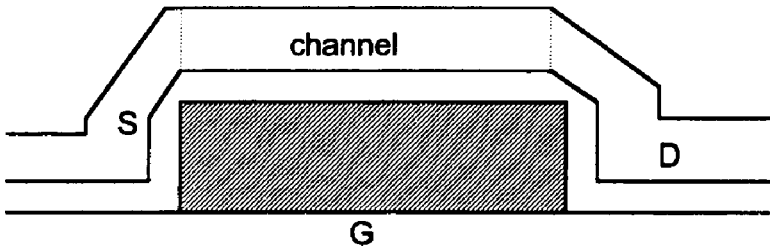
1.2 Current state of research

Because of the ease of integration of TFTs into SRAM[14],[15] technology as well as the tremendous applicability to active matrix liquid crystal displays or page width sensors[16],[17], much interest has been developed in polysilicon thin-film-transistor (TFT) technology. Thin film transistors can be made with a wide variety of structures and materials. Currently, there are two basic types of TFT structure, the upright and the inverted structure (figure1.3a and 1.3b, respectively)[18].



(a)

Upright TFT with Gate Electrode above the active (channel) region



(b)

Inverted TFT with Gate Electrode below the active (channel) region

Figure 1-3. The upright and the inverted thin film transistor structure.

The major differences are in the process sequence. For example, the upright TFT structure has the gate electrode defined on top of the active layer while the inverted structure has the gate electrode defined below the semiconductor active layer. In active matrix display applications, the upright structure is used extensively because it lends itself to self-aligned processes. In SRAM applications, however, the upright structure introduces back channel as well as integration complications. Current submicron integrated circuit designs prefer to use inverted thin film transistors[14],[19],[20],[21]. The inverted structure increases the integration density, improves the topography, and reduces the number of photolithography levels thereby simplifying fabrication in the submicron regime. It has also become indispensable in three-dimensional integration because of interconnection restraints.

Due to the higher carrier mobility and better device stability over amorphous silicon based TFTs, recent research efforts have focused on improving some of the undesirable device characteristics of polysilicon TFTs, such as better threshold voltage control and lower off state leakage current. To achieve these goals, much effort has been placed on low temperature ($\leq$ 650 °C) substrate processing. This is necessary to obtain larger grain sizes and a lower number of grain boundaries, which result in a lower number of trap sites and lower leakage current. Consequently, several polysilicon grain enhancement technologies have become an integral part of TFT fabrication procedures[8],[22],[23],[24],[25]. Additionally, the passivation of grain boundary defects by atomic hydrogen has proven to be an

effective method in reducing the leakage current and enhancing the characteristics of TFTs[19],[26],[27],[28]. Despite grain enlargement techniques and passivation of the grain boundaries with atomic hydrogen to reduce the off state leakage current, a better understanding of the mechanisms that cause off state leakage current is needed to improve the state-of-the-art TFT technology.

1.3 Application of polysilicon TFTs to AMLCDs technology

The initial efforts in polysilicon TFTs was geared towards three dimensional (3D) silicon integrated circuit (IC) applications. The research efforts were designed to investigate the use of polysilicon as a passive substrate for isolating bipolar devices[29]. Beside the substantial increase in packing density, building devices on an isolated substrate eliminates latch-up in CMOS, increases circuit speed as a result of the reduction in coupling capacitance which can occur throughout the substrate, and improves radiation tolerance by eliminating charge generation in the substrate. These attributes drove the interest in silicon-on-insulator (SOI) and silicon-on-sapphire (SOS) technologies in late 1970s[30]. Because of the higher current drive capability[31] compared to the amorphous devices, and the fact that polysilicon TFT devices offer the flexibility of being used

to build peripheral drive circuitry on the same substrates to interface with AMLCD, attention shifted to polysilicon TFTs for display applications.

Figure 1.4 illustrates the application of polysilicon TFTs to an active matrix liquid crystal display. In a line-at-a-time addressing, for example, all TFT gates of a row are opened for a certain time duration to allow the voltage from individual data lines to charge or discharge the pixel. The gates are then closed and the next row is addressed with properly re-configured data lines. Thus, if the TFT gates are open for a time period of (T/K), where K is the number of resolution lines, then the TFT leakage current must be low enough to maintain the correct charge on the pixel for a period of time equal to (T(K-1)/K).

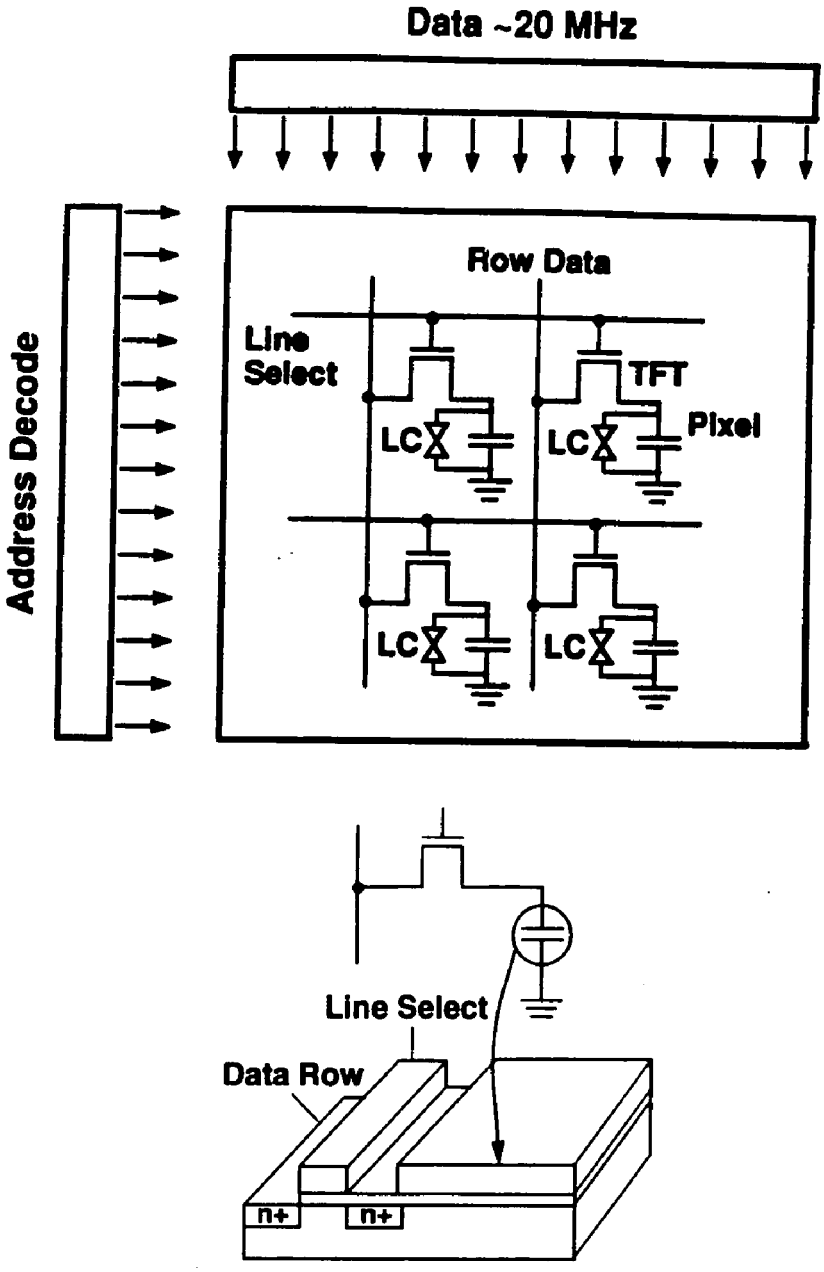


Figure 1-4. Active matrix addressing illustrating the application of TFTs.

1.4 Application of TFTs in SRAM technology

Static Random Access Memory (SRAM) technology has always been the major driving force of the Metal Oxide Semiconductor (MOS) technology because of its demand for high density, high speed and lower power. Due to the replication of an SRAM cell in an array (figure 1.5), a high payoff in area shrinkage is obtained by using tight design rules and compact cell designs. Thus, the future of memory development is strongly coupled to the memory cell size.

As the MOS technology is driven into the sub-half micron regime, due to the increasing demand for smaller cell size and higher packing density, it is necessary to scale the cell supply voltage to satisfy leakage current and power dissipation requirements. In the megabit SRAM, for example, reducing the cell size and increasing the supply voltage forces the level of a cell node which stores a "high" to be reduced. As a result, the cell's operating stability becomes a serious problem. This technological drive towards the submicron regime and high packaging density has forced 6T cells designs to be reduced to 4T polysilicon load resistor cells. Recently, PMOS Thin-Film-Transistors (TFTs) have been used to replace the polysilicon load resistors in the 4T cell designs (figure 1.5 & 1.6).

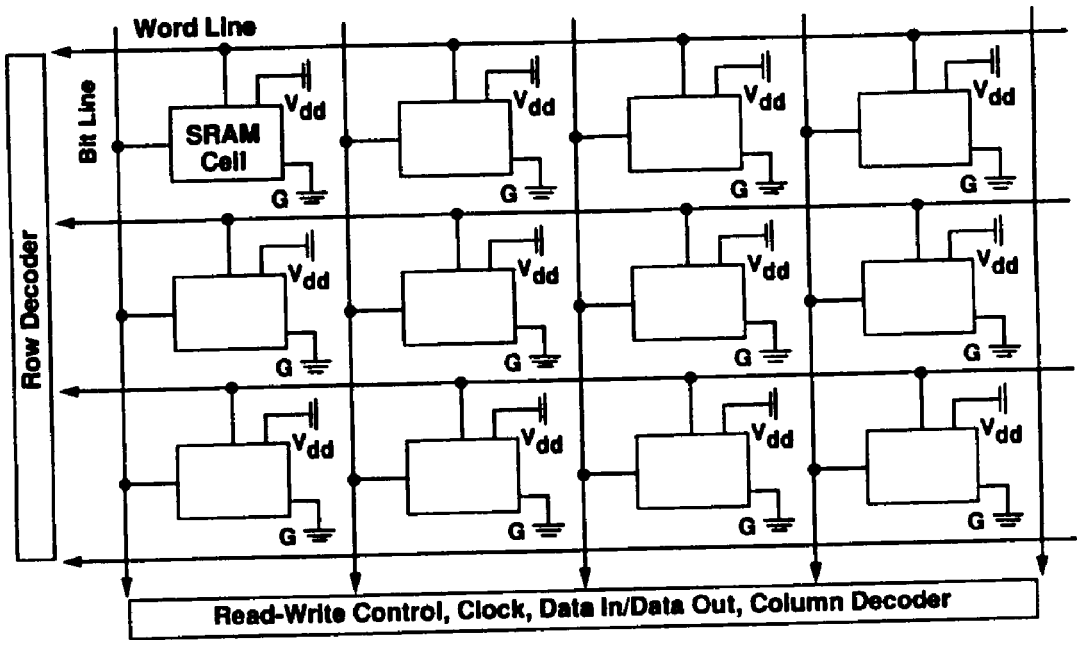


Figure 1-5. Illustration of SRAM cells.

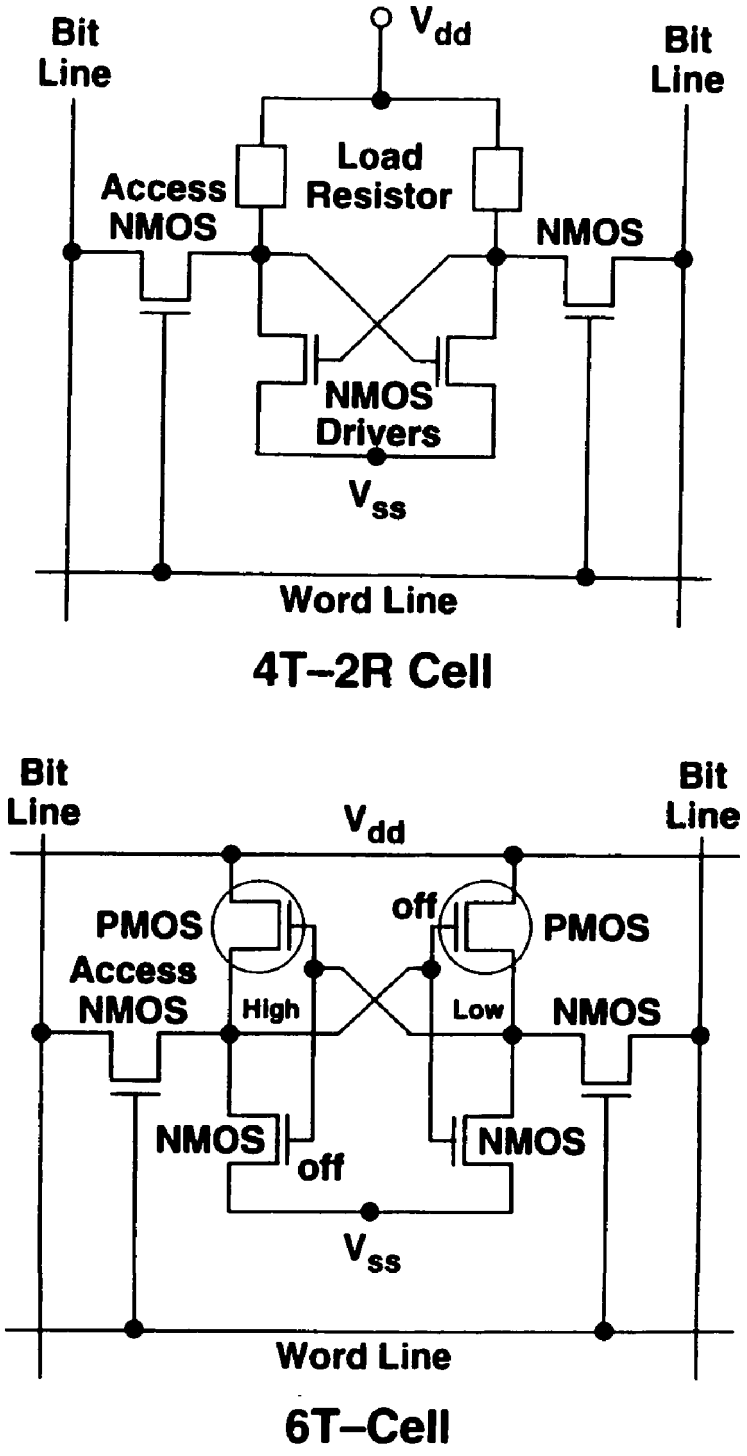


Figure 1-6. Illustration of a cell design for SRAM technology.

The 6T cell offers the best operating stability and PMOS switching characteristics. However, drawbacks such as large access and cycle time and large area penalty make it less attractive for today's aggressive SRAM markets. The 4T polysilicon load resistor cell allows for cell area minimization and simultaneous benefits in speed. Unfortunately, the Poly (Hi-R)[32],[33] cell can only satisfy minimum standby current and power dissipation requirements due in part to its poor transfer characteristics (figure 1.7(b)). Furthermore, soft error rates (figure 1.7(a)) become severe due to a decrease in storage node capacitance and cycle time. All of these problems present a formidable barrier to the development of high density (≥ 4Mbit) SRAMs using the Hi-R cell. To overcome these difficulties, the PMOS TFT load cell was developed[10]. The TFT load cells are attractive for 4Mbit SRAMs and beyond because of their cell stability, large on current and smaller "IR" drop[11], which reduces the influence of abnormal leakage current known to cause retention failure in the Hi-R 4T cells.

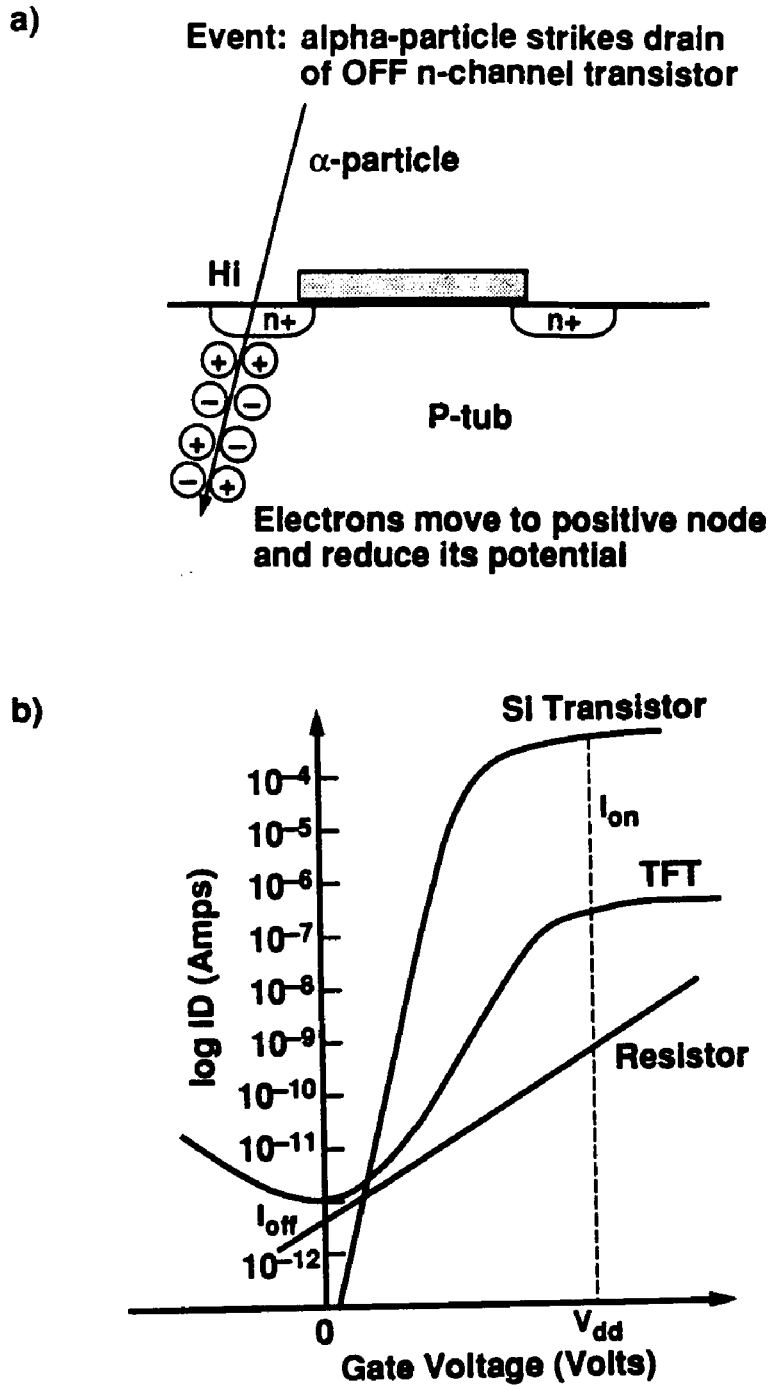


Figure 1-7. (a) Illustration of a soft error in an N-channel transistor, and (b) the transfer characteristics of silicon PMOS, PMOS TFT and 4T-2Resistor cells.

1.5 Areas of Concentration

The limiting factor of a polysilicon TFT for use in active matrix displays and in memory technologies is its leakage current. The leakage current limits the display resolution that can be fabricated with polysilicon TFTs and it limits the application of polysilicon TFTs in fast static random access memories. This dissertation will focus on engineering the drain offset on submicron polysilicon TFTs to obtain the minimum leakage (off) current and maximum drive (on) current possible. In addition to determining the optimum drain offset length, the optimum dopant concentration needed in the drain offset region for optimum device performance will be determined.

The next chapter will focus on the physical and electrical properties of polysilicon. Chapter 3 will focus on fabrication of sub-micron polysilicon TFTs and in chapter 4, the experimental results will be presented. Analytical models for the drive (on) current, leakage (off) current and the effect of drain offset structure on the performance of polysilicon TFT will be presented in chapter 5. This model will show that the dominant mechanism for the leakage current is thermionic carrier emission at low field, and thermionic field emission and tunneling of carriers from the traps located in the drain depletion region at high drain field. Additionally, it will be shown that the drain offset structure acts as a series resistance that decreases the drive current and reduces the tunneling probability of carriers from trap sites in the drain depletion region by reducing the space charge electric field.

Chapter 2 PROPERTIES OF POLYSILICON FILMS

2.1 Introduction

In order to have a better understanding of the influences of grain boundaries and their associated defects on the electrical properties of polysilicon and polysilicon devices, this chapter will present both the physical and electrical properties of polycrystalline silicon materials. The chapter will begin with an introduction to the grain boundary structure in polysilicon films. This will be followed by discussion of the effect of the grain boundaries on the conduction and carrier transport properties of polysilicon. Finally, a few of the carrier transport models will be discussed.

The inverted P-channel polysilicon TFTs studied in this dissertation were fabricated on 5 inches diameter silicon wafers using re-crystallized amorphous silicon (α-Si). The fabrication process starts with a sequential H_2SO_4/H_2O_2 and BHF cleans. This is followed by the deposition of 400 nm of Low Pressure Chemical Vapor Deposition (LPCVD) SiO_2 by TEOS pyrolysis at 720°C and the deposition of 50 nm of α-Si in an LPCVD reactor by pyrolysis of SiH_4 at 550°C and 0.5 Torr. The chemical reaction is

$SiH_4 = Si + 2H_2$ ----------(2.1)[34]

LPCVD is a popular deposition method because it provides good uniformity within the wafer and from wafer to wafer and at the same time offers excellent step coverage. Because the pyrolytic reaction, equation (2.1), was carried out at a temperature below 575°C, the deposited silicon film show no detectable structure; thus it is amorphous. In order to transform the amorphous film into polysilicon, it was crystallized using a low temperature (≤ 600°C) crystallization furnace anneal for 15 hours. The crystallization process is summarized in figure 2.1. This process results in the formation of several single crystalline silicon grains separated by grain boundaries.

As indicated in figure 2.1, the crystallization process involves two stages: nucleation and grain growth. Once the growing grains impinges on each other, grain growth stops. Please refer to Tolis[34] for detailed discussion of crystallization process.

The two major tools used to analyze polysilicon films are transmission electron microscope (TEM) and x-ray diffraction. These tools are used to estimate the grain size, structure and texture of the polysilicon film. In this work, TEM was used to estimate the average polysilicon grain size, and it was found to be 0.5μm. X-ray diffraction was not used in this work.

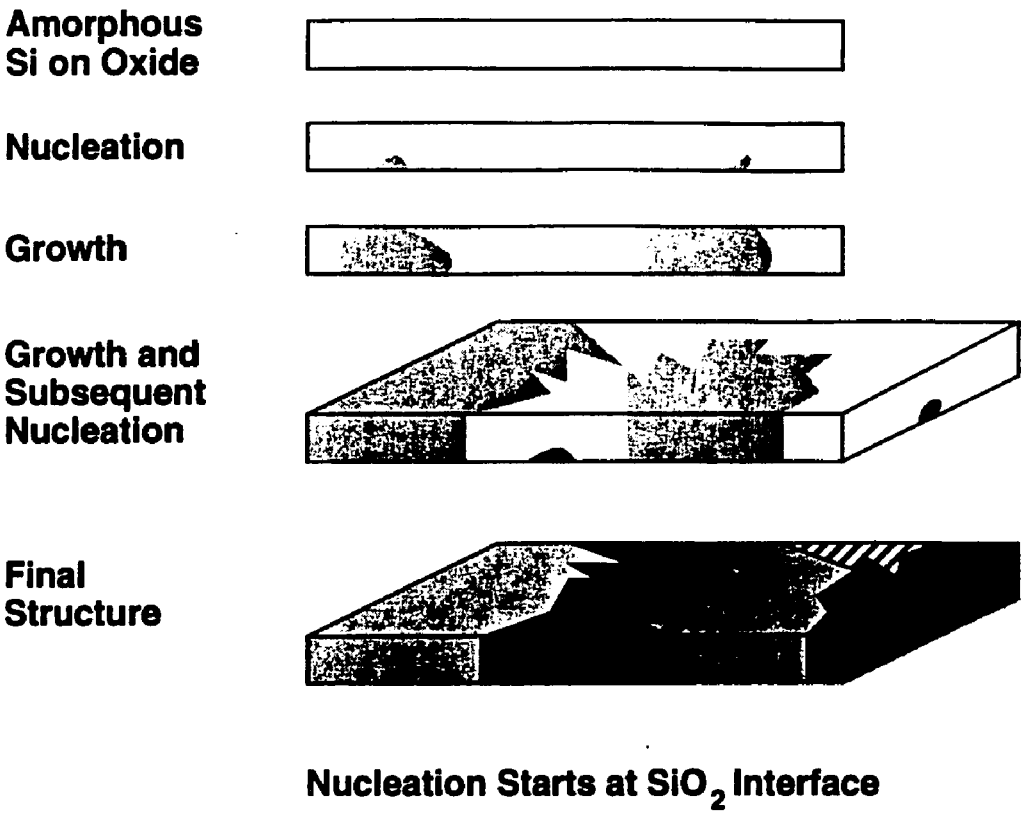


Figure 2-1. Schematic illustration of crystallization process to form polysilicon.

2.2 Grain boundary effects

The grain boundaries of polysilicon contain two kinds of bond disorders as indicated in figure 2.2. These disorders, strained and dangling bonds, are partly responsible for increasing the bonding energy. Additionally, they introduce energy states within the band gap in silicon. The strained bonds are believed to generate the tail states while dangling bonds generates the defect states at midgap (figure 2.3)[35].

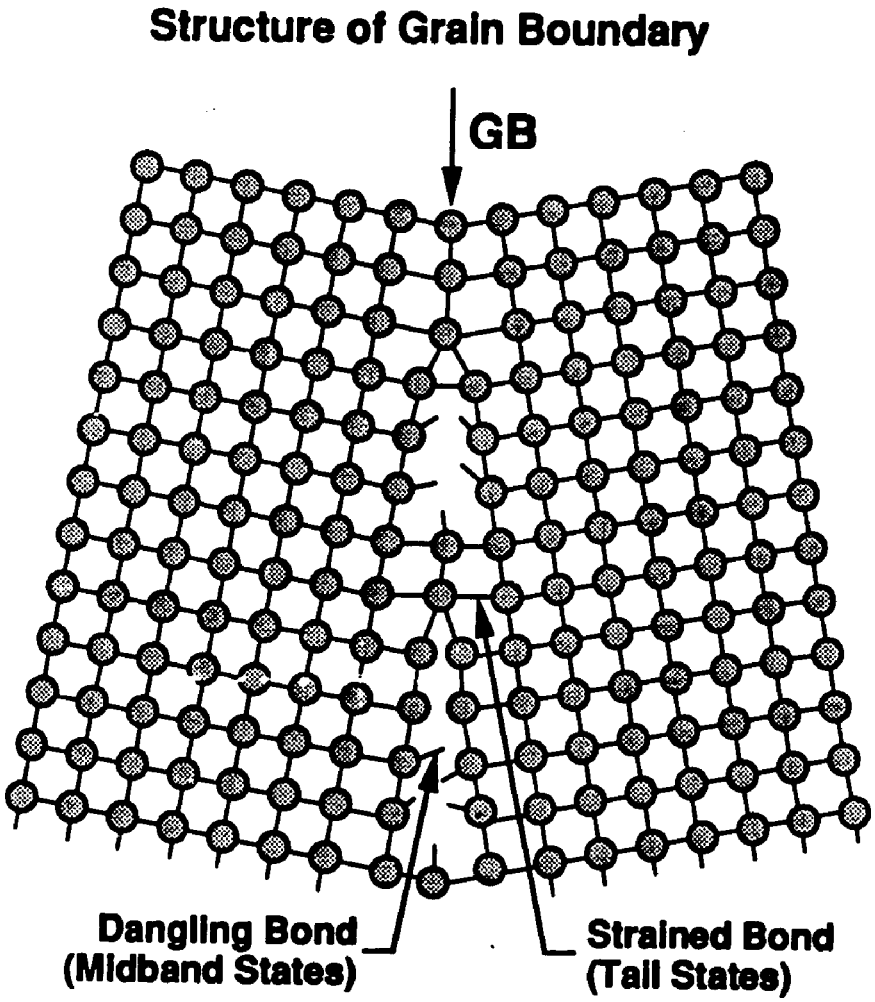


Figure 2-2. Defects associated with grain boundaries in polysilicon.

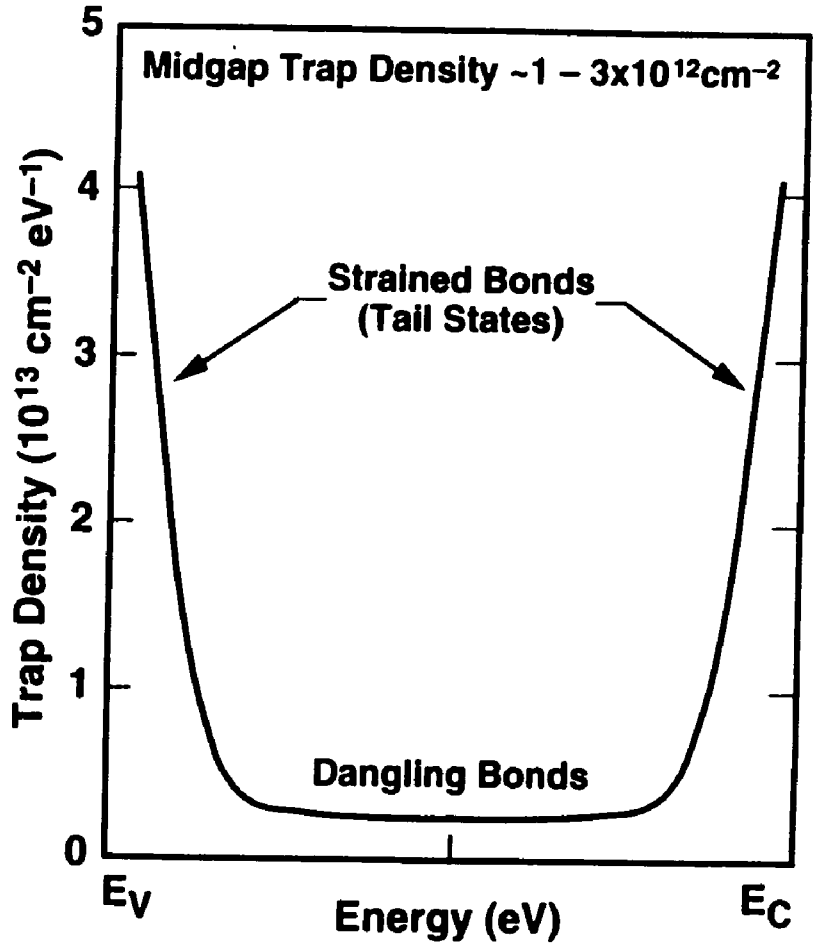


Figure 2-3. Distribution of trap energy across the energy band gap[35].

The midgap states consist of singly and doubly occupied states located near the center of the bandgap[36],[37] . These, states can act as generation and recombination centers which degrade the electrical performance of devices fabricated in polysilicon films. Therefore, the lower the number of grain boundaries, the lower is the amount of carrier/trap interaction that can degrade the devices' electrical performance.

2.3 Carrier Transport and Conduction in Polysilicon Films

Polysilicon can be viewed as an agglomeration of single crystal silicon grains separated by grain boundaries. The grain boundaries are the loci of orientational misfits and are associated with both deep and shallow (tail) electronic states. Since carriers usually travel from one grain to another, these electronic states create potential barriers at the grain boundary that impede carrier transport. This section will focus on carrier transport and conduction in polysilicon films.

According to Seto[5] , polysilicon can be modeled as a linear chain of identical crystallite grains of size 'L' as shown in figure 2.4. The boundaries between the grains function as carrier trapping, scattering, generation and recombination centers. The grain boundary is further assumed to be of negligible thickness compared to 'L' and contains a concentration, Nt, per unit area of traps

located at energy, Et, with respect to the intrinsic Fermi level. The charge exchange mechanism within the grain boundary is shown in figure 2.5.

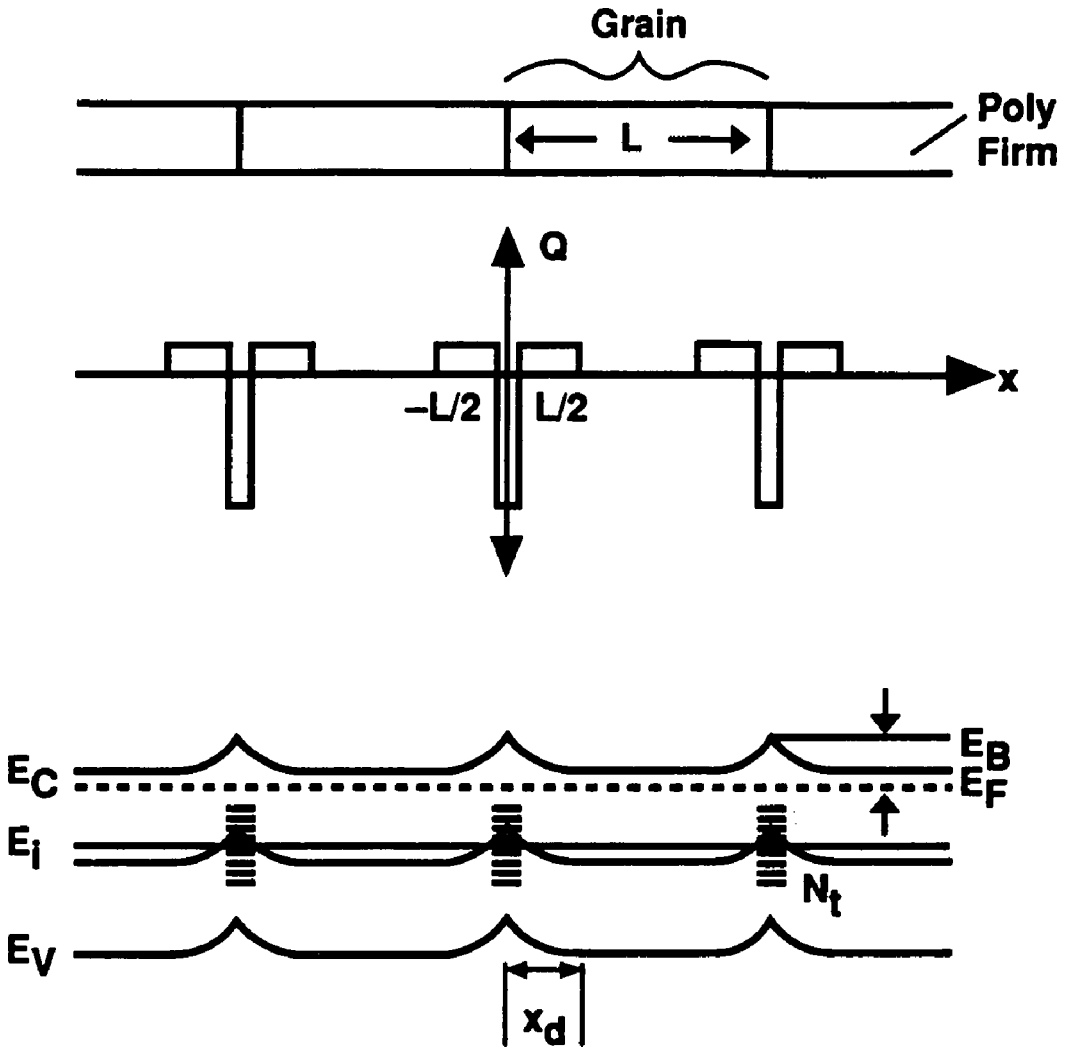
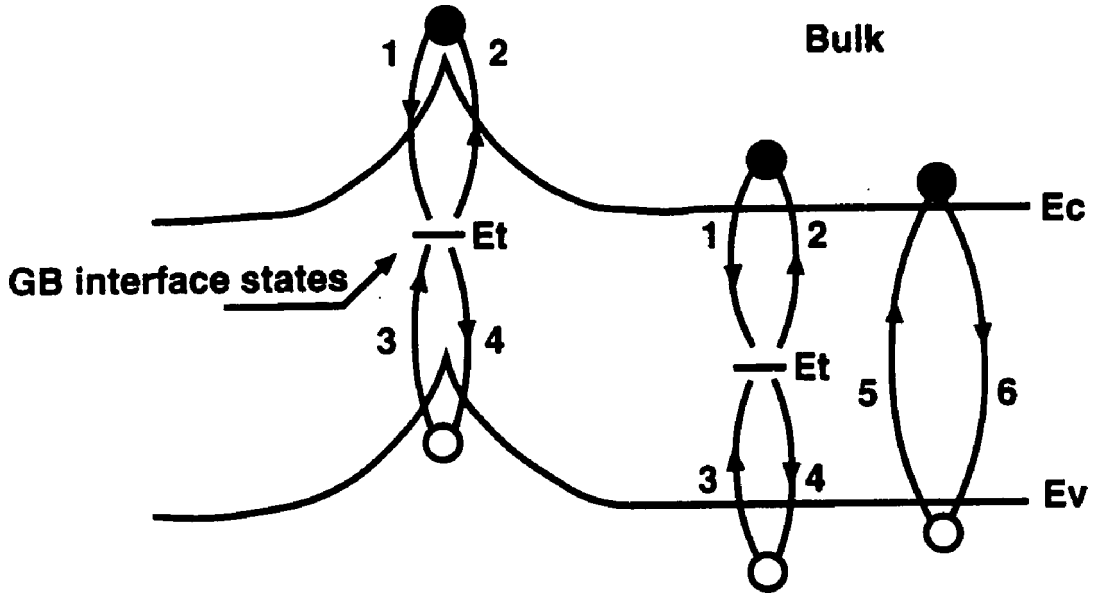


Figure 2-4. Grain structure and boundary assumed in the grain boundary trapping model[5].



Process 1: electron capture
2: electron emission
3: hole capture
4: hole emission
5,6: electron-hole recombination

Traps close to the middle of the gap are most effective.

Figure 2-5. Charge exchange mechanism within the grain boundary.

If the grain boundary traps are assumed to be acceptor type traps (neutral when empty of electrons and negatively charged when filled with electrons), then electron emission is through thermionic emission, tunneling through the grain boundary barrier, or thermionic field emission as shown in figure 2.6.

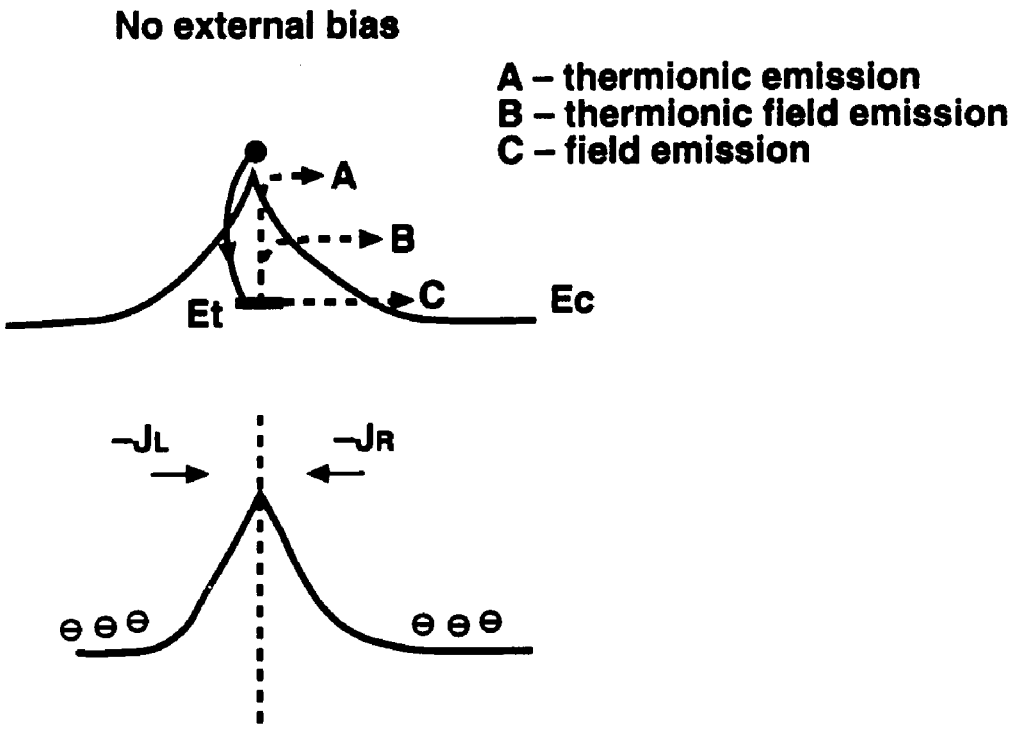


Figure 2-6. Carrier transport mechanism in polysilicon film.

If we consider thermionic emission the current density for carrier flow between grains is given by:

$$J = -qnv_c e^{-[\frac{q}{kT}(V_B - V)]} \text{----------2.2)}$$ [4]

where n = free carrier density,

V_c = collection velocity = $\{\sqrt{(KT/2\pi m^*)}\}$,

qV_B = energy barrier height,

V = applied bias across depletion region,

k = Boltzmann's constant,

T = Temperature in absolute Kelvin, and

q = electronics charge

With no external bias applied (V=0), the forward current density (J_F) and the reverse current density (J_R) are equivalent because the barrier (V_B) is equal in both direction.

$$J = J_F - J_R = 0 \text{----------(2.2}a\text{)}$$

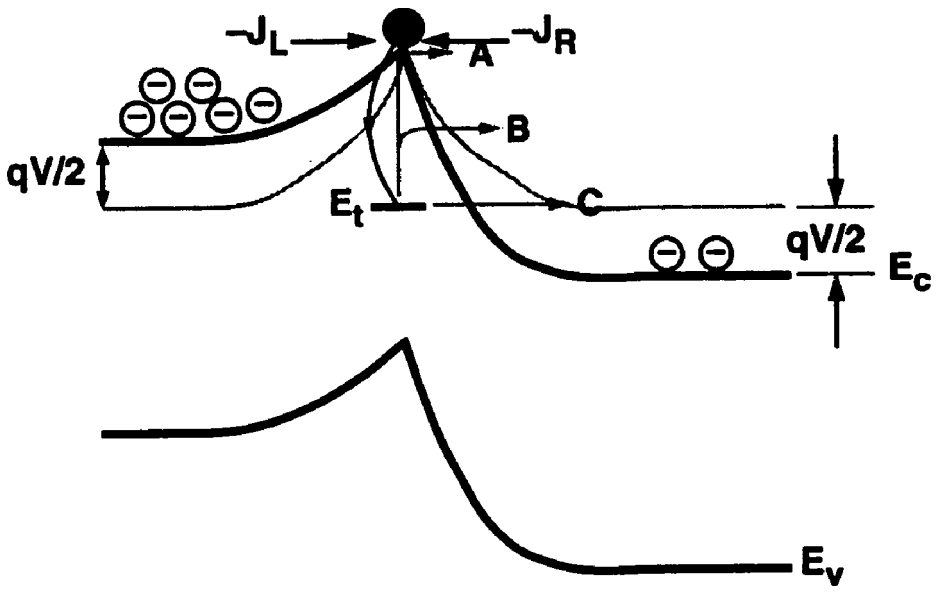
For a single grain boundary with an externally applied bias, the barrier to electron transport in one direction decreases, while it increases in the opposite direction, as

shown in figure 2.7. Approximately half the applied bias appears across each depletion region. By considering thermionic emission in both directions, the net carrier current density is given by,

$$J = J_F - J_R = -qnv_c e^{-\frac{qV_B}{kT}} \{e^{(\frac{qV_g}{2kT})} - e^{-\frac{qV_g}{2kT}}\} \text{-----} (2.3)$$

Equation (2.3) can be rewritten as

$$J = -2qnv_c e^{-\frac{qV_B}{kT}} \sinh(\frac{qV_g}{2kT}) \text{----------} (2.4)$$



Mechanisms B and C involve tunneling through the GB potential boundary. These processes are enhanced by externally applied field.

Figure 2-7. Grain boundary band diagram under applied bias.

For 'N' grains, the net current density becomes

$$J = -2qnv_c e^{-\frac{qV_B}{kT}} \sinh(\frac{V}{\xi}) \text{----------(2.5)}$$

where

$$\xi = \frac{2kTN}{q} = \frac{2kTZ}{qL_g}$$

N = number of grains,

Z = channel length, and

L_g = grain size.

$V_g = \frac{V}{N}$ is the voltage across a grain.

For a small applied bias, sinh(V/ζ) becomes (V/ζ) and the thermionic emission current density becomes

$$J = -qnv_c e^{-\frac{qV_B}{kT}} \left(\frac{qVL_g}{2kTZ}\right) \text{----------(2.6)}$$

The average conductivity of polysilicon can now be defined as

$$\sigma = \frac{J}{\varepsilon} = \frac{q^2 n v_c L_g}{kT} e^{-\frac{qV_B}{kT}} \text{----------(2.7)}$$

Thus, conduction in polysilicon is an activated process with an activation energy (E) proportional to the barrier potential (qV_B). The resistivity of the film is inversely proportional to the conductivity described by equation (2.7). Additionally, the resistivity of polysilicon varies with doping concentrations (figure 2.8)[5],[38] . Compared to the resistivity of single crystal silicon, polysilicon is characterized by a higher resistivity at a lower dopant concentration. Although the resistivity decreases as the dopant concentration is increased, the lowest value is higher than that of single crystal silicon.

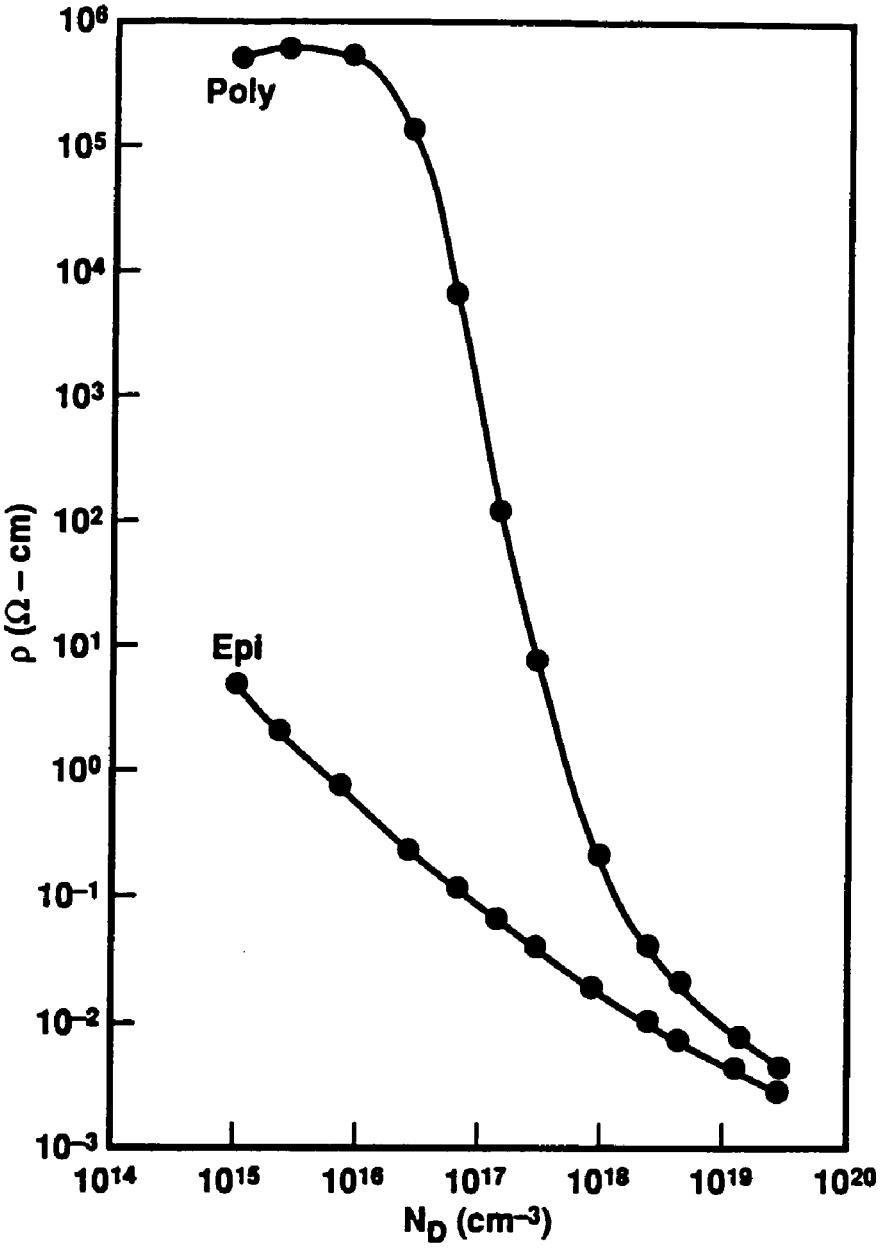


Figure 2-8. Resistivities versus doping concentration at room temperature for polysilicon and for single-crystal silicon[39].

Several models have been proposed to explain the resistivity behavior of polysilicon films. Two of the models, the dopant segregation model[40] and the carrier trapping model[5], will be discussed. This section will focus more on the dopant segregation model while the next section will focus on the carrier trapping model. In the dopant segregation model, the grain boundary acts as a sink for the preferential segregation of impurity atoms. It is hypothesized that, the resistivity variation is a result of impurity atoms segregating to the grain boundaries leaving few (ionized) impurity atoms in the intra-grain regions. As a result, few carriers are available for conduction at low dopant concentrations. However, as the dopant concentration is increased (approaching the degenerate doping level), the fraction of the segregated to the total dopant atoms decreases, resulting in a resistivity value that approaches that of single crystal silicon.

The factors that influence the distribution of dopant atoms between the grains and the grain boundaries are the "chemical effect" and the size of the dopant atom[41]. The chemical effect makes segregation more likely if adding the dopant atoms lowers the melting temperature of silicon. A size effect favors segregation of the dopant atom to the grain boundary, both when the dopant atom is larger or when it is smaller than silicon. It is believed that segregation lowers the energy by reducing the lattice strain. Thus, the tendency to segregate is favored by a greater difference in the size of the atom[41].

Additionally, the disorder structure of the grain boundaries provides low energy sites at which dopant atoms can be preferentially located. Because segregation is a thermodynamic process, it is reversible. Therefore, the amount of dopant segregated and the film resistivity can depend on the last annealing steps in the fabrication process.

2.4 Carrier Trapping Model

In the carrier trapping model[5],[41a] the grain boundary defect states trap a fraction of the carriers from the ionized dopant atoms in the intra-grain regions. Consequently, the number of free carriers available for conduction is reduced, and potential barriers are established at the grain boundary. These potential barriers lead to alternative carrier transport mechanisms in polysilicon films with respect to the conventional drift and diffusion mechanisms used in single crystal silicon films.

The "carrier trapping" model attributes the high resistivity observed at low dopant concentrations to the fact that most of the carriers available for conduction are trapped at the grain boundary. The number of trapped carriers and the potential barrier adjacent to the grain boundary increase as the dopant concentration increases. Beyond a critical value, Ncr, a further increase in dopant concentration leads to an increase in the fraction of free carriers to the total dopant concentration and to a reduction of the potential barrier at the grain boundary. As

a result, the resistivity is sharply reduced. Any additional increase in dopant concentration reduces the potential barrier at the grain boundaries, and the number of free carriers approach that of a the total dopant concentration. As a result, the resistivity approaches that of single crystal films.

To derive the current equations of the carrier trapping model, the following assumptions were made:

(a) all impurity atoms are ionized and are uniformly distributed.

(b) grain sizes are uniformly distributed and are of equal length.

(c) the single crystal silicon energy band structure can be used in the intragrain regions.

(d) the one dimensional approximation is valid.

(e) the depletion approximation is applicable.

(f) the grain boundaries electrical properties are equivalent.

(g) the grain boundaries have negligible effective width.

It will also be assumed that defects at the grain boundaries are present at a density, Nt, and are located at a single energy level, Et, measured relative to the intrinsic energy level at the grain boundary. This simplification is appropriate because the trap density at the grain boundaries have been observed to peak at midgap[42],with the Fermi level at 0.62eV below the conduction band edge[43] . It is also assumed that the trap states are initially neutral and become charged when carriers are trapped.

The average carrier concentration and the potential distribution in the intragrain region can be obtained by considering the charge trapped in the grain boundary defect states to be equal to the depletion charge in the adjacent intragrain regions. Consider the grain boundaries of zero effective width located at 'x' = ±nL, as shown in figure 2.9. L is the grain length and 'n' is an integer.

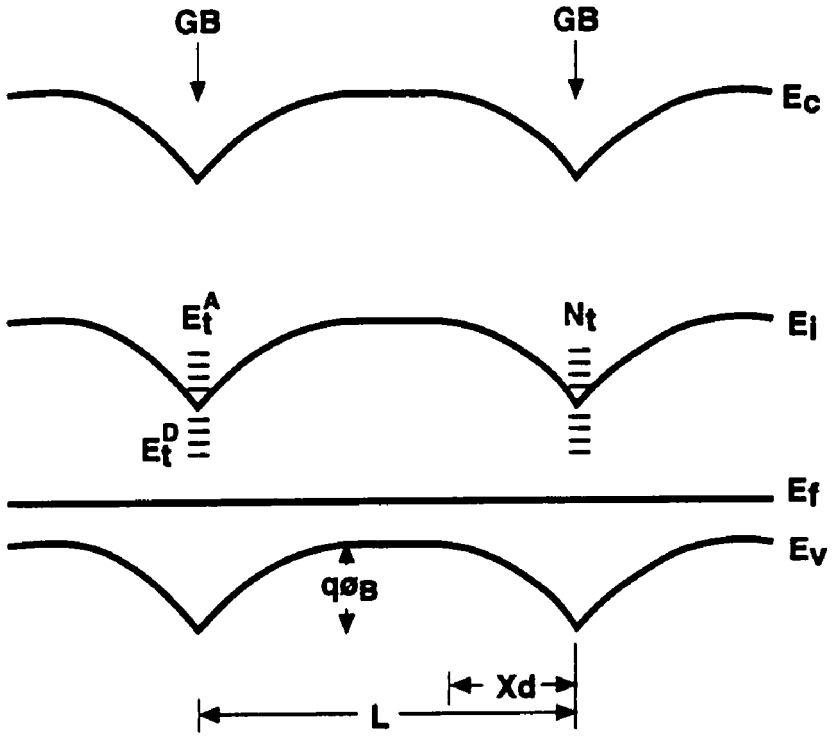


Figure 2-9. Equilibrium potential energy band diagram for n-type polysilicon with depletion width less than L/2 showing the assumed acceptor and donor type trapping states.

In figure 2.9, a depletion region of length (L/2) is formed on both sides of the grain boundary when carriers are trapped at the grain boundary states. The Fermi level is assumed to be pinned at the grain boundaries by the presence of a large trap concentration; the trapped charge is responsible for the band bending that creates the potential barrier at the grain boundary. This potential barrier can be calculated using Poisson's equation at equilibrium conditions for the curvature formed in the energy bands by taking the energy difference between the center of the grain and the grain boundary.

$$\frac{\partial^2 \varphi(x)}{\partial x^2} = \frac{qN}{\epsilon}; 0 \leq |x| \leq x_d \text{ ----------} (2.8)$$

where

N is the ionized dopant concentration (cm^{-3}),

$\varphi(x)$ is the electrostatic potential ,

x_d is the depletion width,

q is the electronic charge, and

ϵ is the permitivity of the polysilicon film.

Using $\partial\varphi(\pm x_d)/\partial x = 0$ as the boundary condition, while keeping $\varphi(x)$ continuous, equation (2.8) can be integrated twice to obtain the band bending potential expressed as a function of position, $\varphi(x)$.

$$\varphi(x)=\varphi(x_d)+\frac{qN}{2\in}(|x|-x_d)^2;0\leq|x|\leq x_d \text{--------(2.9)}$$

where $\varphi(x_d)$ is the potential of the conduction band edge at the center of a crystal. The two cases of interest are when the adjacent intragrain regions are fully depleted, such that $x_d = L/2$ or when the intragrain regions are partially depleted such that $x_d < L/2$. The conductivity transition from a high to a low resistivity in polysilicon at a low dopant concentration occurs at (Ncr), which is determined by the dopant concentration at which a quasi-neutral region appear at the center of the grains. While assuming that all carriers available for conduction are trapped, for N<Ncr, charge neutrality between the negatively charge filled states and the positively ionized donors require that

$$N_c=\frac{N_t}{L} \text{----------(2.10)}$$

In this case, the intra-grain region is fully depleted, the potential barrier along the grains is given by equation (2.9) and the equilibrium potential barrier height, φi, is the difference between $\varphi(0)$ and $\varphi(L/2)$, and is given from equation (2.9) to be

$$\varphi i = \frac{qL2}{8\epsilon} N \text{----------(2.11)}$$

Since the boundary condition $\partial\varphi(\pm x_d)/\partial x = 0$, the result is a small grain boundary potential barrier height for a small N or a small L. The energy needed to surmount the barrier is '$q\varphi i$' (eV). It can be surmised from equation (2.11) that the potential barrier height increases linearly with the ionized dopant concentration, N. By assuming that N is equivalent to the net acceptor type dopant concentration, the average mobile carrier concentration of electrons, n^-, is given by

$$n^- = \frac{2}{L} \int_0^{L/2} n(x)dx \text{----------(2.12)}$$

n(x) can be estimated using Boltzmann statistics to be

$$n(x) = nie^{-\frac{q(\varphi(x)-\phi_n)}{kT}} \text{----------(2.13)}$$

where $\varphi(x)$ is equivalent to $\{-(Ei - Eo)/q\}$, and ϕ_n is equivalent to $\{ -(Ef - Eo)/q\}$ the constant Fermi potential for the equilibrium case. Eo is a reference energy, T is temperature in Kelvin, 'ni' is the intrinsic carrier concentration and k is Boltzmann's constant. If the intrinsic Fermi energy, 'Ei', is equal to Eo at 'x' = $\pm$ L/2, then $\varphi(L/2)$ is equivalent to zero and,

$$\varphi(x) = \frac{qN}{2\in}(|x| - \frac{L}{2})^2; 0 \leq |x| \leq \frac{L}{2} \text{----------(2.14)}$$

The average electron concentration can now be obtained by substituting equations (2.14) and (2.13) into (2.12) to obtain

$$n^- = \frac{ni}{qL} e^{\frac{q\phi_n}{kT}} \sqrt{\frac{2\pi kT\in}{N}} erf(\frac{qL}{2}\sqrt{\frac{N}{2kT\in}}) \text{--------(2.15)}$$

$$erf(t) = \frac{1}{\sqrt{\pi}} \int_{-t}^{t} e^{-x^2} dx \text{----------(2.16)}$$

The value of ϕ_n can be obtained from equation (2.17). Equation (2.17) allows the average carrier concentration to be expressed as a function of grain length, dopant concentration and trap energy level[43a].

$$NL = N_{gb}\left(\frac{1}{1+2e^{(\Delta E_t - q\phi_n + q\varphi i)/kT}} - \frac{1}{1+2e^{(\Delta E_t + q\phi_n - q\varphi i)/kT}}\right) \quad (2.17)$$

where

Ngb is the density (cm^{-3}) of the two discrete trap levels at each grain boundary located at energies, '±Et', with respect to the intrinsic Fermi level, 'Ei'.

For the partially depleted intragrain region case ($x_d < L/2$), there exist a value of N for which $x_d \leq L/2$. This corresponds to the condition that the magnitude of the charge trapped at the grain boundary is less than qNL. The equilibrium potential barrier for this case can be obtained by modifying equation (2.5) to yield:

$$\varphi i = \frac{qx_d^2}{2\epsilon}N \quad (2.18)$$

If we define the charge at the grain boundary, Qgb, to be $2qNx_d$, equation 2.18 can be modified to obtain an inverse relationship between the equilibrium potential barrier height and the dopant concentration.

$$\varphi i = \frac{Q_{gb}^2}{8q \in N} \text{----------(2.19)}$$

Equations 2.9, 2.12, and 2.13 result in the average carrier concentration

$$n^- = \frac{ni}{qL} e^{\frac{q\phi_p}{kT}} \left(\sqrt{\frac{2\pi kT\in}{N}} erf\left(qx_d \sqrt{\frac{N}{2kT\in}}\right) + q(L - 2x_d)\right) - (2.20)$$

Since we are concerned with partially depleted intragrain region , ϕ_n can be obtained by assuming that the dopant concentration is equivalent to the carrier concentration . Thus,

$$\phi_n = \frac{kT}{q} \ln\left(\frac{n}{ni}\right) \text{----------(2.21)}$$

The average carrier concentration has been used to derive the effective mobility[5] in terms of the material resistivity, ρ, and is given by:

$$\mu_{eff} = \frac{1}{q\rho n^{-}} \text{----------} (2.22)$$

The basic results of the trapping model derivation is that for low dopant concentration and fully depleted grains, the equilibrium potential barrier height is directly proportional to the dopant concentration and the square of the grain length. At a dopant concentration for which the intragrain region is partially depleted and the grain boundary charge is constant, the equilibrium potential barrier height is inversely proportional to the dopant concentration and directly proportional to the square of the grain boundary charge. The use of one dimensional analysis in this example is only valid for the case in which the depletion width is less than L/2. Otherwise, the grain should be considered as a three dimensional system with the trapped charge existing over the entire area of the grain.

Dopant segregation and carrier trapping have been considered independently. However, modification of the electrical properties of the grain boundaries can result from the segregated dopant[44] . This is because the dopant atoms segregating to the grain boundaries may interact with the dangling bonds and other defects to satisfy some of the unsaturated bonds and reduce the trap density and film resistivity. Therefore, as the dopant segregates, dopant loss from the substitutional sites within the polysilicon grains increases the resistivity.

However, the reduction in carrier trapping that accompanies this process tends to reduce the overall resistivity[45] . These effects are readily observable in a moderately doped polysilicon films.

2.5 Grain boundary passivation

As mentioned at the beginning of this chapter, the grain boundaries contain unwanted traps which degrade the electrical properties of polysilicon films, and, consequently, the devices fabricated with it. The two main approaches to reduce the active trap density are (1) to remove or reduce the grain boundaries via grain enlargement processes, and (2) to reduce the effectiveness of the trap sites by hydrogen passivation. This section will examine the hydrogen passivation technique.

Traps are associated with dangling bonds at the grain boundaries arising from lattice discontinuities that form when differently oriented grains join. These dangling bonds can be passivated with atomic hydrogen to reduce the number of active trapping states[10], [11], [12], [13] . As the number of trapped carriers decreases, the potential barrier associated with the grain boundary also decreases and the device performance improves (figure 2.10). Because hydrogen is not firmly bound to silicon, passivation is rapidly lost from the grain boundaries by annealing at temperatures in excess of 400°C[46] [47] . Therefore, hydrogenation must be done after the device has seen all high temperature treatments. It must be emphasized

that passivation of the grain boundaries to the maximum extent possible does not eradicate all the active grain boundary states.

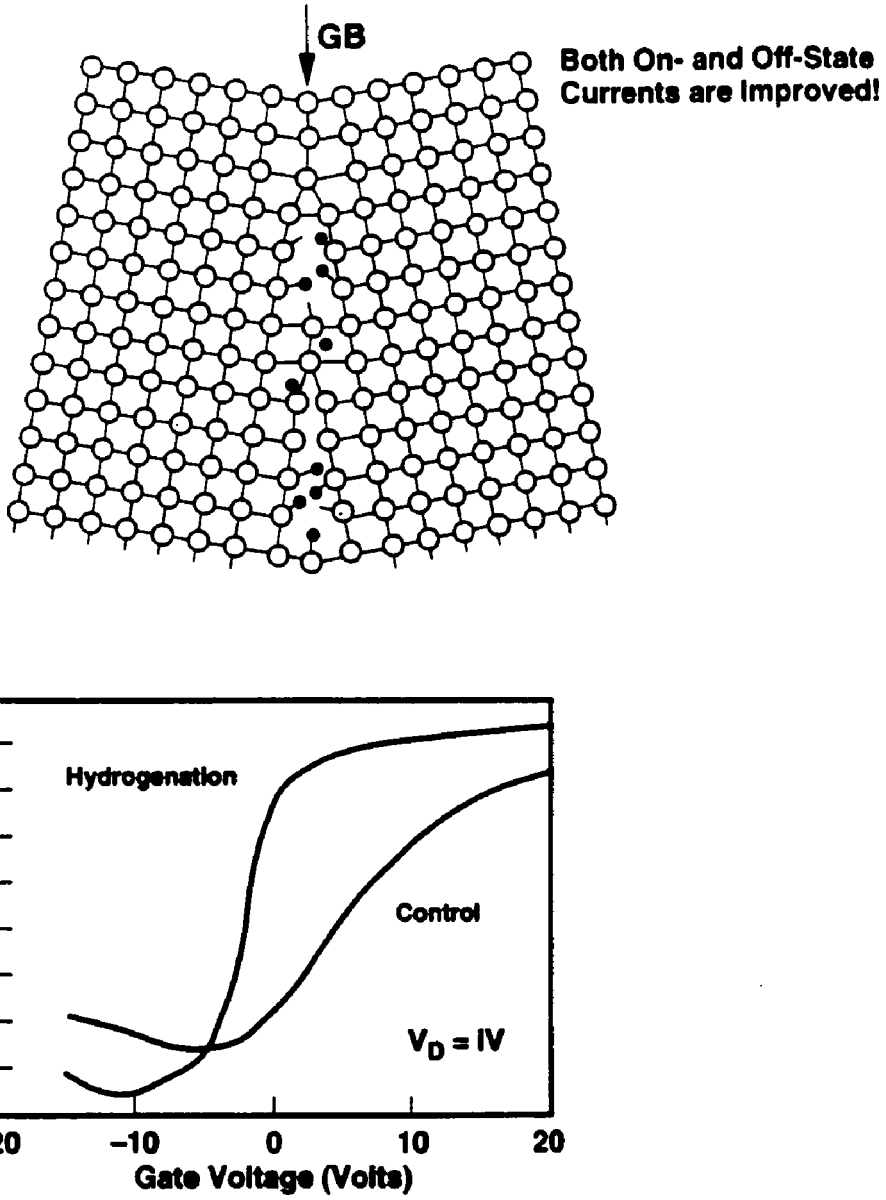


Figure 2-10. Effect of hyrogen passivation on grain boundaries and device performance.

Chapter 3 TFT EXPERIMENT AND FABRICATION

3.1 Introduction

The purpose of this study is to examine the causes of off-state leakage current in submicron thin-film-transistors and to investigate how the drain offset structure can be used to reduce it. With a good understanding of the effect of the drain offset on the leakage current, better techniques can be devised to lower the TFT off state leakage current. To achieve these goals, P channel TFT's were fabricated. The TFT devices have channel length (Lch) varying from 1.0μm to 0.35μm and their channel widths vary from 0.8μm to 0.35μm. Additionally, the drain offset length will vary from 0.0μm to 1.0μm. In this study, conventional substrate preparation procedures that incorporate grain-size enhancement [48] [49] will be used.

The TFT device structures are simple in design and they require few masks compared to MOSFETs. Although the devices were fabricated on an insulator, efforts are made to ensure that the processing steps are compatible with standard MOSFET process because these devices will be used as load devices in SRAM applications. This chapter begins with a description of the TFT test structures used in this study. The rest of the chapter will describe the processing sequence and will highlight the important fabrication steps.

3.2 TFT Process Sequence

In this work, two inverted TFT device structures were used. The main difference between the two testers is the drain offset design. One structure was designed with symmetrical drain and source offsets while the other is designed with an offset only on the drain side of the device. As indicated in figure 3.1, the TFT device fabrication starts with the deposition of a thick undoped LPCVD oxide on a silicon wafer followed by 1200Å degenerately (phosphorous) doped polysilicon gate electrode. An N-type gate electrode was used to guaranteed compatibility with the NMOS load drivers in SRAM designs. The gate definition is followed by the deposition of 180Å gate oxide and a low temperature (550°C) deposition of 500Å of α-Si for the TFT channel. The LPCVD α-Si thickness was carefully chosen to minimize the topography during fabrication.

In the symmetrical drain/source offset structure, a thick (6000Å) layer of undoped plasma enhanced SiO_2 was deposited on the channel α-Si, and the source and drain were defined by photolithography. An oxide mask (figure 3.1(c)) was formed on the channel following anisotropic plasma etching of the thick oxide. This particular step allowed the drain offset to be implanted. To arrive at step (d) in figure 3.1, another thick (4000Å) layer of plasma enhance SiO_2 was deposited followed by complete etchback of the deposited SiO_2 to form a spacer around the oxide mask. The spacer layer formed the offset length. Depending on the thickness of film deposited, it can be used to form different offset lengths. Subsequent

process steps include the source and drain implants and deposition of dielectric layers for isolating metal contacts from device terminals as depicted in figure (3.1 d & e). Note that the dielectric must also isolate the driver transistors from the access transistors and planarize the underlying topographies to ensure adequate depth of focus for the subsequent photolithography steps.

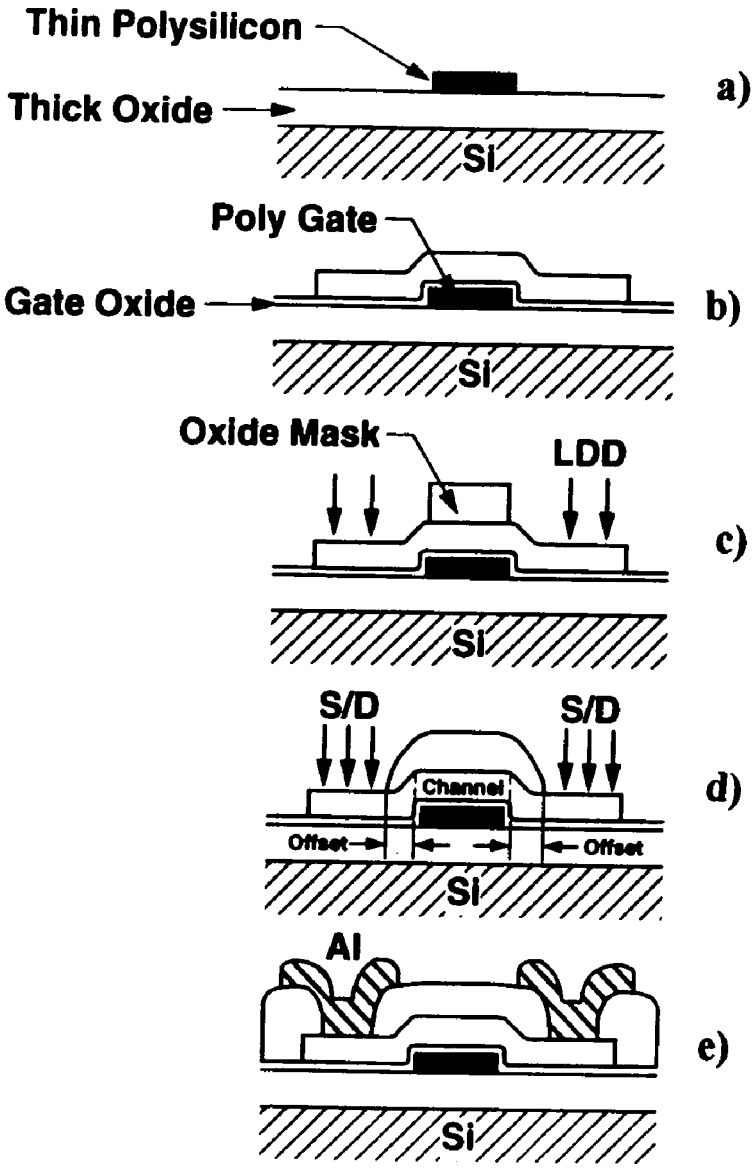


Figure 3-1. The inverted TFT structure showing symmetrical source/drain offset process sequence

For the other device structure, one additional mask level (drain offset mask) was used to define the drain offset. As indicated in figure 3.2, steps (a), (b) and (e) are similar to the previously described tester in figure 3.1. Instead of an oxide mask, photoresist was used to define the source, the drain, and the drain offset regions. This structure provide a drain offset length that ranged from 0.0μm to 1.0 μm. Since the leakage current is attributed to the carrier emission from the drain depletion region, this structure is particularly useful to study the TFT leakage effects (see Appendix A for process sequence).

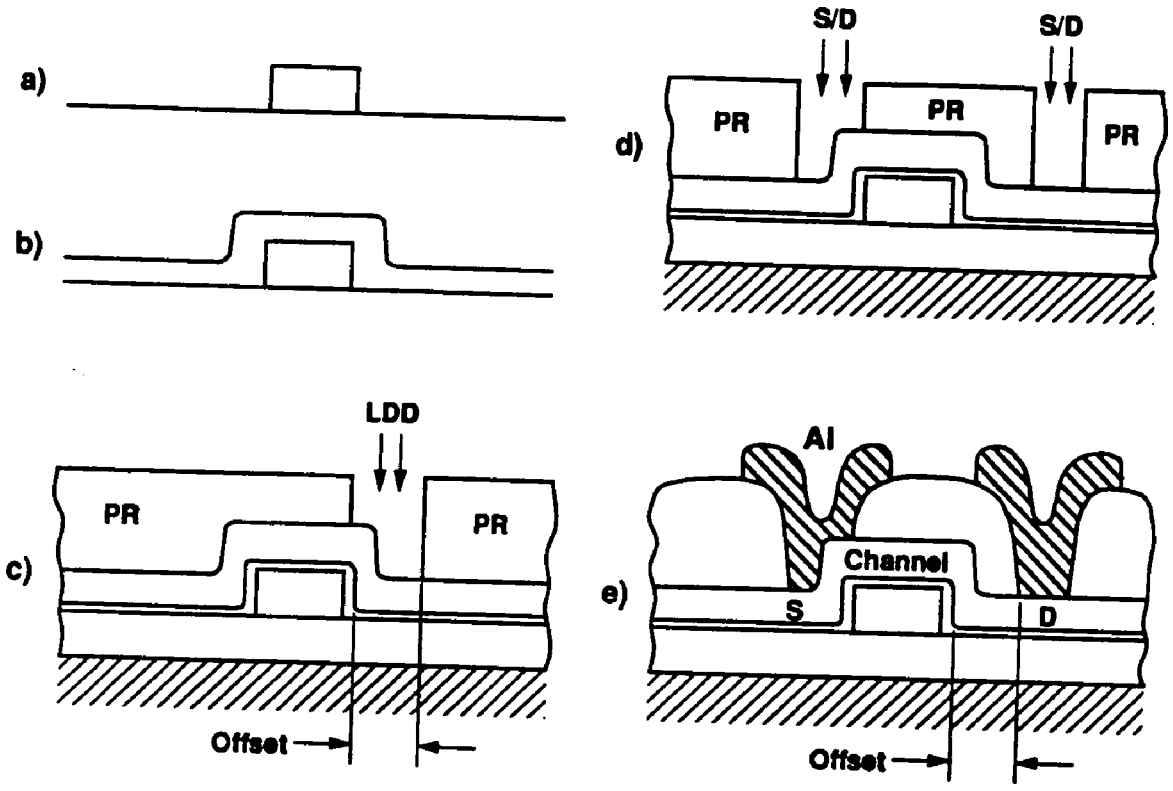


Figure 3-2. The inverted TFT structure showing drain offset structure and process sequence.

The gate and channel etching were carried out in a state-of-the-art etching reactor using combinations of 40% Hydrogen Bromide (HBr) and 60% Helium (He) gases. This combination was chosen based on previous work, to prevent undercuts, stringers (see Appendix B for process issues) and tapering. Although tapering the gate edges may be beneficial in reducing the corner electric field, uniformity and reproducibility may be compromised. Additionally, chemical cleans in subsequent process steps may preferentially etched away the oxide.

3.3 Test Transistors

The test transistors have channel lengths that range from 0.35μm to 1.0μm and channel widths that range from 0.35μm to 1.4μm. The offset length on the structure with only a drain offset ranged from 0.0μm to 1.0μm. As shown in figure 3.3, (the structure with symmetrical offsets) the transistors share common source and common gate contacts but each have separate drain contacts.

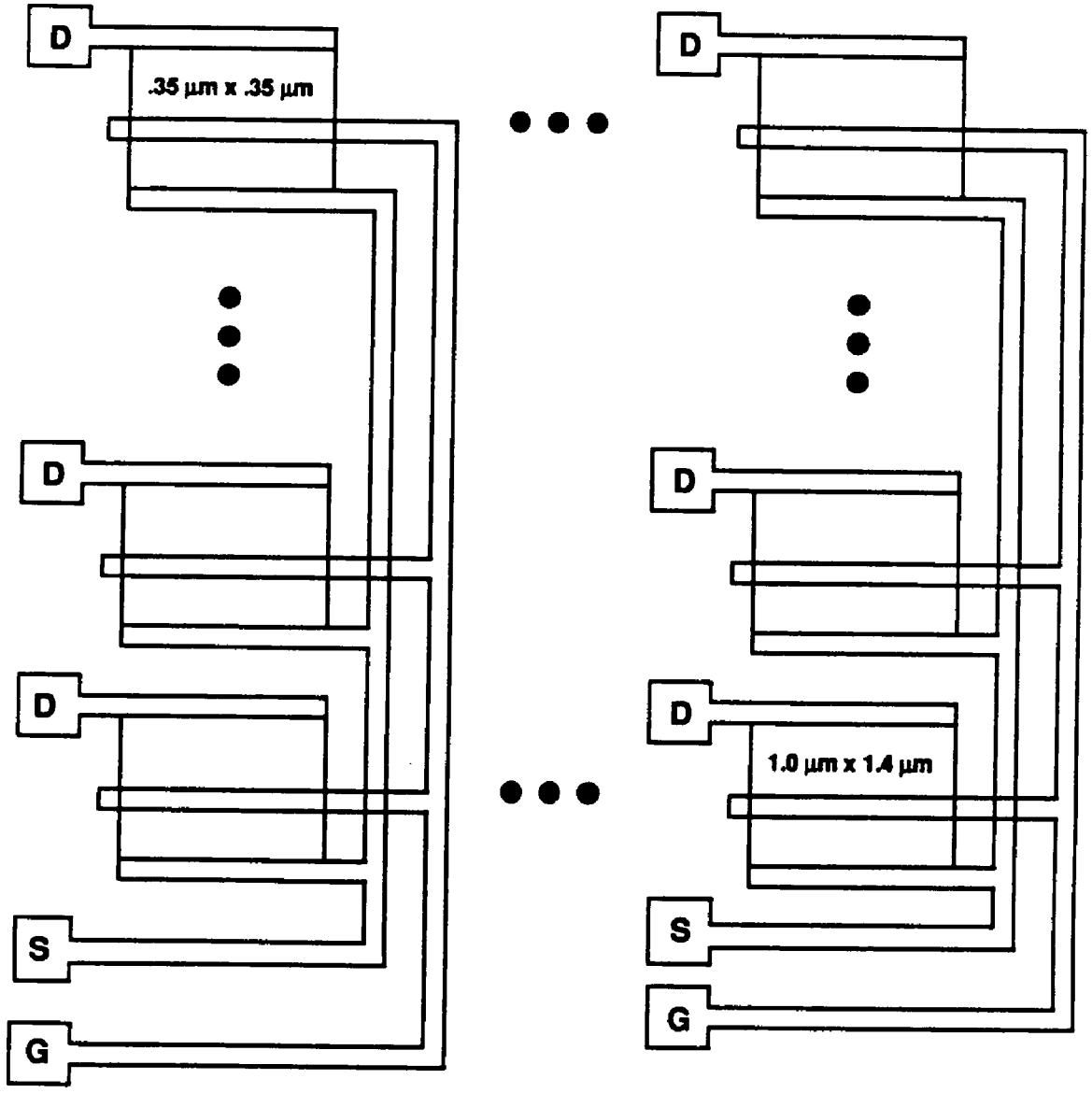


Figure 3-3. Schematic illustration of test transistor layout for the symmetrical offset structure

Each transistor in the drain offset only structure share no contacts with other transistors. The transistor arrays have varying lengths, varying widths and varying offset lengths. A schematic illustration is shown on figure 3.4.

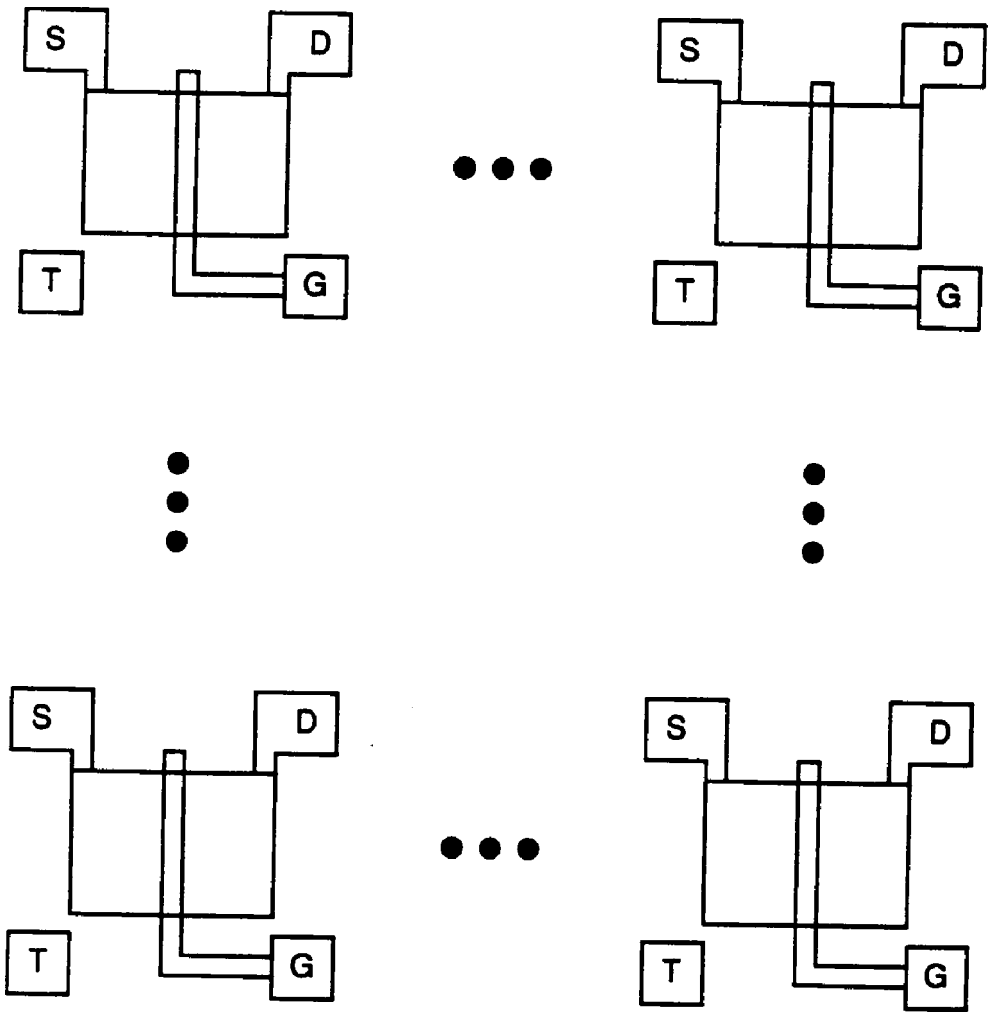


Figure 3-4. Schematic illustration of test transistor layout for the asymmetrical drain offset structure.

3.4 Test facilities

The electrical test equipment used for this study consists of a Hewlett-Parckard (HP) Model 4145B Semiconductor Parameter Analyzer, a wafer probe station, a Hewlett-Packard switching matrix, a Temptronic temperature controller, and an HP 7470A plotter (figure 3.5).

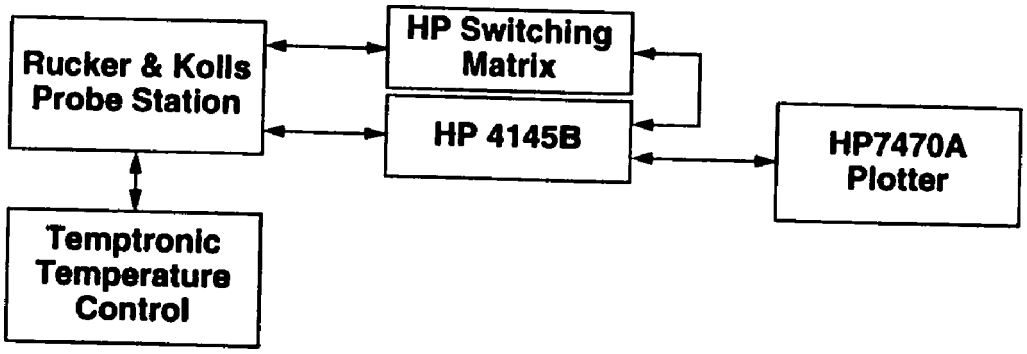


Figure 3-5. Block diagram showing the electrical test equipment

Chapter 4 DEVICE CHARACTERIZATION

4.1 Introduction

The objective of this dissertation is to study the effect of the drain offset on the leakage and drive currents of submicron Polysilicon thin-film transistors (TFTs). This chapter will focus on the characterization techniques and the results obtained from this study. Using the equipment described in the previous chapter, the I_{ds}-V_{ds}, threshold voltage, effective mobility, I_{on}/I_{off} characteristics, subthreshold swing, leakage (off state current) and the drain current activation energy will be characterized. In this chapter a qualitative explanation of the measured device characteristics will be provided, and an analytical expression that explains the electrical behavior will be developed in chapter 5.

The channel lengths of interest ranged from 1.0μm to 0.35μm while the channel widths vary from 0.35μm to 1.4μm. The drain offset length ranged from 0.0μm to 1.0μm. The drain offset region implant dosage ranged from 1E12 to 3E14 atom/cm^2, and the channel implant dosage ranged from 0.0 to 6E12 atom/cm^2. Since this work was directed towards static memory (SRAM) applications, most of the transistors were fabricated with 180Å gate dielectric. However, results from transistors fabricated with 500Å gate dielectric will also be presented.

4.2 Device characteristics

This section will focus on device characterization; both measurements and results will be discussed. All result presented are average of eighteen data points.

4.2.1 Drain characteristics (I_{ds} vs. V_{ds})

The drain current as a function of drain voltage (I_{ds} vs. V_{ds}) was measured with the drain and gate terminals biased relative to the source terminal as depicted

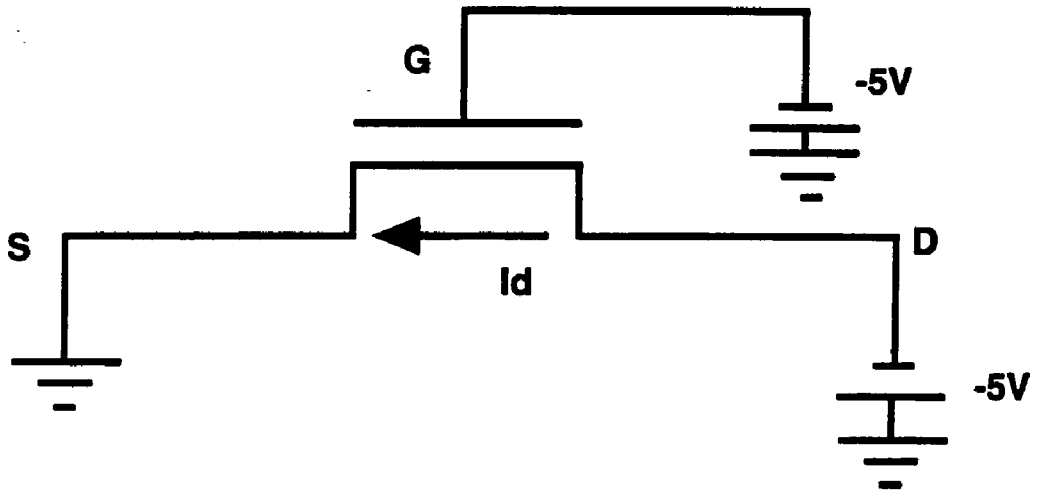


Figure 4-1. Schematic diagram of biased circuit for drain current versus drain voltage measurement.

In this measurement both the drain and gate voltages were ramped from 0.0 volts to -6 volts at -0.05 volt and -1.0 volts, respectively. With this arrangement the drain current as a function of drain voltage can be measured at different gate voltages.

In figure 4.2 the I_{ds}-V_{ds} characteristics for different gate voltages are shown for a device having channel length and channel width of 0.35μm and 0.35μm, respectively. In figure 4.2 no significant short channel effects were observable for drain biases less than -10 volts. However, above -10 volts on the drain, an increase in drain current was observed. This increase can be attributed to the drain-induced barrier lowering effect. Further increase of drain bias above -15 V will result in punch-through. This is not surprising since at V_{ds} = -12 volts, the drain depletion width is estimated to be about 0.29 μm, which is more than 80% of the source to drain separation. Similar inferences can be drawn in figure 4.3, except that the gate and drain voltages are held at -6 volts because the gate dielectric is only 180Å thick. For drain voltage less than -5.0 volts, the beginning of punch-through effect was observed.

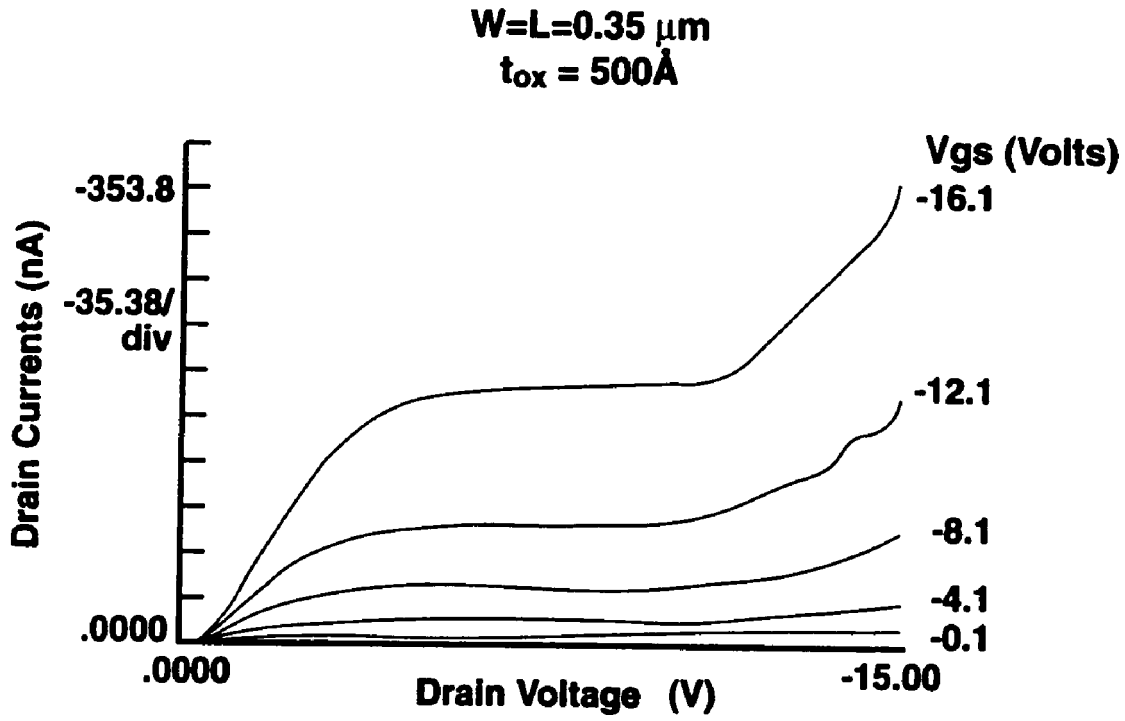


Figure 4-2. I_{ds}-V_{ds} characteristic for 0.35 μm x 0.35μm poly-Si TFT's with several gate biases (W = L = 0.35 μm, Offset = 0.35μm, t_{ox} = 500Å. Vgs = -2.0 volts → -10.0 volts).

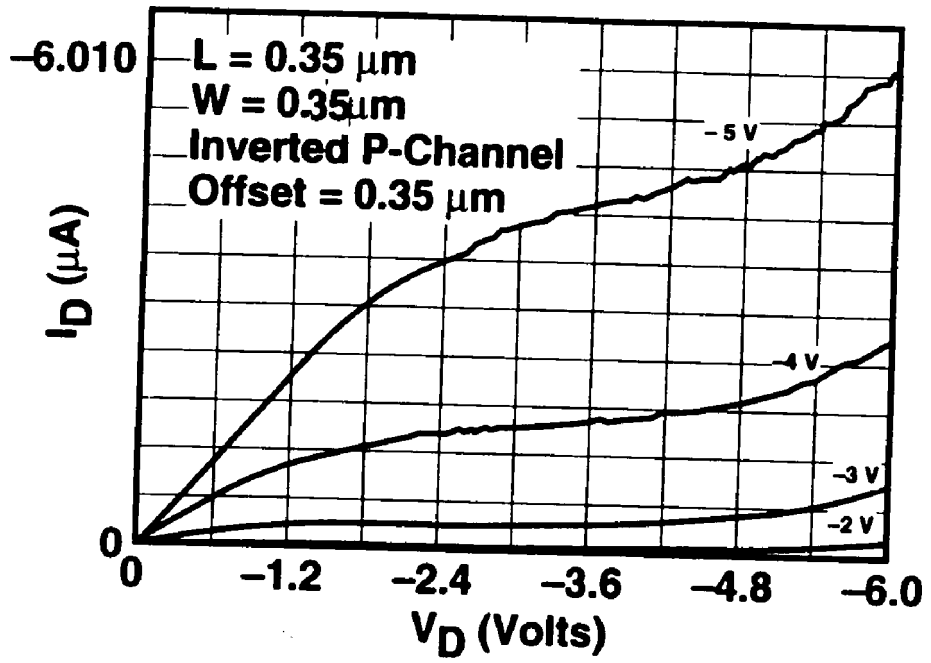


Figure 4-3. I_{ds}-V_{ds} characteristic for 0.35 μm x 0.35μm poly-Si TFT's with several gate biases (W = L = 0.35 μm, Offset = 0.35μm, t_{ox} = 180Å. Vgs = -2.0 volts → -5.0 volts).

.4.2.2 Threshold voltage(Vt)

The gate-to-source voltage required to create the surface inversion necessary to form a conducting channel between the drain and the source region is called the threshold voltage, V_t, of the transistor. The V_t is found experimentally by measuring the drain current variation as a function of the gate voltage for a fixed drain voltage. Usually a drain voltage of -0.1volts is used because it causes the transistor to operate in the linear region. A line that can be extrapolated to the gate voltage intercept is then drawn along the I_{ds} curve at the maximum transconductance (gm) point. At the maximum gm point, V_t is given by the MOSFET drain current equation as:

$$Vt = V_{gs} - \frac{I_{ds}}{g_m V_{ds}} - \frac{V_{ds}}{2} \qquad (4.1)$$

Where:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{\mu \in_{ox}}{t} \frac{W}{L} \quad \text{and}$$

μ = channel mobility which will be defined later in this chapter,

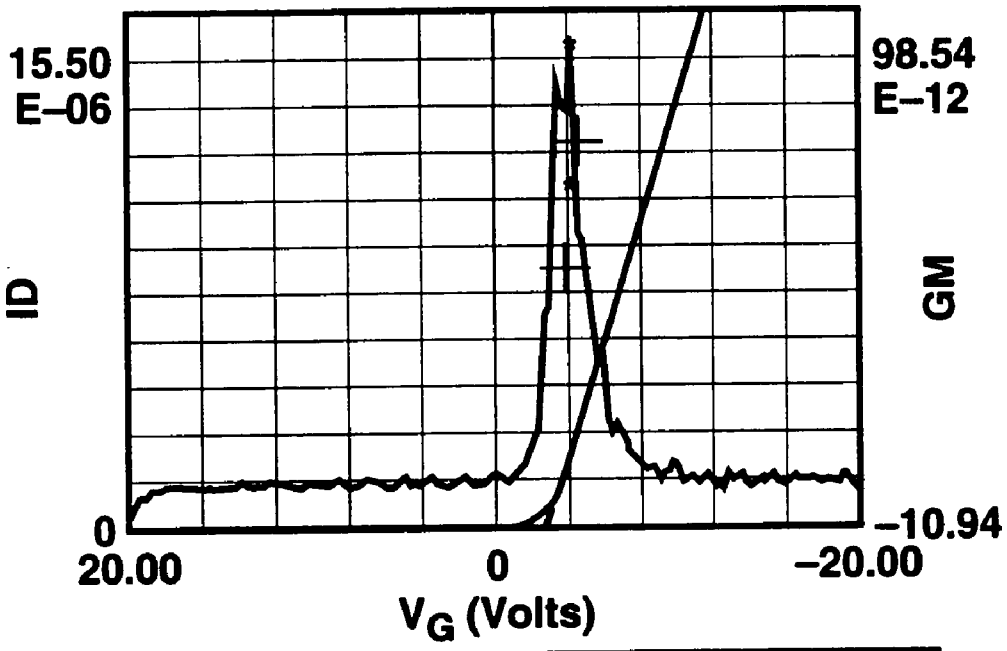
L = channel length,

$\in$ = dielectric permitivity

W = channel width, and

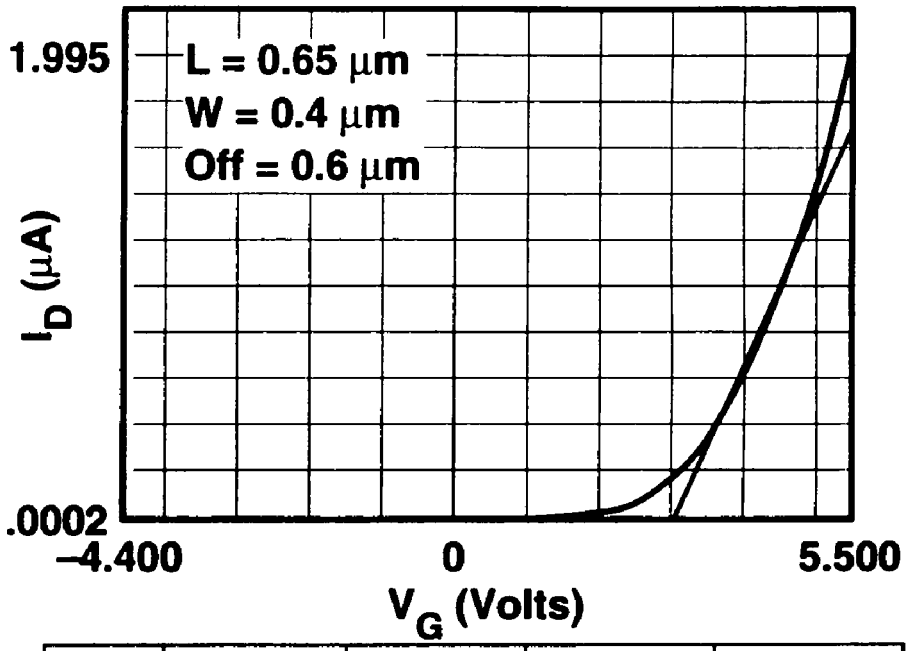
t = gate oxide thickness

The method described above is known as the maximum transconductance method of obtaining the threshold voltage. Vt is defined as the linear extrapolation of the I_{ds} curve to the V_{gs} axis at the point of maximum β. Representative plot of both techniques are shown on figures 4.4 and 4.5 for 0.6μm by 0.4μm devices.



	Grad	1/Grad	Xintercept	Yintercept
Line 1	-4.33E-06	-231E+03	-1.61E+00	-6.98E-06
Line 2				

Figure 4-4. Representative plot of I_{ds} vs. V_{gs} showing V_t for a 0.6μm by 0.4μm device (W = 0.4μm, L = 0.6 μm, Offset = 0.35μm, t_{ox} = 500Å. Vds = -0.1 volts).



	Grad	1/Grad	Xintercept	Yintercept
Line 1	6.12E–09	1.63E+06	3.27E+00	–2.00E–06
Line 2				

Figure 4-5. Representative linear plot of I_{ds} vs. V_{gs} showing V_t for a 0.6μm by 0.4μm device (W = 0.4μm, Offset = 0.6μm, L = 0.65 μm, t_{ox} = 180Å. Vds = -0.1 volts).

The continuous increase of the current at high drain voltages in figures 4.2 and 4.3 indicate a reduction in threshold voltage. Figure 4.6 summarizes the results for Vt as a function of V_{ds}. A large Vt shifts exist for devices without the drain offset structure, and the shift is more significant for short channel devices. As indicated in figure 4.6, the Vt reduction from the 1.0μm device to the 0.5μm device is more pronounced at higher V_{ds}. For V_{ds} below -4 volts, the slope has increased and the extrapolation of Vt becomes less accurate. With the drain offset structure, which will be discussed later in the chapter, the control of Vt is better and the reduction is smaller as V_{ds} decreases.

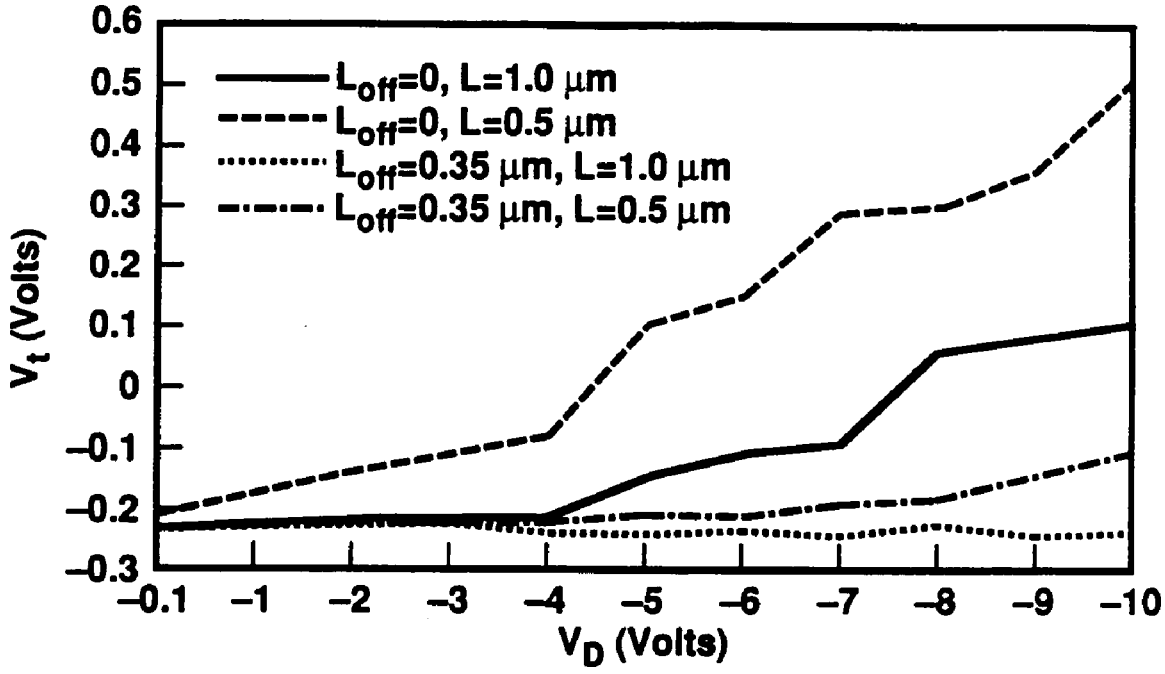


Figure 4-6. Threshold voltage (Vt) as a function of drain bias. Note how the effect of the drain offset structure suppresses short channel effects.

4.2.3 Qualitative explanation for the low threshold voltage (Vt)

The inverted TFT's have a complicated two dimensional potential distribution. At the threshold, the inversion charge is negligible compared to the space charge; both supported by the gate voltage. In a short channel device, the source and drain depletion regions also support a large portion of the space charge. As a result, the gate charge required to support the field across the gate oxide is reduced. Consequently, Vt is reduced. As V_{ds} increases the depletion region at the drain junction extends further into the channel and further reduces Vt. When a drain offset region is introduced, the drain junction electric field is reduced. Therefore, the reduction of Vt due to short channel effects is suppressed.

4.2.4 Carrier effective mobility

The effective carrier mobility (μ_{eff}) is obtained from the linear region of the I_{ds}-V_{ds} characteristics at constant gate to source voltage. From the drain current equation, μ_{eff} can be expressed as

$$\mu_{eff} = \frac{g_d}{\frac{W}{L} C_{ox}(V_{gs} - Vt)} \equiv \frac{\mu_o}{1 + \Theta(V_{gs} - Vt)} \text{----------(4.2)}$$

$$g_d = \frac{\partial I_{ds}}{\partial V_{ds}}; |V_{gs} = constant$$

Θ is the mobility degradation factor .

Figure 4.7 shows a representative plot of drain current as a function of drain voltage in the linear region for a 0.8μm channel length device. For this device the plot of effective mobility as a function of gate voltage is shown in figure 4.8. An extrapolation to the mobility axis gives μo. Given μo and μ_{eff} , the mobility degradation factor was calculated to be 1.1 /volts.

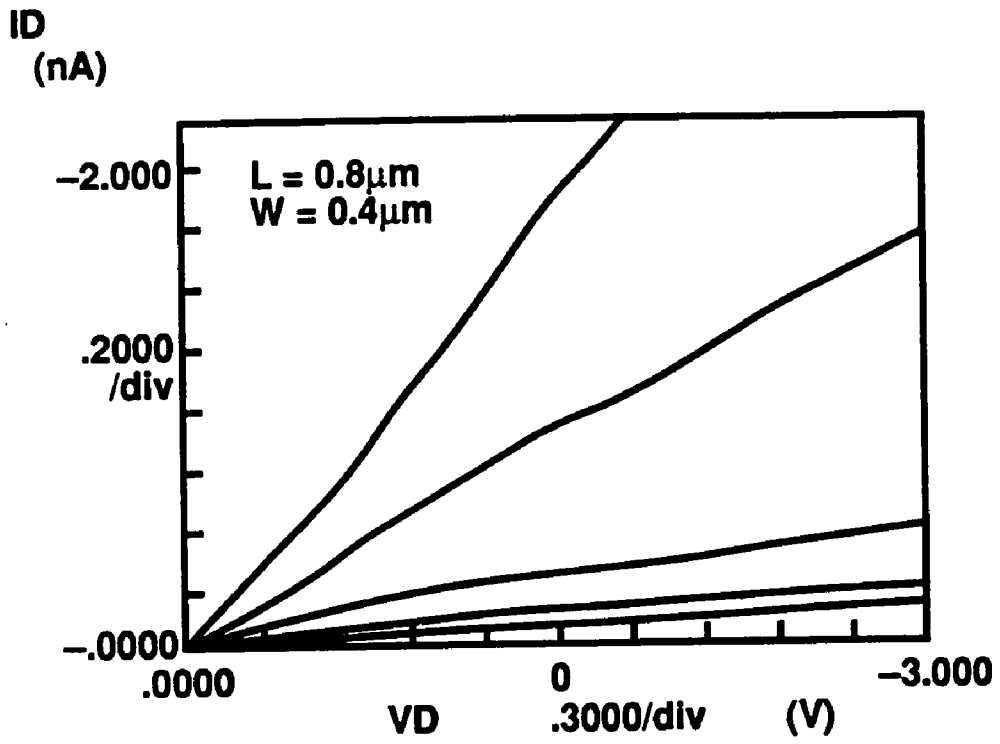


Figure 4-7. Representative plot of Ids-Vds used in mobility calculation (W = 0.4 μm, L = 0.8μm, t_{ox} = 180Å).

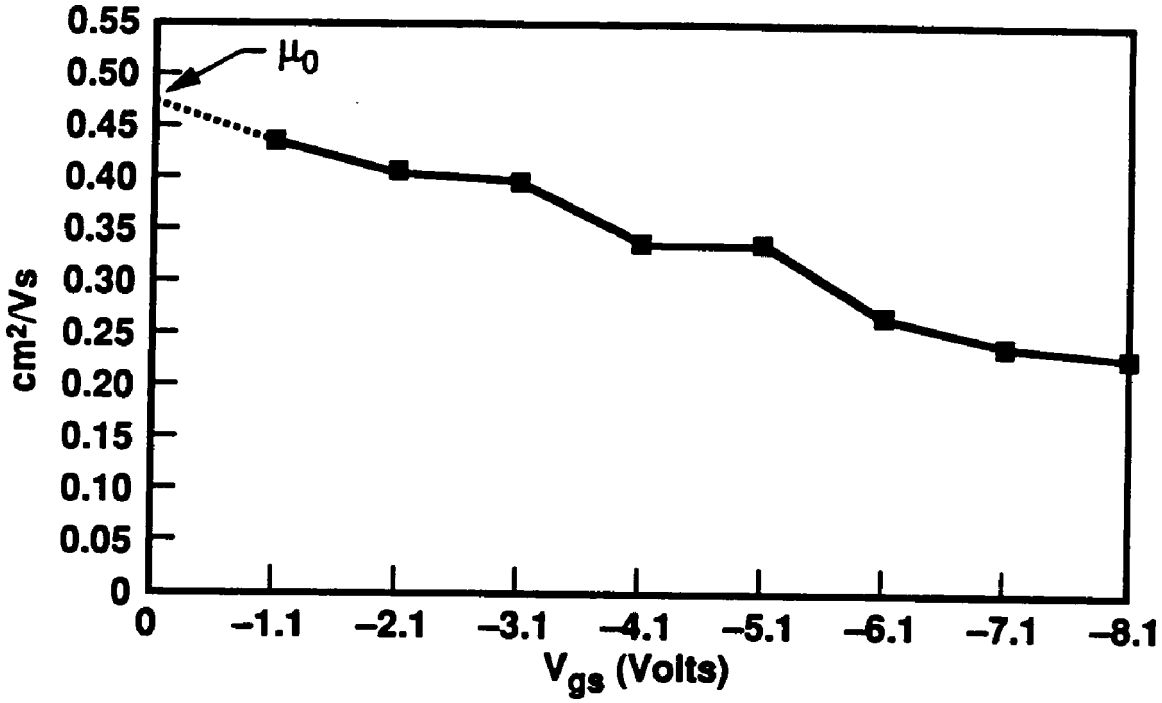


Figure 4-8. A plot of effective mobility as a function gate bias used to estimate the value of μo ($W = 0.4\ \mu m$, $L = 0.8\mu m$, $t_{ox} = 180Å$).

4.2.5 On/Off current characteristics

The Ids-Vgs device transfer characteristics show three regions of device operation, the off state leakage current region, subthreshold current region and the saturation current region. In order to obtain low leakage current, high drive current and a steep subthreshold slope, the grain boundary trap density must be low. The subthreshold slope gives an indication of the trap density in the channel because the gate voltage swing provides a relative measure of the number of induced carriers required to lower the grain boundary potential barrier that impedes carrier mobility in the channel. In this section, the leakage current, the drive current and the subthreshold swing will be examined as a function of drain bias, drain offset length and channel length.

The 'ON', 'OFF' and leakage currents (I_{on}, I_{off} & I_L) of polysilicon TFTs are found from the I_{ds} versus the V_{gs} characteristics curve for a fixed drain bias as shown in figure 4.9. I_{on} is the drain current at the device's operating voltage. For example, I_{on} for a -5 volt P-type TFT is the drain current at $V_{gs} = V_{ds}$ =-5 volts with the source and the substrate grounded. At these terminal biases, the transistor is in saturation. I_{on} indicates the current drive capability of the transistor. In this work I_{off} will be defined as the minimum drain current. The ratio of I_{on} to I_{off} serves as a figure of merit for the TFT. The leakage current is obtained by applying positive voltage to the gate of a P-channel device.

The I_{ds}-V_{gs} characteristics of the device with the channel width, channel length and length of drain offset length equal to 0.35μm is shown in figure 4.10. At a drain bias of -5 volts, in figure 4.10, the **"off"** (Ioff) current is 5pA and the **"on"** (Ion) current is 2.7μA, resulting in an Ion /Ioff current ratio of 5.4x105. As shown in the figure, I_{off} increases as the drain bias increases from -0.1 volts to -5.1 volts. This effect is the result of carrier emission from trap centers located in the drain depletion region. The emitted carriers readily contributed to the drain current in the "off" state because the potential barrier has been reduced by the drain field.

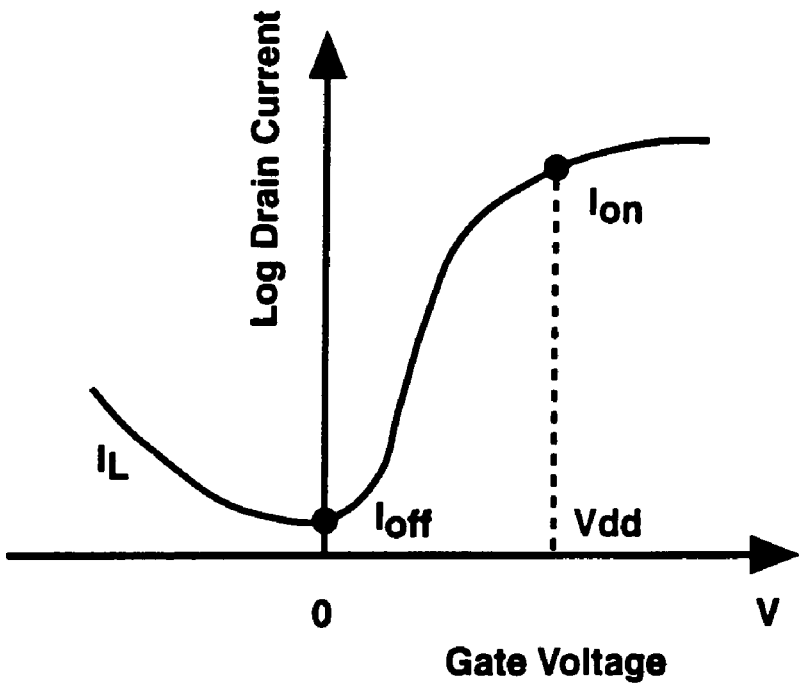


Figure 4-9. I_{on}, I_{off} & I_L in a Polysilicon TFT.

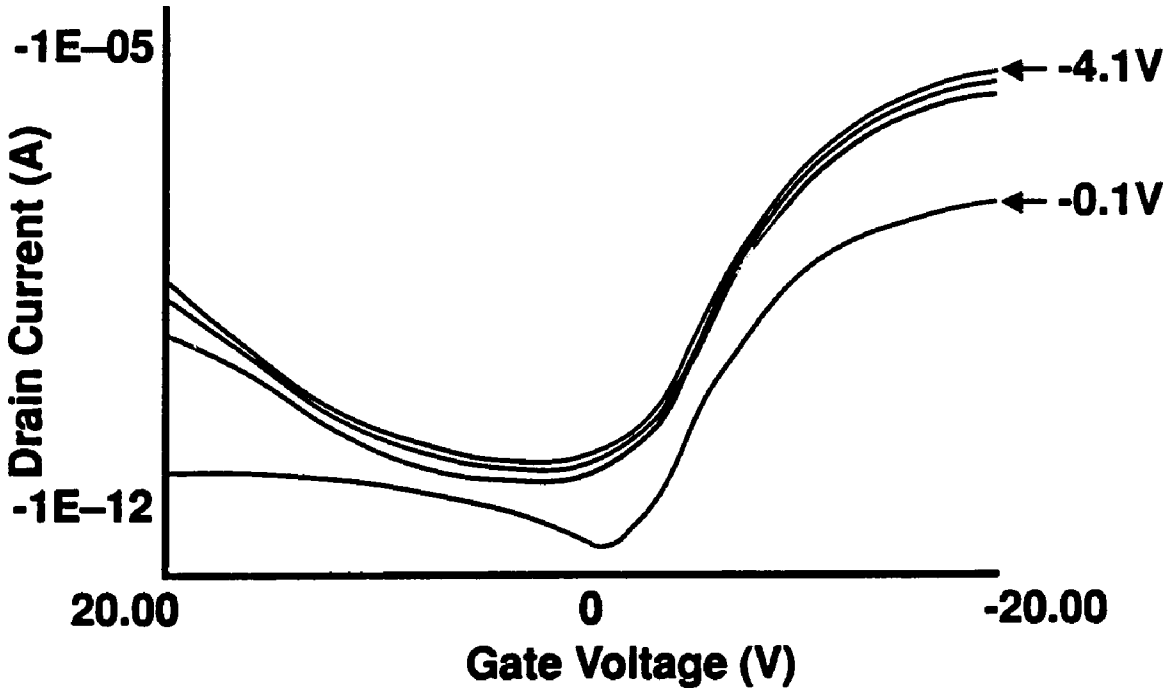


Figure 4-10. I_{ds}-V_{gs} characteristics for a poly-Si TFT's with L,W, and L_{off} equal to 0.35 μm for drain biases ranging from -0.1 volts to -4.1 volts.

For the sub-half micron device presented above, the switching characteristics are broad and the subthreshold slope (S) ranges from 660 mV/decade to 800 mV/decade of current. Because the on-currents (I_{on}) are low, the effective mobility (μ_{eff}) at low drain voltage (-0.1 V) are very low. The average values summarized in table I are not uniformly distributed. As such, no general correlation to channel length can be made. It has been reported [50] that further reduction of I_{off} is achievable after the passivation of the dangling bonds at the polysilicon grain boundaries with atomic hydrogen. As such, further improvement in I_{on} and subthreshold characteristics is expected after hydrogenation.

Table 4.1 Poly-Si TFT characteristics as a function of channel length (W=0.6μm).

Coded Channel Length (μm)	I_{on}/I_{off}	S (mV/decade)	μ_{eff} (cm^2/V.s)
1.0	$4.1x10^5$	762	0.193
0.9	$8.1x10^5$	763	0.196
0.8	$6.8x10^5$	662	0.300
0.7	$6.4x10^5$	734	0. 540
0.6	$4.9x10^5$	737	0.183
0.5	$4.4x10^5$	763	0.023
0.4	$3.3x10^5$	792	0.049
0.35	$5.4x10^5$	800	0.086

The classical p-n junction[51] diffusion current model can not explain the enhanced leakage current seen at large gate or drain biases. Carrier generation from the traps in the drain depletion region has been found to cause leakage currents in TFTs. In particular, thermionic field emission of carriers from the drain space charge region has been considered[52] . Although this model explains the leakage current mechanism at low field, it does not explain the increase in leakage current seen at high field. This observation suggest the existence of an additional mechanism, possibly carrier tunneling.

In this work the anomalous leakage current of the polysilicon TFT increases with gate and drain to source voltage(figure 4.11). As shown in the figure, the leakage current increases linearly with increasing drain bias. This suggests that channel behaves like a resistor. However, the leakage current dependency on gate bias is exponential. The increase in leakage current can be attributed to carrier emission and carrier tunneling from the traps located in the drain depletion region. The minimum leakage current (see figure 4.12 (a) & (b)) at V_{ds} = -5 volts showed no unique dependency on the channel dimensions. This is contrary to an earlier report[53] where a unique dependency was observed for devices with larger polysilicon grain size. In this study channel lengths $\leq$ 1.0 μm and channel widths $\leq$ 1.4 μm were examined. Note that the average polysilicon grain size was 0.4 μm. The result shown in figure 4.11(a) is for a 0.6 μm channel width. Contrary to the result of figure 4.12(a), the minimum leakage current shown in figure 4.12(b) exhibited a dependency on channel width. Although minimal, the leakage current

increases as the channel width increases from 0.4 μm to 1.4 μm. In both instances, the leakage current was less than 11 pA.

To better understand the leakage mechanism, the temperature dependence of the TFT drain current will be measured and analyzed in the next section. The results will be used to develop a leakage current model.

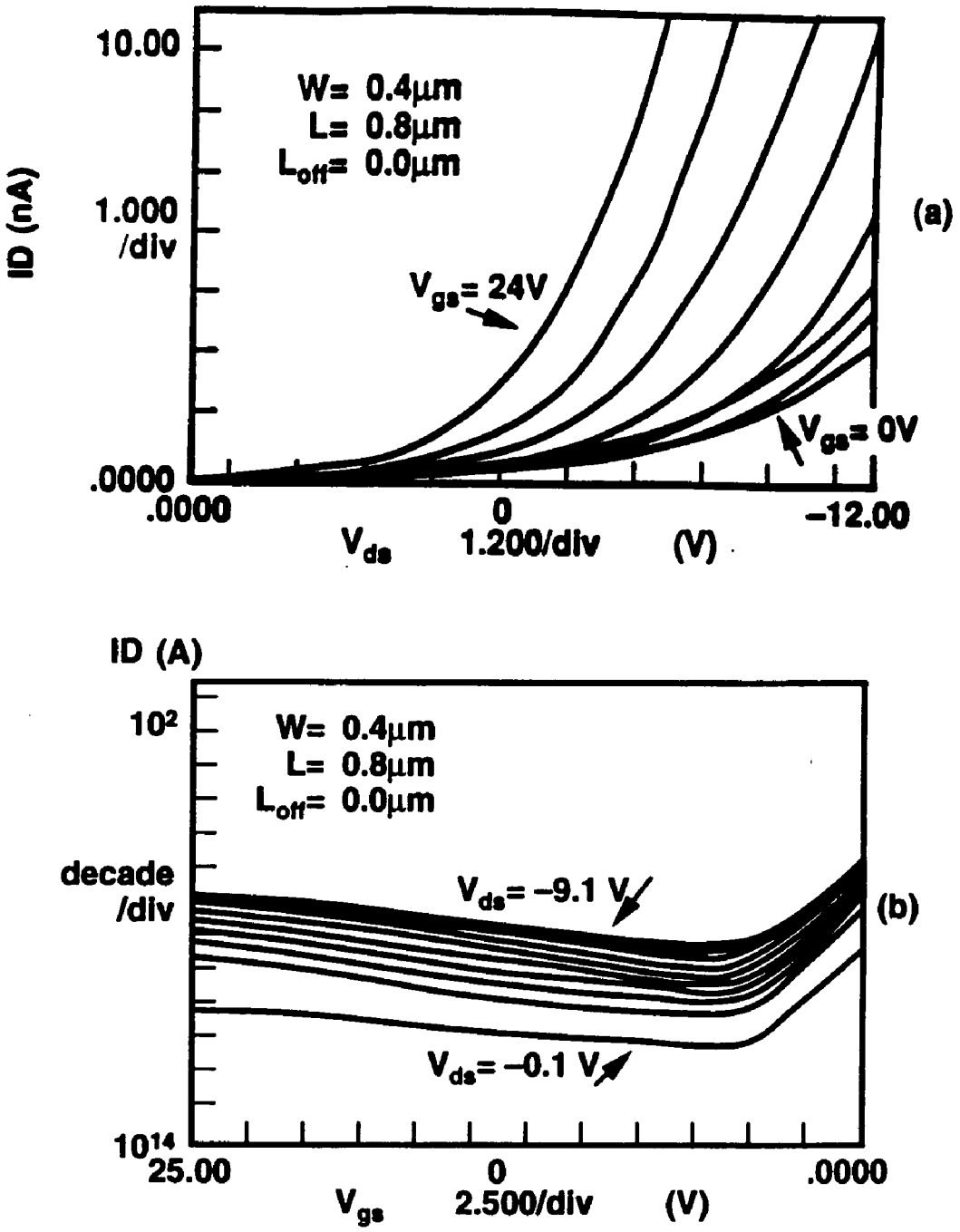


Figure 4-11. Leakage current as a function of (a) drain biases, and (b) gate biases (gate dielectric is 500Å thick).

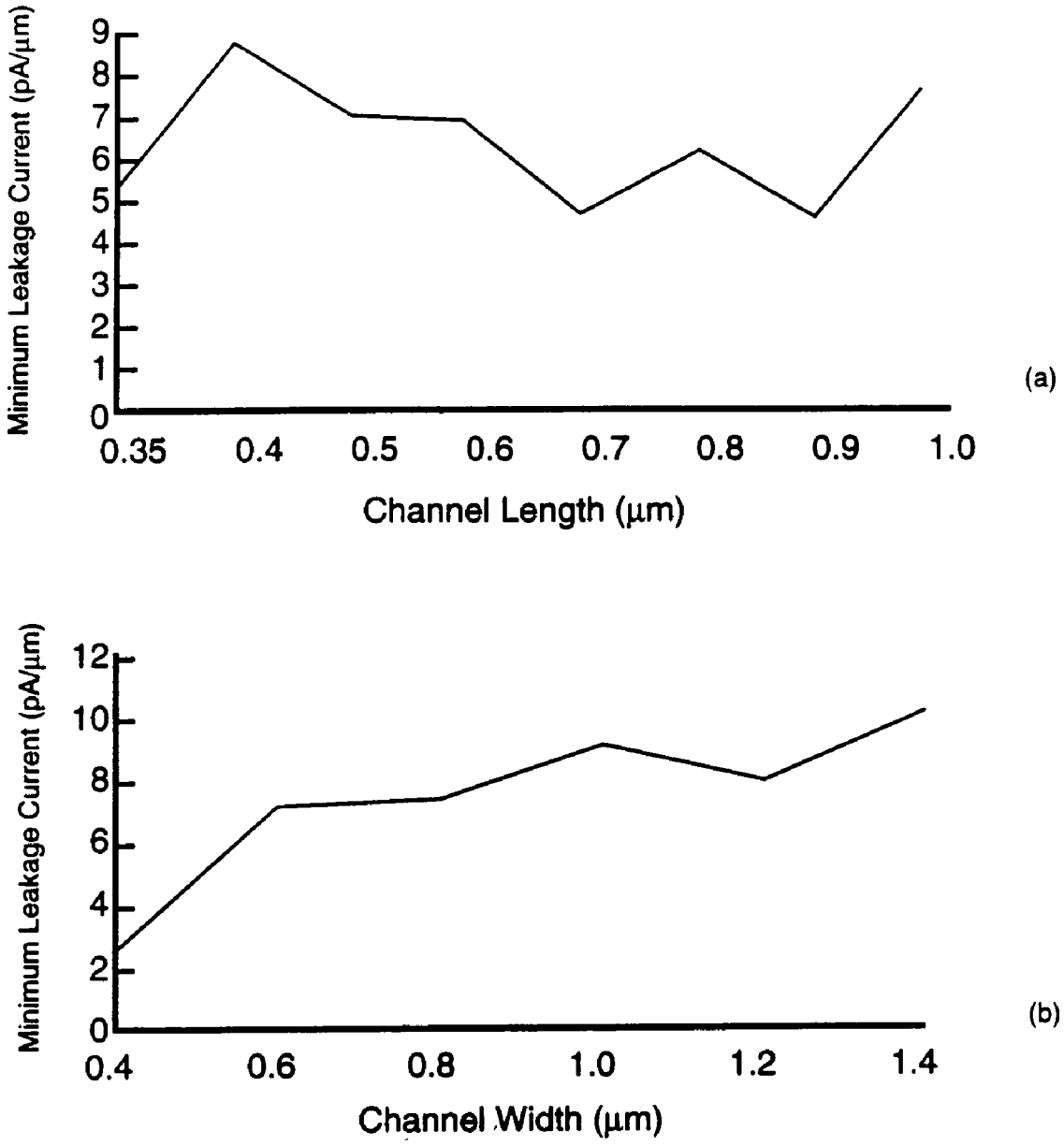


Figure 4-12. Minimum leakage (I_{off}) current as a function of (a) Channel length (W = 0.6 μm) and (b) Channel width (L = 0.8μm).

4.2.6 Drain current activation energy

The effects of carrier generation and recombination can be obtained by considering the trap levels that are active for conditions that aid rapid increases in leakage current. In the off state, there are fewer free carriers and the Fermi level in an undoped TFT channel is pinned at the grain boundary midgap states. The temperature dependence of the mobile holes in equilibrium with the trapped charge is given by:

$$I_{off} = I_o e^{-\frac{E_a}{kT}} \text{----------(4.3)}$$

Io = constant independent of temperature, and

Ea = drain current activation energy which measures the difference between the valence band edge and the energy of the grain boundary states within kT of the Fermi level.

The grain boundary states were assumed to be uniformly distributed about the midgap This allows small variations in Ea with gate voltage. At zero gate bias and low (-0.1 V) drain bias Ea is expected to be about half the band gap (Eg/2) and to

decrease steadily as gate bias is made more negative (P channel) and to increase slightly as the gate bias is made more positive (low leakage current). This is possible since in the off-state, the Fermi level will be swept to states within the trap normal distribution further away from valence band. But the Fermi level will be closer to the valence band in the on state. Therefore, measuring the drain current as a function of temperature, drain bias and gate bias yield the height of the potential barrier the carriers must overcome.

The activation energy (Ea) of the on and off current was obtained from the slope of Arrhnius plot of drain current in the On and Off state, respectively (figure 4.13). The data, which was taken over a temperature range from 25°C to 175°C, follow a straight line. This allows accurate determination of Ea. Figure 4.14 shows the plot of Ea as a function of gate bias for different drain voltages. For a low drain voltage, the activation energy has a value of about 0.56 eV and it drops to about 0.49eV at high Vg (6 V).

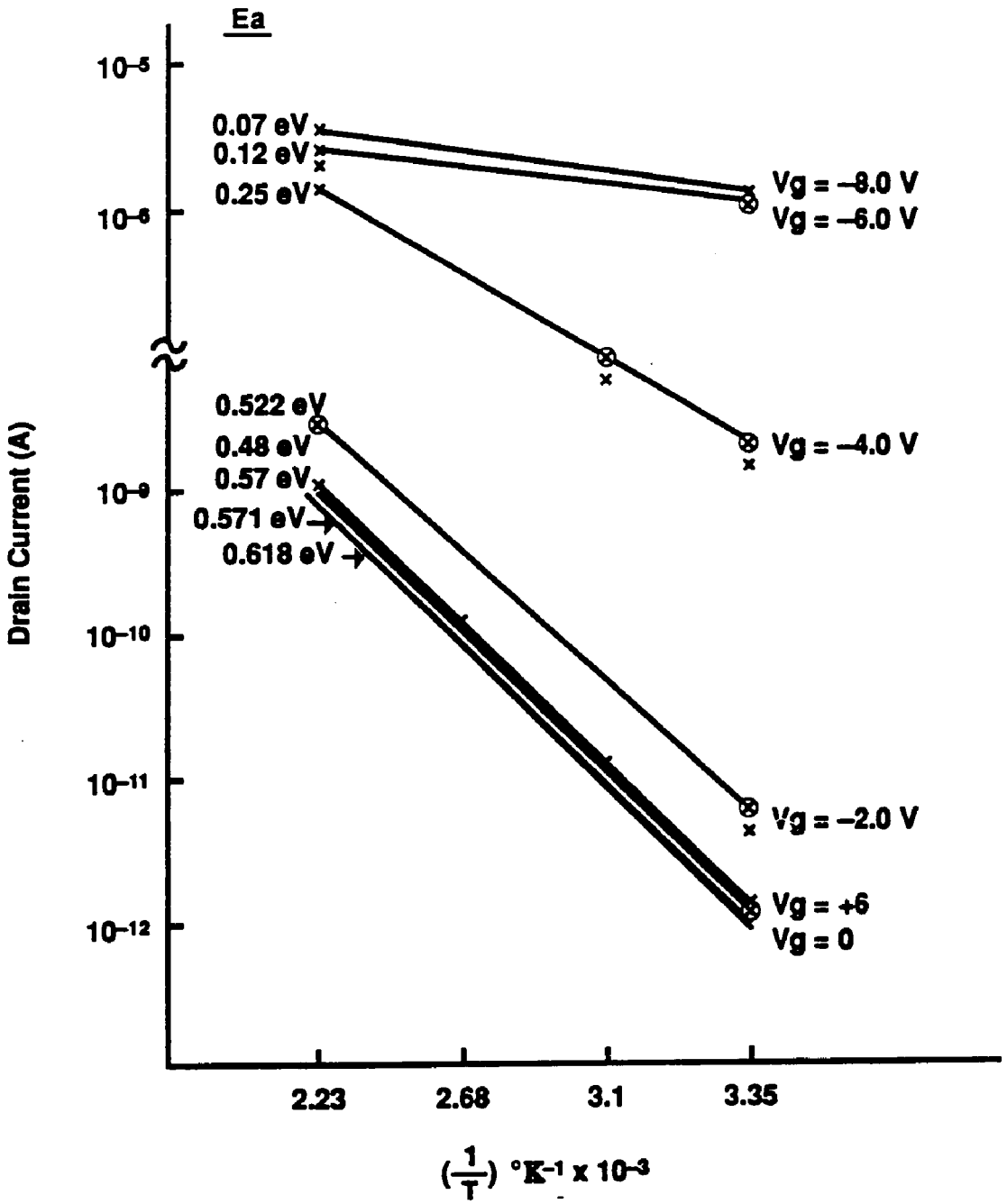


Figure 4-13. Arrhenius plot of the drain current of 1.0 μm p-channel device for different gate and drain voltages. The slope of each line defines the activation energy (Ea).

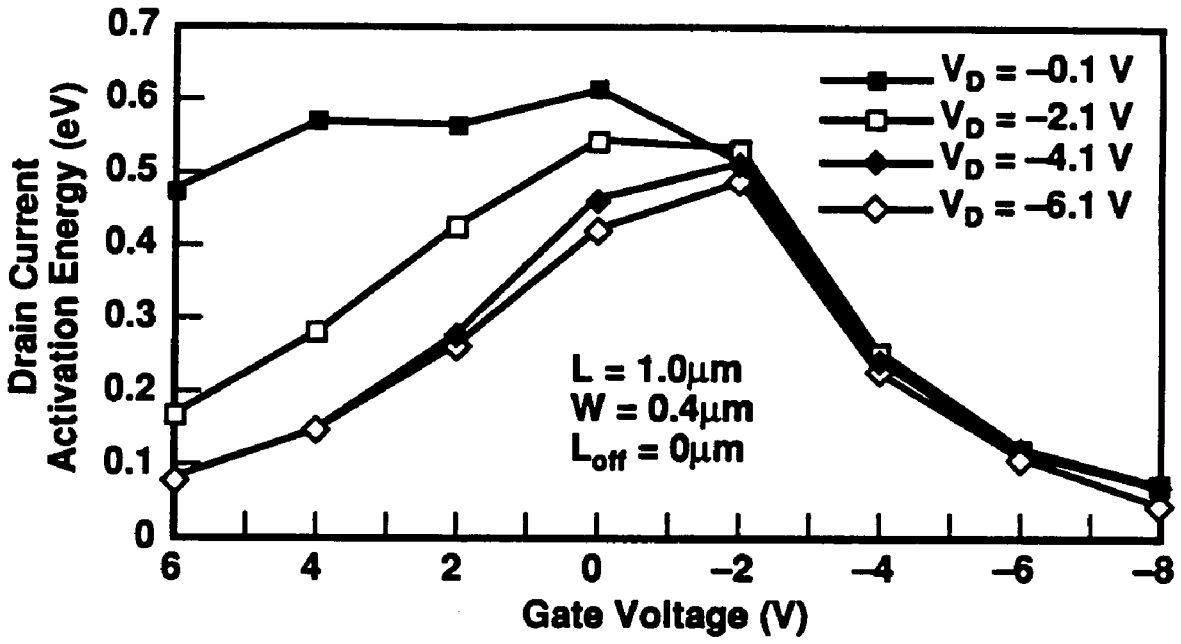


Figure 4-14. Dependency of activation energy on gate and drain voltages for 1.0 μm p-channel device.

For a constant gate bias (e.g. 0.0 V) in (figure 4.14), the activation energy decreases as the drain bias increases (more negative). When Ea decreases the carrier generation rate from the traps increases. This eventually results in the observed increase in off current as the drain bias increases.

As expected in the on state (negative Vgs), Ea decreases steadily as gate voltage decreases from 0 to -8.0 volts. The Ea curves nearly collapse to a single curve for all the drain voltage investigated. The decrease in Ea indicates that the Fermi level moves slowly towards the valence band as the traps are filled. Thus, to obtain an appreciable drive current from a polysilicon TFT, all traps closer to Si/SiO_2 interface (i.e. the channel surface) must first be filled. Interestingly, even at Vgs of -8.0 V, some unfilled traps are still present. The filling of the traps results in a gradual increase in on-current, which explains the broad subthreshold characteristics of the TFT obtained in this work.

In the off state of the device (Vgs = 0.0 volts), Ea decreases about 0.1eV for an increase of -2.0 volts in drain bias (see figure 4.14). As indicated in this figure, the activation energy decreases as the drain bias becomes more negative. Three different mechanisms responsible for leakage current are identifiable in figure 4.14. At a low drain field (-0.1 volts), the lowest activation energy is 0.48 eV. This indicate that for a carrier emitted from the trap to contribute to conduction process it must surmount 0.48 eV. Since the Ea is about Eg/2, thermionic emission is the dominant leakage mechanism at low field. This is the process step (1) in figure 4.15.

As the drain bias increases (more negative), the drain depletion field increases and Ea decreases (see figure 4.14). This suggest that the high field in the drain depletion region has reduced the barrier that carrier (hole or electron) must overcome. As such, the dominant leakage current mechanism is thermionic field emission and is represented by process (2) in figure 5.15. This process could be accomplished by combination of emission and tunneling processes. Further increase of the drain bias put Ea below 0.1 eV. Since Ea < 0.1 eV present almost no barrier to the carrier motion, the dominant leakage mechanism is pure tunneling. This is described by process (3) in figure 4.15.

As electrons from the valence band are captured by the traps via any of the three processes described (i.e thermionic emission, thermionic field emission, and tunneling), the hole generated are swept to the drain and they result in leakage current. For the trap to remain active, it must emit the captured electrons to the conduction band via similar process as shown in figure 4.15. This electrons accumulates in the channel, and they make the channel more negative with respect to the source (Note source is grounded). As a result, these electrons are attracted to the source where they recombine with holes supplied by the ground. This generation recombination process continues the cycle.

It must be emphasize that the most effective traps are located in the mid bandgap. Carrier capture and carrier emission is a two stages process as shown in figure 4.15. Tail state (tail (v) figure 4.15) traps located near the valence band can easily be filled. However it may never be emptied since energy electron must

overcome to be emitted into the conduction band is equivalent to bandgap energy. Similarly, tail state (tail(c)) close to the conduction band can easily be emptied. It will remain empty unless electrons are able to surmount approximately Eg energy to be capture from the valence band.

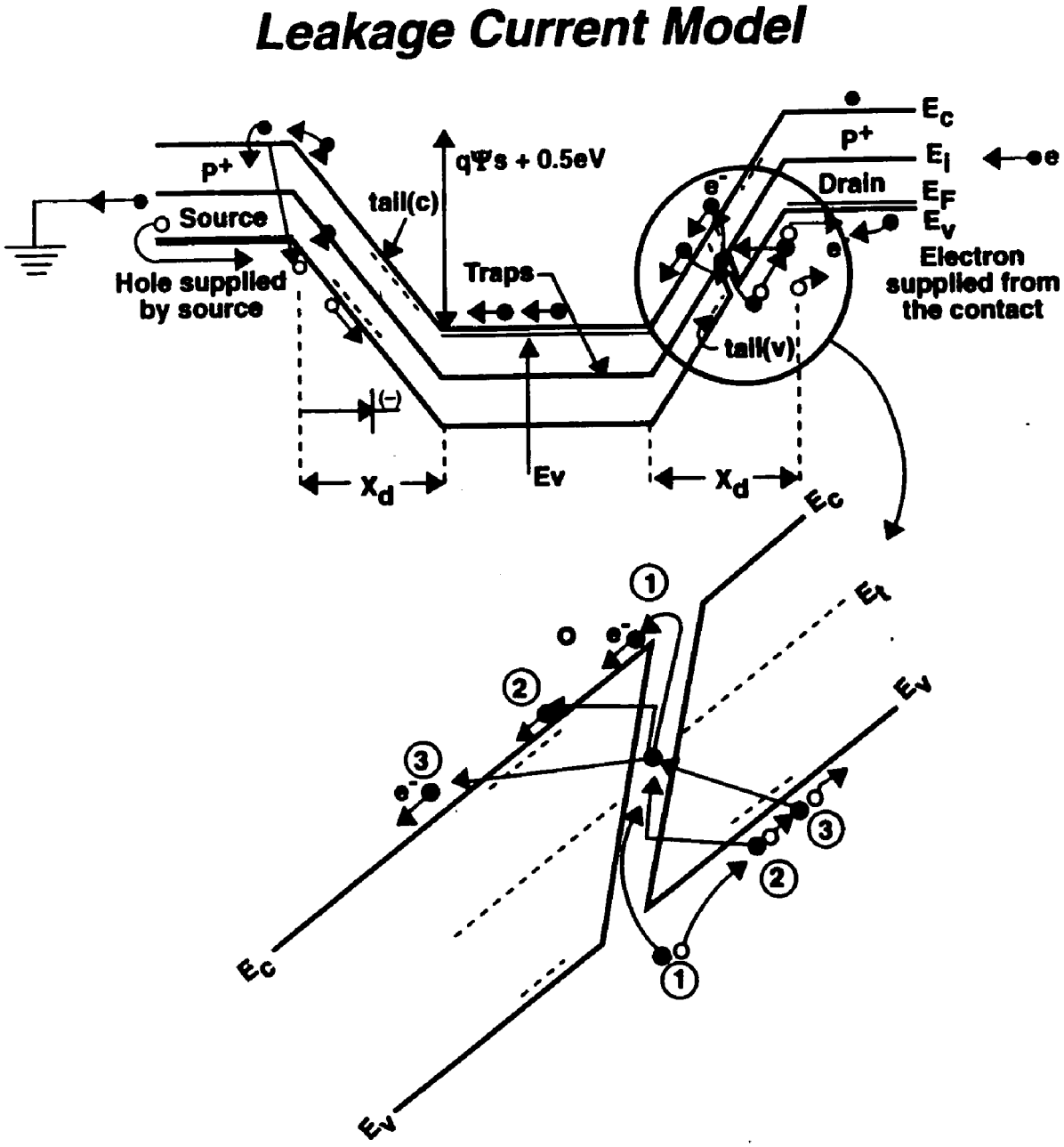


Figure 4-15. Schematic illustration of the leakage mechanism model in a sub-micron polysilicon TFT.

4.3 Effect of the drain offset

As previously mentioned the leakage current is a result of carrier emission and carrier tunneling from the trap sites due to a high electric field in the drain depletion region. If the electric field in the depletion region can be reduced, the carrier emission rate should decrease accordingly. The electric field in the drain depletion region can be reduced by moving the drain a distance 'L_{off}' away from the channel. L_{off} is the drain offset length. Since the offset region is not modulated by the gate, it is a highly resistive region that reduces the transverse as well as horizontal electric fields in the depletion region by reducing the effect of the externally applied drain bias on the channel. Additionally, the resistance of the offset region depends on the grain boundary potential barrier height. As such, the choice of offset length and the dopant implant dose determines the effectiveness of the drain offset region in reducing the leakage current without sacrificing the drive current. This section will present the effect of different drain offset lengths and dopant doses on TFT leakage and drive currents.

Figures 4.16 and 4.17 show the Ids-Vgs characteristics of a 0.8μm p-channel TFT with different drain offset lengths at -0.1 volts and -6.1 volts. At low drain bias, the leakage currents is low. The low field in the drain depletion region results in a lower carrier emission rate from the traps. Consequently, lower leakage current results. Because of the high electric field at the drain depletion region (-6.1 volts on the drain), the leakage current increases as the length of the

offset decreases. The changes in the drive and the leakage currents as a function of drain offset lengths are shown in figure 4.18 . As already indicated both the leakage and the drive currents increase as the drain offset length decreases. However, the leakage current saturates for drain offset lengths less than 0.3μm. This suggests that no further leakage reduction advantage could be derived for drain offset lengths less than 0.3μm.

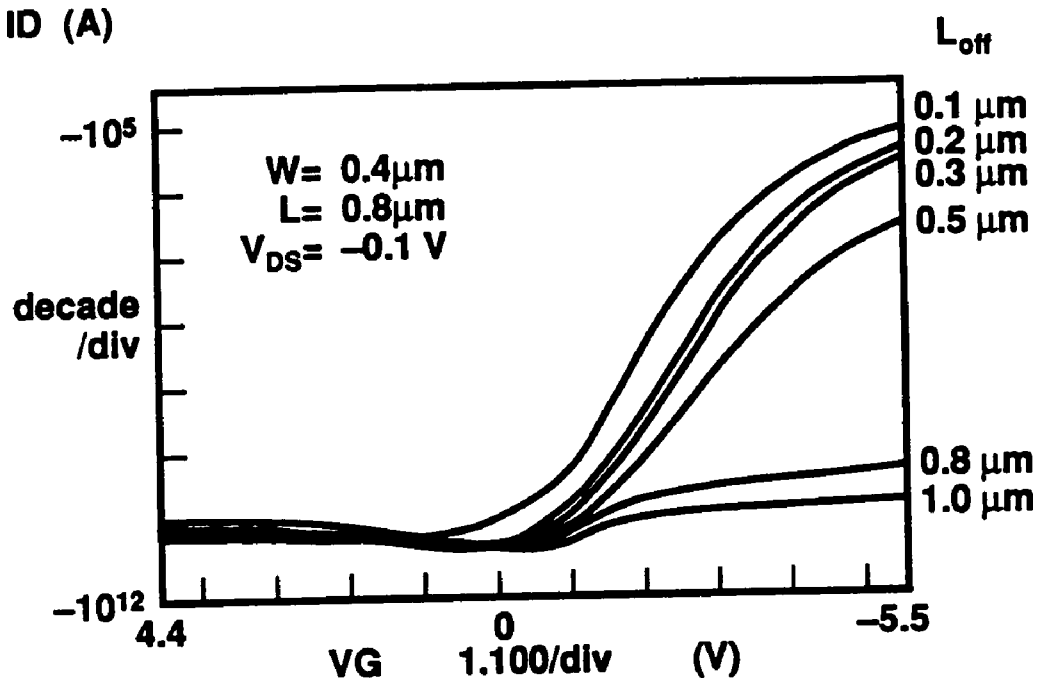


Figure 4-16. I_{ds} versus V_{gs} for different drain offset lengths for -0.1 volts drain bias (gate dielectric is 180Å).

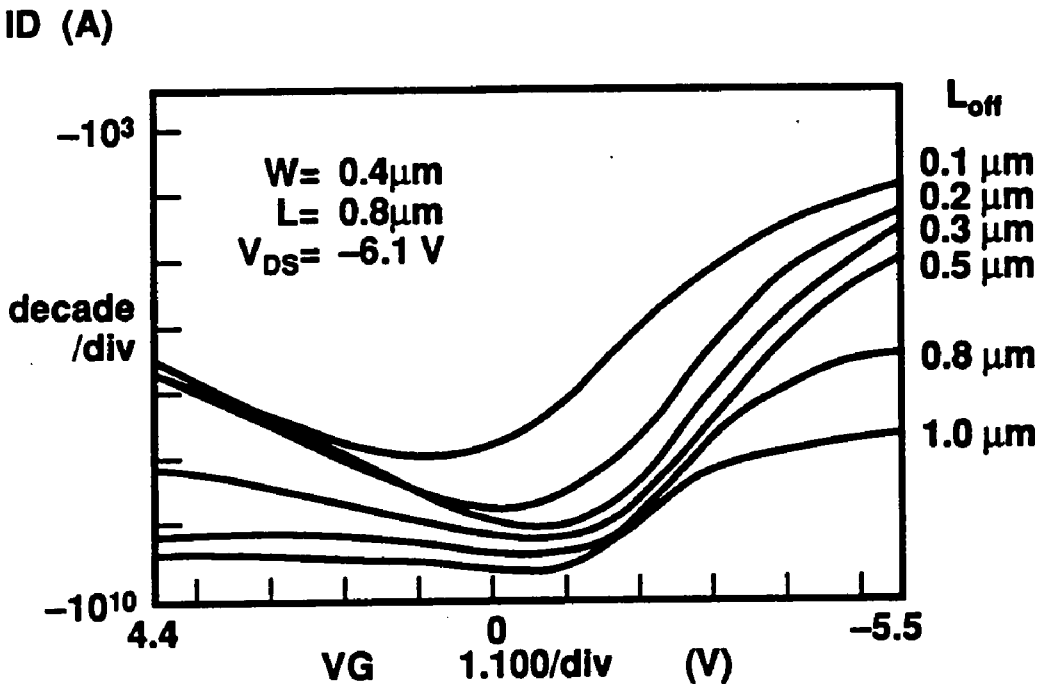


Figure 4-17. I_{ds} versus V_{gs} for different drain offset lengths for -6.1 volts drain bias (gate dielectric is 180Å)..

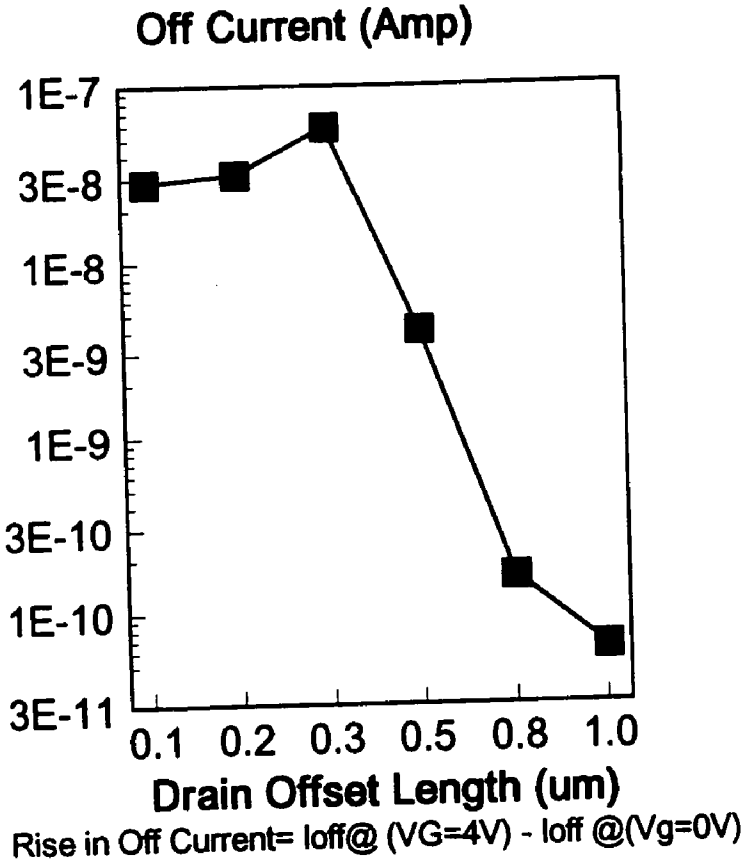


Figure 4-18. Changes in Off current as a function of drain offset lengths (gate dielectric is 180Å).

The resistance of the offset region increases, thereby decreasing the drive current, as the offset length increases. However, the resistance of the offset region can be reduced by doping the region[54] . As the dopant concentration in the drain offset region is increased, the drive current increases due to the reduction of the series resistance. The effect of dopant concentration on a TFT with a 0.35μm drain offset for several channel lengths is shown in figure 4.19. As indicated the drive (I_{on}) current increases as the dopant concentration in the offset region is increases from 1E12/cm^2 to 1E14/cm^2 due to the decrease in series resistance . Furthermore, the leakage (I_{off}) current decreases as well. A further increase of the offset region dopant concentration dosage to 3E14/cm^2 increases the leakage current without further improvement of the drive current. This suggest that the junction electric field is best balanced with a drain offset region dopant concentration $\leq$ 1E14 atom/ cm^2. A better understanding of the effect of the drain offset length can be obtained by studying the temperature dependency of the drain current as a function of drain voltage, gate voltage and drain offset length.

Figures 4.20 and 4.21 shows the drain current activation energy for a 0.8μm P-channel TFT device at drain biases of -0.1 volts and -6.1 volts, respectively. Three characteristics are identifiable in figure 4.20. In the off state, the activation energy is about 0.56 eV for all the L_{off}'s considered at V_{ds} = -0.1 volts. This indicates that the generation process is through thermionic emission from traps located at midgap. The other two characteristics are related to the 'On'

state, where the activation energy decreases gradually for $L_{off} \leq 0.5\mu m$ and remains at about midgap for $L_{off} > 0.5\mu m$. For $L_{off} > 0.5\mu m$, the series resistance of the offset region remains high such that most of the applied drain voltage is dropped within this region. Consequently, the drive current remains very low.

For a higher drain bias as shown in figure 4.17, the leakage current is appreciable for $L_{off} \leq 0.5\mu m$ due to the higher electric field in the drain depletion region. As revealed in this figure, the activation energy decreases as the gate bias becomes more positive. At 6.0 volts, for example, the barrier a carrier needs to overcome for a $0.1\mu m$ drain offset length is only 0.08eV while it is about 0.3eV for a $0.5\mu m$ drain offset length. Even at a higher drain bias, the activation energy remains very close to the midgap for $L_{off} > 0.5\mu m$ in the off state, and the Fermi level slowly moves towards the valence band in the on state.

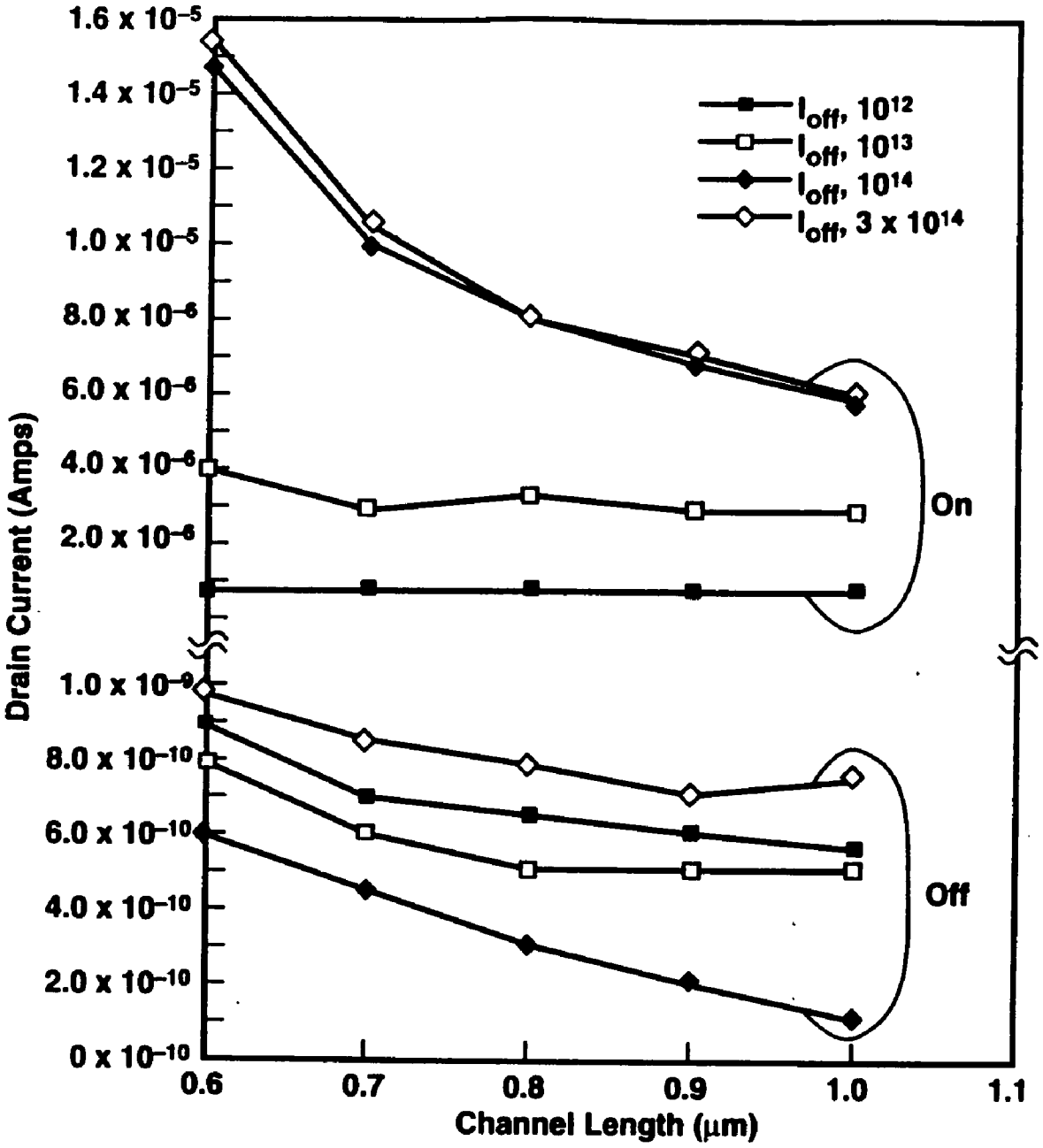


Figure 4-19. Drive current and leakage current as a function of drain offset implant dose (channel width is 0.6μm).

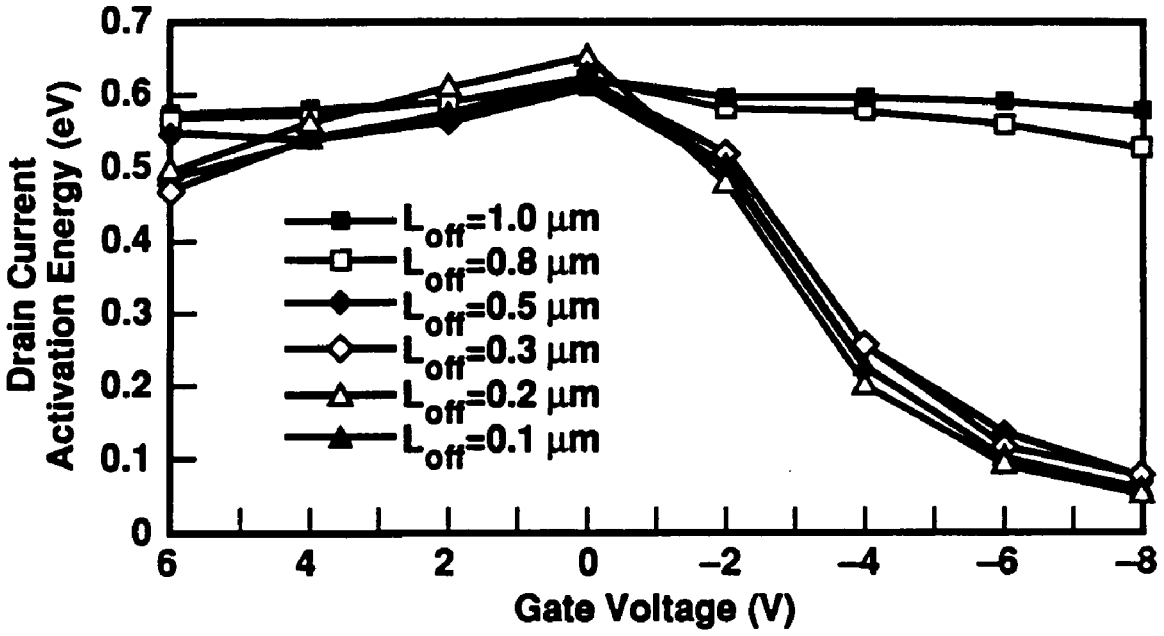


Figure 4-20. Drain current activation energy for 0.8μm p-channel inverted TFT for several drain offset lengths at -0.1 volts drain bias.

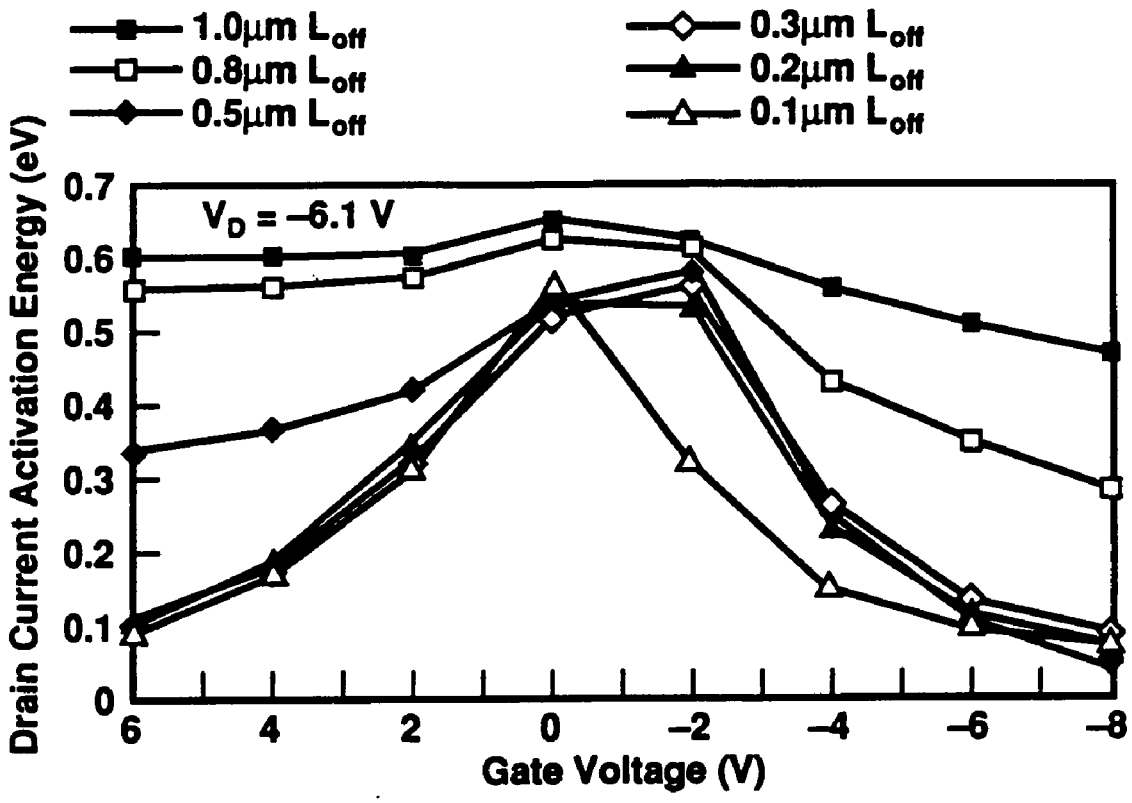


Figure 4-21. Drain current activation energy for 0.8μm p-channel inverted TFT for several drain offset lengths at -6.1 volts drain bias.

The leakage current model, using a p-channel device, is described as follows. As the gate voltage becomes more positive, the field in the drain space charge becomes higher. Electrons are captured by the active traps in the drain depletion region and thus holes are emitted into the valence band. Due to the high electric fields, these holes are quickly swept to the drain (see figure 4.15). The introduction of the drain offset reduces the electric field and it reduces the penetration of the drain depletion into the channel. As the drain offset length increases, the penetration of the depletion width (p+n of drain/channel junction) moves further away from the channel; thereby moving the peak electric field location away from the channel/drain junction. Although electrons accumulate in the channel, the reduction of the drain space charge field reduces the amount of carriers that reach the drain side. Consequently, the leakage current is reduced as the drain offset length increases.

An analytical expression and a model that describes both the drive and leakage current will be presented next.

Chapter 5 THEORETICAL ANALYSIS

5.1 Introduction

The operation of polysilicon TFT devices is similar to that of MOSFET devices. In an N-channel TFT, for example, a positive voltage on the gate will induce ($C_{ox}V_{gs}/q$) electrons in the polysilicon film. For a small value of applied gate bias, these electrons will be localized in the deep states of the polysilicon. When the applied bias is above the threshold voltage, some portion of the induced electrons will be mobile and the conductivity of the polysilicon will increase as the applied gate bias increases. The transistor will switch 'ON', and an electron current will flow from source to drain.

Although a polysilicon TFT is similar to the classical MOSFET, important differences exist between the two devices. This chapter will focus on the findings about submicron polysilicon TFTs and the differences between the TFT drain current and that of a classical MOSFET. The effect of the drain offset on the ON and OFF current and the mechanism responsible for the enhanced leakage current in the "off" state will be examined. The enhanced conduction in the "off" state will be shown to depend on carrier emission from the traps located in the drain space charge region. Both the analytical and physical model that will be presented in this chapter are based on P-type polysilicon TFT devices.

The chapter will begin with a qualitative description of a long channel MOSFET drain-to-source (I_{ds}) current equation. This equation will be used as a basis to compare similarities and differences between MOSFETs and TFTs. A model that accounts for short channel and drain offset effects on the polysilicon TFT drain current will be derived. It will be shown that the drain offset acts like resistance that tends to lower both the on and off current of a TFT. Next, the origin of the leakage current will be discussed. Emphasis will be place on giving both analytical and physical models to show that the leakage current is a result of carrier generation from the traps in the space charge region. Finally, it will be shown that at high electric fields, the leakage current can be explained with Poole-Frenkel band lowering and tunneling mechanisms.

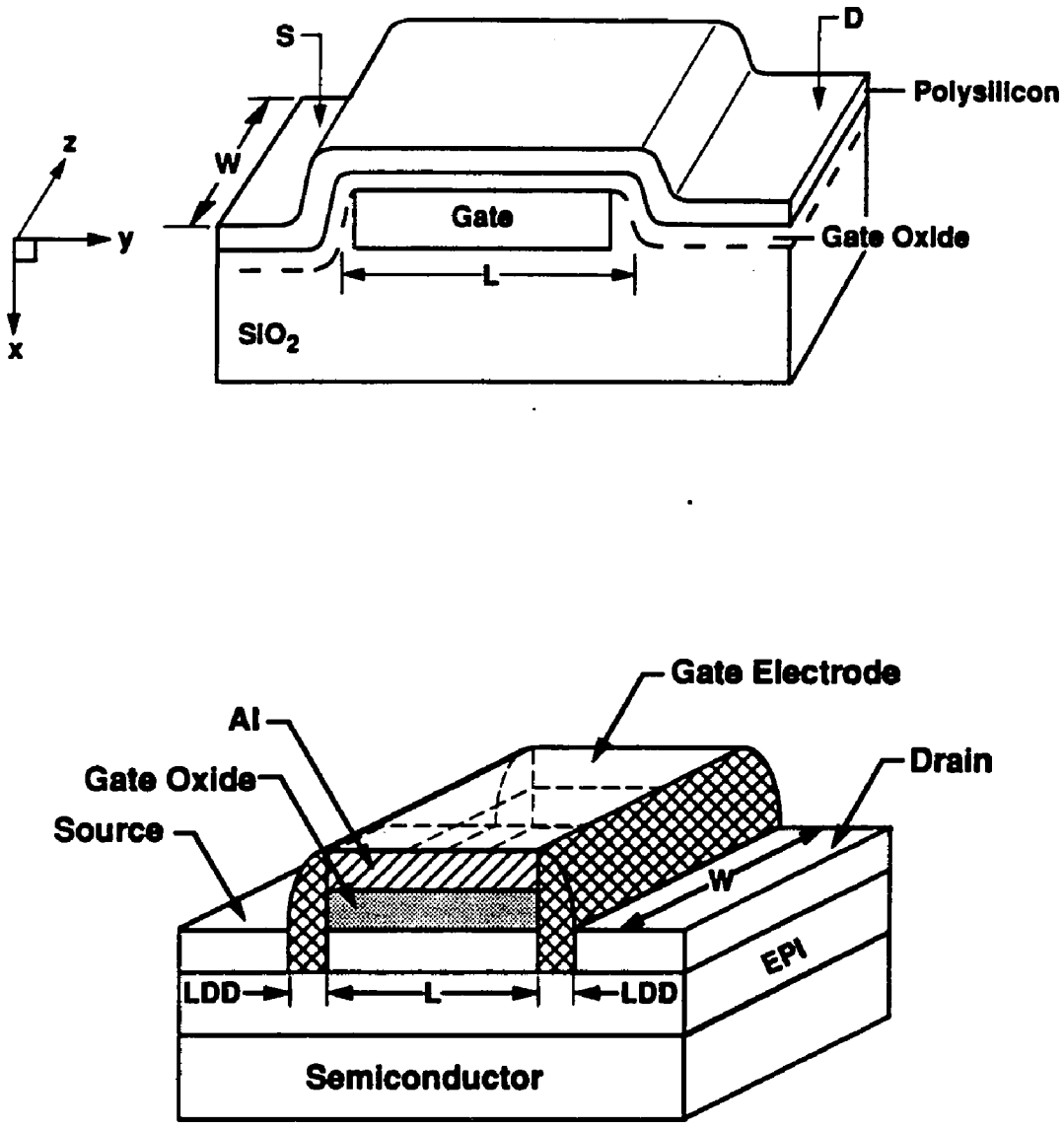


Figure 5-1. Schematic illustration of a cross-sectional view of (a) an inverted TFT and (b) a single crystal MOSFET.

5.2 Device structure and Operation

The cross-sectional view of a TFT is shown in figure 5.1(a). Unlike the single crystal MOSFET, figure 5.1(b), the entire device is on an insulating substrate and, therefore, has no substrate contact. This makes a TFT a three-terminal device instead of a four terminal device like a MOSFET. The three terminals (source, drain and gate) of a TFT are the same as those of the single crystal MOSFETs. The gate is formed by depositing and defining polysilicon on top of an insulator. This is followed by depositing a gate dielectric and lastly, depositing amorphous silicon, which is later crystallized to form the channel of the TFT devices. Unlike a TFT, the gate of a MOSFET is formed by depositing and defining polysilicon on the silicon dioxide grown by thermal oxidation of the substrate, and the channel is formed on single crystal substrate.

For both TFTs and MOSFETs, the source electrode usually serves as the reference voltage. In an enhancement P-MOSFET, for example, no drain current flows until the gate voltage reaches a critical value "Vt", called the threshold voltage. In this region of operation (termed subthreshold region), the source and drain are two oppositely placed "n-p+" junctions with small leakage currents through the drain junction, which is reversed biased. With sufficient voltage on the gate, enough holes are attracted under the gate from the contacts to locally invert the material from an 'n' to 'p' type to form the channel between the source and the drain. Depending on the value of drain voltage, the device can operate in the linear

or saturation modes. In the linear region of operation (|Vds| < |Vgs-Vt|), the device behaves like a gate-controlled variable resistor, and the drain current varies linearly with drain voltage. In the saturation region (|Vds| > |Vgs-Vt|), the drain current is independent of the drain voltage.

As indicated in figure 5.1(a), a TFT is similar in structure to a MOSFET except that the device is floating with no substrate contact. Like a MOSFET, an applied gate potential induces charge in the channel. However, the traps at the grain boundaries tends to create a barrier that impedes the flow of carriers from source to drain. As a result, the drain currents are lower, the subthreshold characteristics are more broad and the off-state leakage currents are higher than in a MOSFET. Unlike a MOSFET, the gate is more efficient[55] in generating carriers in the channel because the channel polysilicon is much thinner than the bulk silicon. Therefore, the gate of a TFT does not need to support the substrate charge. As an illustration, the vertical electric field as a function of depth is plotted for MOS and SOI devices in figure 5.2. In this figure one can see that the substrate charge increases as the channel-to-substrate potential increases, going from source to drain for a MOS device. An additional difference between a TFT and a MOSFET is the absence of substrate current[56] in the TFT. Since the floating device makes no contact to the substrate, it develops a positive bias with respect to the substrate, which reduces the threshold voltage and increases the drain-to-source current.

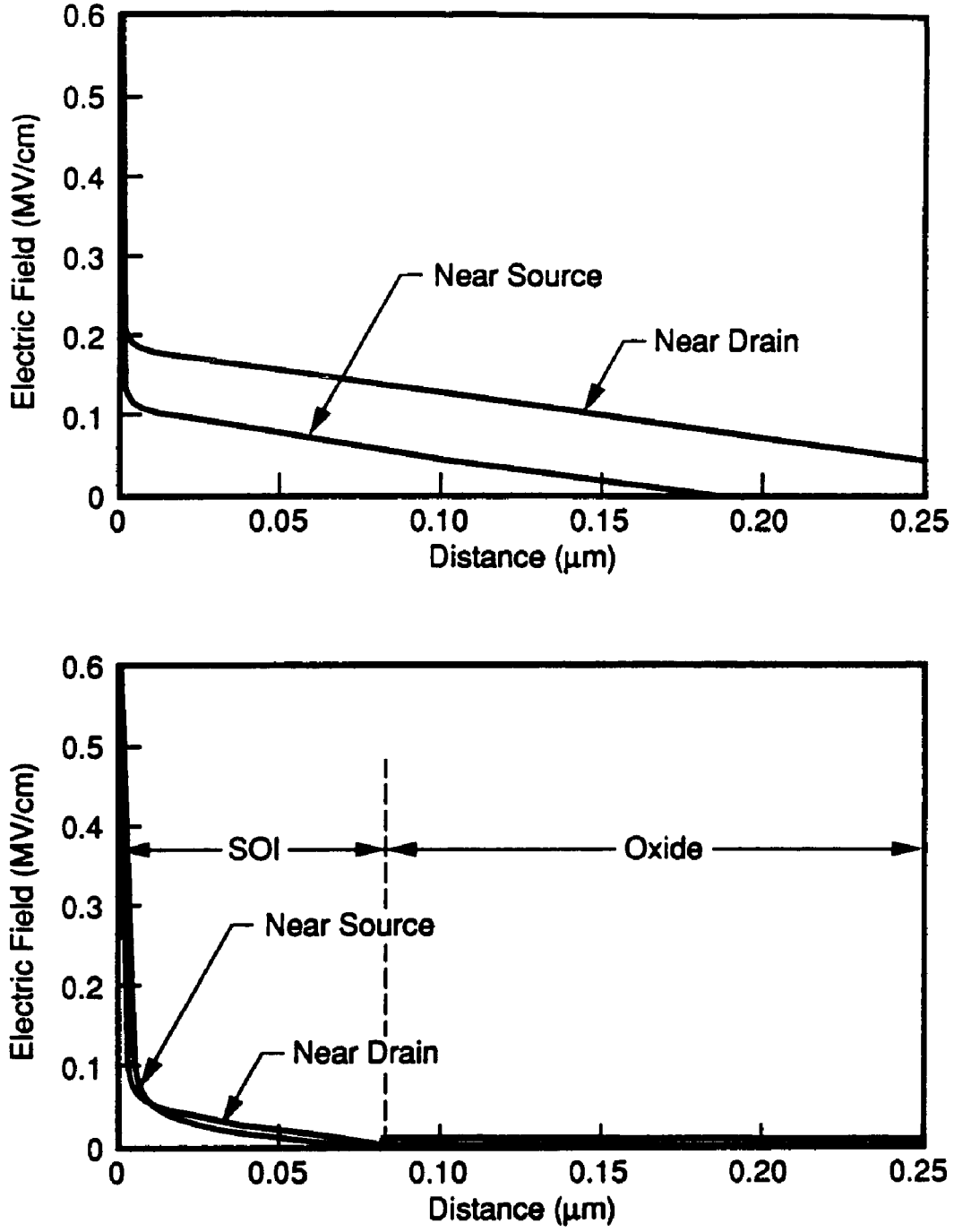


Figure 5-2. Vertical electric field as a function of depth near the source and drain of MOS and SOI devices[54] (VD = 2.5volts, VG-VT = 3.0 volts, gate oxide = 200Å, L=20 μm VS=VSUB=0 volts, and Ns = 4E16 /cm3).

5.3 Long channel MOSFET current equation

The derivation of a drain-to-source current equation will follow that presented by S. M. Sze[55] with the following assumptions:

(i) the channel doping is uniform,

(ii) the gate oxide and the substrate structure are an ideal MOS capacitor

(iii) the reverse leakage current is very small, and

(iv) The gradual channel approximation (transverse field larger than the longitudinal field) will be used.

For |Vg| > |Vt|, and |Vds| < |Vdsat| the current density is given by;

$$J_p = q\mu_p p\varepsilon - qD_p \nabla p \text{ ----------(5.1)}$$

where,

Jp = the hole current density,

μp = the hole mobility,

p = hole carrier concentration per volume,

ε = electric field,

Dp = hole diffusion constant, and

∇p = hole gradient .

The first term on the right of the equal sign is the drift component of the current while the second term is the diffusion component of the current. Within the conducting channel the current is flowing almost entirely in the y direction (figure 5.1). Because the hole concentration is approximately equal to the doping concentration (Na) or the trap density Nt, the diffusion component of the current density can be neglected. Equation 5.1 can be written as,

$$J_p = J_p(y) = q\mu(y)_p p\mathcal{E}(y) \text{----------(5.2)}$$

$$\mathcal{E}(y) = \frac{\partial \psi}{\partial y}$$

Jp(y) is the hole current density in the y direction, and $\mathcal{E}$(y) is the electric field in the y direction. The mobility and hole concentrations are all position dependent. In the absence of current sinks or additional current sources, the current flowing through any cross-sectional area of the channel is I_{ds}, where I_{ds} is given by :

$$I_{ds} = -\int\int J_p(y)dxdz = -W \int_0^{x(y)} J_p(y)dx \text{----------(5.3)}$$

$$I_{ds} = -\{Wq\int \mu_p(x,y)P(x,y)dx\}\frac{\partial\psi}{\partial y} \text{----------(5.4)}$$

$$= \{-W\frac{\partial\psi}{\partial y}\}\{-q \int_0^{x(y)} \mu_p(x,y)p(x,y)dx \text{----------(5.5)}$$

where

W is the channel width.

Equation 5.5 can be defined as the product of the channel total electronic charge and the effective mobility. Thus, the drain-to-source current can be written as:

$$\int_0^L I_{ds}dy = \{-W\partial\psi\}\{-q \int_0^{x(y)} \mu_p(x,y)p(x,y)dx \text{----------(5.6)}$$

$$I_{ds}L = W\mu_{eff} \int_0^{V_{ds}} Q_p(y)\partial\psi \text{----------(5.7)}$$

With the exception of $Q_p(y)$, all parameters in equation 5.7 are independent of position. Because the charge induced by the gate is balanced by the depletion region and $Q_p(y)$, the point-to-point variation of the depletion region that results when drain terminal is biased must be incorporated into the charge balance relationship. By considering the changes in the depletion width, Q_p can be expressed as a function of position along the channel as.

$$Q_p(y) = -C_{ox}\{V_{gs} - Vt - \psi(y)\} - \{2q \in_s N_D(\psi(y) + \phi_{si})\}^{\frac{1}{2}} - -(5.8)$$

where

C_{ox} = gate oxide capacitance per unit area,

$\in_s$ = dielectric constant of silicon,

N_D = number of donors per unit volume,

ϕ_{si} = built-in potential, and

$\psi(y)$ = potential along the channel.

The drain-to-source current for a long channel single-crystal MOSFET can be obtained by substituting equation 5.8 into equation 5.7 , performing the integration over the specified limit and dividing both sides of equation 5.7 by the channel length, 'L'.

$$I_{ds} = -[C_{ox}\mu_{eff}\frac{W}{L}\{(V_{gs} - Vts)V_{ds} - MZ\} \text{----------} (5.9)$$

$$Vts = \phi_{ms} - \phi_{si} + \frac{Q_{ox}}{C_{ox}} - \frac{V_{ds}}{2} \text{----------} (5.10)$$

$$M = \frac{2\sqrt{2q \in_s N_D}}{3C_{ox}} \text{----------} (5.11)$$

$$Z = (V_{ds} + \phi_{si})^{\frac{3}{2}} - \phi_{si}\frac{3}{2} \text{----------} (5.12)$$

5.4 Drain current model for submicron polysilicon TFT

The conduction mechanism in polysilicon is closely tied to the presence of the grain boundaries. As a result, the effect of the grain boundaries must be incorporated into the drain current equation of a polysilicon TFT . Additionally, the gate voltage of a TFT does not need to support as many donor charges in the conducting channel as in a single-crystal MOSFET. From equation 2.12, shown below, conductivity in polysilicon depends directly on the grain size, free carrier concentration and collection velocity. It also varies exponentially with grain boundary potential barrier and varies both exponentially and inversely with

temperature. Because the grain boundary potential barrier impedes carrier transport, the drain current of polysilicon TFTs are low.

$$\sigma = \frac{q^2 p v_c Lg}{kT} e^{-\frac{E_B}{kT}} \text{----------(5.13)}$$

As previously mentioned, the gate of a TFT does not support bulk charge. As such, the effect of the bulk charge in the drain current equation 5.9 can be omitted. The modified drain current equation for a small drain voltage in the direction of current flow is therefore:

$$I_{ds} = -[\frac{W}{L} C_{ox} \mu_{eff} \{V_{gs} - Vts) V_{ds}\}] \text{----------(5.14)}$$

where μ_{eff} is the effective mobility, which incorporates transport across the grain boundaries. Now, equation 5.13 can be substituted into equation 5.14 to obtain the TFT drain current at a low drain voltage.

$$I_{ds} = -[\frac{W}{L} C_{ox} \mu_a e^{-(\frac{E_B}{kT})} \{V_{gs} - Vt\} V_{ds}] \text{----------} (5.15)$$

$$\mu_a = \frac{q v_c Lg}{kT} \text{----------} (5.15a)$$

$$v_c = \sqrt{\frac{kT}{2\pi m^*}} \text{----------} (5.15b)$$

$$E_B = \frac{q^2 N_T^2 t}{8 \in_{si} (N_D t + N_{gi})} \text{----------} (5.15c)$$

$$N_{gi} = \frac{C_{ox} V_{gs}}{q} \text{----------} (5.15d)$$

where

m* = the hole effective mass,

Ngi = the gate induced charge concentration per unit area,

t = thickness of polysilicon film,

N_D = channel doping concentration,

Vt = threshold voltage, and

N_T = trap density per unit area.

The mobility has been expressed in terms of the grain boundaries potential barrier, and the barrier height is in turn expressed as a function of the applied gate voltage.

Thus, as the hole concentration increases in the channel the barrier height is continuously reduced or screened. If the induced charge in the channel is much larger than the product of the channel doping and the induced channel thickness (i.e Ngi >> N_{Dt}), then a modified expression for the drain current is obtained by substituting equation 5.15c into equation 5.15.

$$I_{ds} = -[\frac{W}{L} C_{ox} \mu_a (V_{gs} - Vt) V_{ds} e^{-\{\frac{q^3 N_T^2 t}{8 \in_{si} kTC_{ox}(V_{gs} - Vt)}\}}] - (5.16)$$

It must be emphasized that equation (5.16) does not hold when Ngi << N_{Dt}. Additionally, equation 5.16 predicts a linear relationship between ln(Ids) and (1/Vgs). As shown in figure 5.3, equation 5.16 does not hold at a low Vgs.

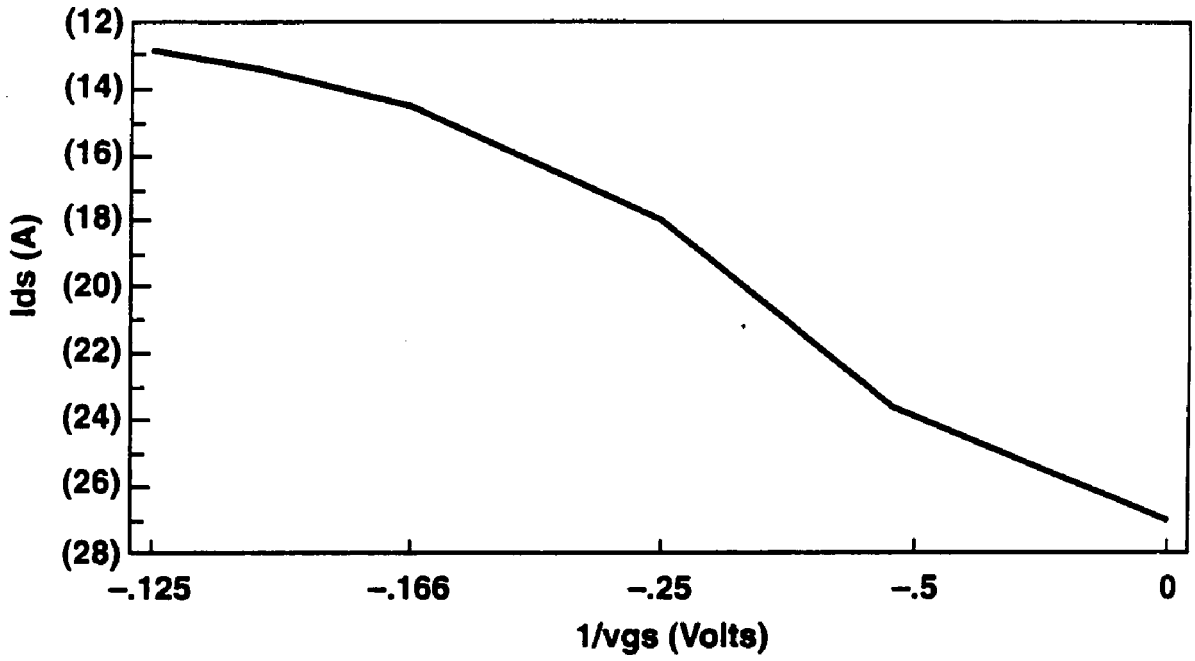


Figure 5-3. ln(Ids) as a function of (1/Vgs) showing failure of eq. 5.16 at low Vgs.

Equation 5.16 fails at low Vgs because of the inaccurate assumption that the channel thickness is equivalent to the film thickness[5]. In reality, the channel thickness is much smaller than the polysilicon film thickness. A better approximation of the drain current can be obtained by calculating the channel thickness (tch) from the solution of Poisson's equation for a trap-free intrinsic film.

$$\frac{\partial^2 \psi(x)}{\partial x^2} = \frac{\rho(x)}{\epsilon_s} \qquad (5.17)$$

where

$$\rho(x) = \rho_0 e^{(\frac{q\psi(x)}{kT})} \qquad (5.18)$$

where

$\psi(x)$ = potential,

ρ = charge density(C/cm^3), and

ϵ_s = relative permitivity of the material.

Equation 5.17 can be solved for $\psi(x)$ in the form:

$$\psi(x) = V_T \ln[\frac{S}{(x-M)^2}] \text{----------(5.19)}$$

where

$$V_T = \frac{kT}{q}$$

Substituting equations 5.19 and 5.18 into equation 5.17 and equating it to equation 5.19 and solving for the constant 'S', we obtain:

$$S = 2V_T \frac{\in_s}{\rho_0} \text{----------(5.20)}$$

From the condition that the total charge from the interface of the Si:SiO2 (x = 0) to a depth (x = ∞) must be equal to the charge on the gate, the constant M can be obtained to be:

$$M = \frac{-2V_T t_{ox}}{V_{gs}} \text{----------(5.21)}$$

where t_{ox} is the gate oxide thickness and V_{gs} is the gate voltage.

The charge (Q) from (x = 0) to any arbitrary depth 'd' is given by,

$$Q = \int_0^d \frac{S}{(x \in_{ox} - M \in_s)^2} dx \qquad (5.22)$$

$$= \int_0^d \frac{2V_T \in_{ox} V_{gs}}{xV_{gs}(\in_{ox} / \in_s) + 2V_T t_{ox}} dx \qquad (5.23)$$

$$= \frac{V_{gs} \in_{ox}}{t_{ox}} - \frac{2qkT \in_{ox} \in_s V_{gs}}{q^2 d \in_{ox} V_{gs} + 2kTt_{ox} \in_s} \qquad (5.24)$$

Due to the logarithmic decrease of channel potential, the gate-induced carrier channel thickness can be defined as the depth at which the charge in the channel incorporates 20% of the induced charge. Therefore the channel thickness is given by:

$$tch = d = \frac{2kTt_{ox}\sqrt{\frac{\epsilon_s}{\epsilon_{ox}}}}{q(V_{gs} - Vt)} \text{ ----------(5.25)}$$

By substituting equation 5.25 into equation 5.16, we obtain better agreement with experimental data, where ln(Ids) varies linearly with ($1/Vgs^2$) even at low gate voltage (figure 5.4).

This equation is:

$$I_{ds} = -\frac{W}{L}C_{ox}\mu_a(V_{gs} - Vt)V_{ds}e^{-\left\{\frac{q^3 N_T^2 t_{ox}\sqrt{\epsilon_{si}/\epsilon_{ox}}}{\epsilon_{si}\,4C_{ox}(V_{gs} - Vt)^2}\right\}} \text{ --(5.25a)}$$

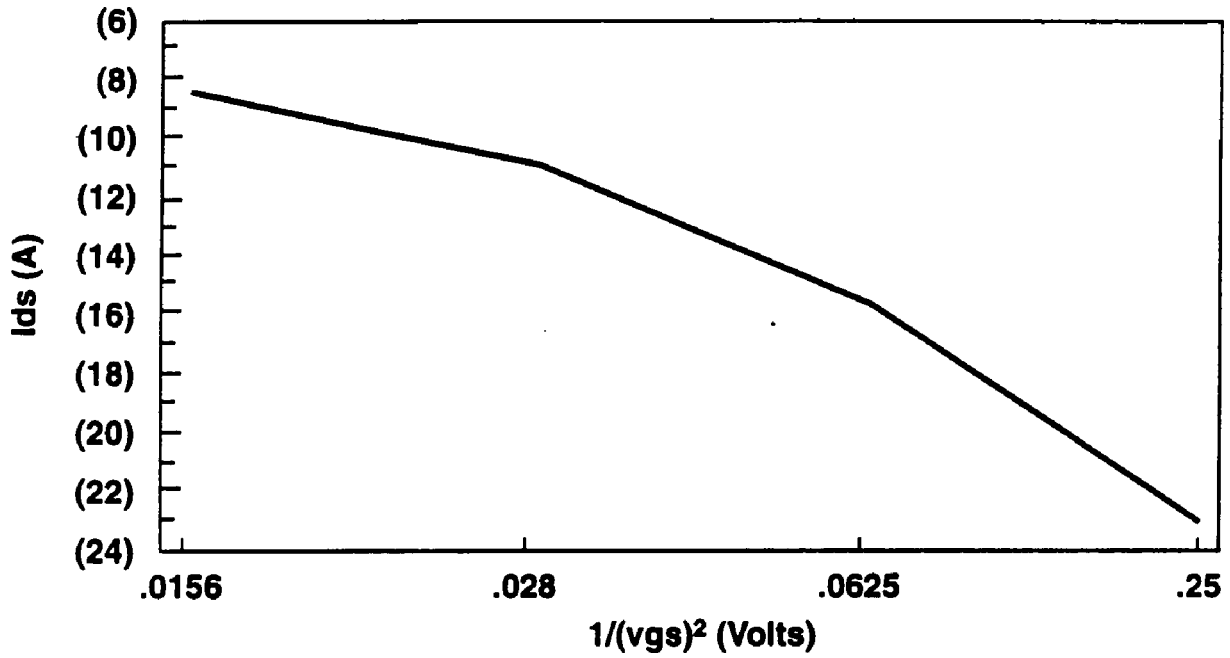


Figure 5-4. ln(Ids) vs. $(Vgs)^2$.

In submicron devices the threshold voltage varies with channel length (L), channel depletion width (xdm) and the junction depth (j). Therefore, the Vt in equation 5.16 must be expressed in terms of channel length, width and junction depth[57] [58] as:

$$Vt = Vts = Vfb + \phi_{si} + \frac{Q_B}{C_{ox}}\{1 - (\sqrt{1 + \frac{2xdm}{j}} - 1)\frac{j}{L}\} - - - - (5.26)$$

$$Vfb = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} - (5.27)$$

By substituting equations 5.26 into equation 5.25a, a complete expression for the drain current of a submicron TFT is obtained.

$$I_{ds} = -[\frac{W}{L}C_{ox}\mu_{eff}(V_{gs} - Vts)V_{ds}] - - - - - - - - - - - - - - (5.28)$$

where μeff and Vts are as previously defined. Equation 5.28 is a first order approximation of the drain current in a submicron TFT at a gate voltage where all

traps at the grain boundaries have been filled. Thus, the gate-induced charge in the channel is much larger than the charge trapped at the grain boundaries. Instead of using Vts, it is more appropriate to use the experimental flatband voltage 'Vfb'. Vfb is approximately equal to the gate voltage at which the induced charge equals the trapped charge. Equation 5.28 exhibits good agreement with experiment as indicated in figure 5.5. However, at Vgs $\leq$ -3.0 volts or when Vgs approaches Vt, equation 5.28 becomes unstable due to the Vgs-Vt term in the denominator of the exponential in equation 5.25a.

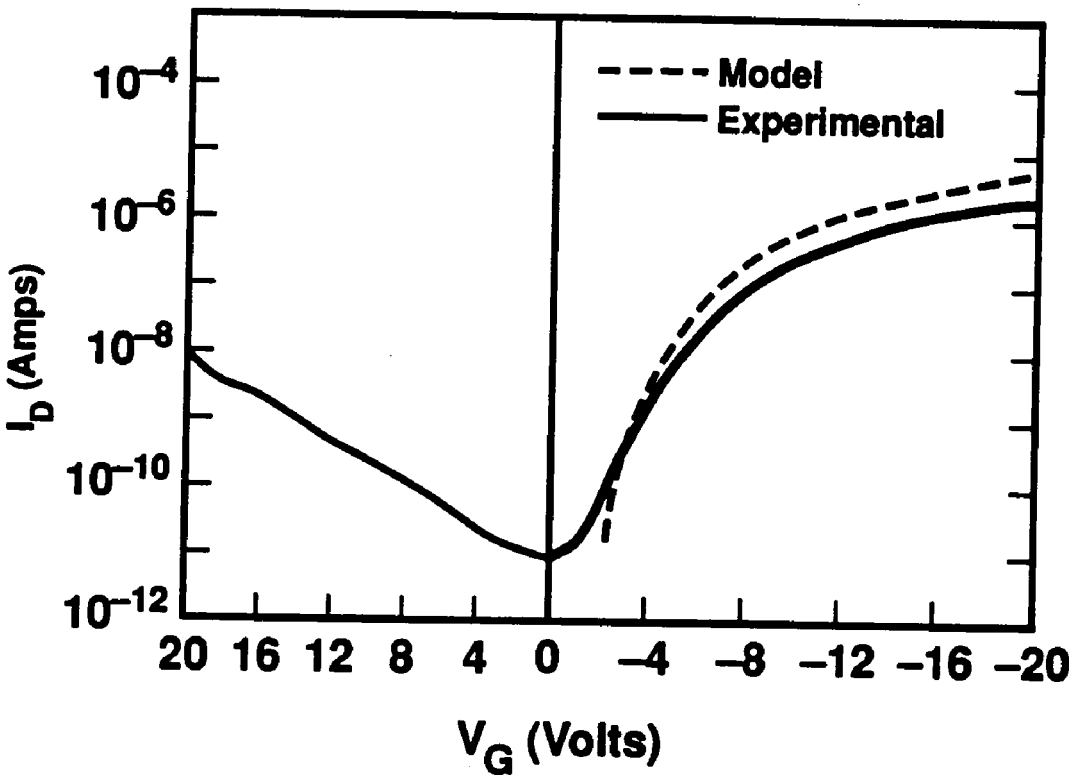


Figure 5-5. Log Ids as a function of gate voltage which compares the experimental result with the theoretical model. Experimental : L= 0.8μm, W = 0.6μm, Vds = -5.0 volts. Model: L=0.8μm, W = 0.6μm, Lg = 0.4μm, tox = 500Å Nt = 2E17 /cm^3.

5.5 Modeling the effect of the drain offset on I_{ds}

The drain offset region (figure 5.6) of a polysilicon TFT reduces the off-state current by lowering the field in the space charge region. Unfortunately, the offset region also behave like a parasitic series resistance that lowers the TFT drive current.

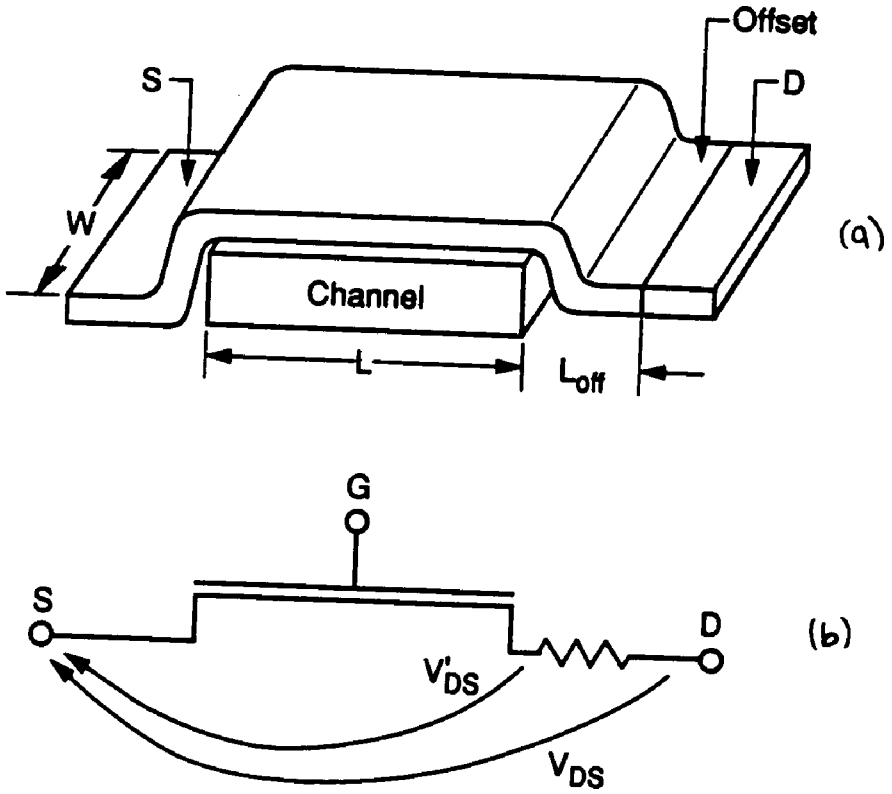


Figure 5-6. Schematic illustration of cross-sectional view of the drain offset in an inverted P-type polysilicon TFT.

Unlike the series resistance associated with a MOSFET source or drain, the resistance of the TFT drain offset is more complicated in that its value depends on several factors such as the length of the offset region, the doping concentration, the grain boundary and the grain boundaries defects. To model the effect of the drain offset on the TFT drain current, the following assumptions were made:

(i) the resistances associated with the source and drain are negligible compared to the drain offset resistance, and

(ii) although devices with drain and source offsets were fabricated, this model will concentrate on the drain offset region only.

The final result will be extended to include the source, drain and the case with a symmetrical offset structure. As indicated in figure 5.6b, some of the applied drain voltage is dropped across the offset region. Therefore, the "internal" or effective drain-to-source bias, V_{ds}', is given as;

$$V_{ds}' = V_{ds} - I_{ds} R_{off} \qquad (5.29)$$

where

V_{ds} = external drain bias and

R_{off} = drain offset resistance.

Substituting equation 5.29 into equation 5.28 and solving for the drain current, we get:

$$I_{ds} = \frac{-(W/L)C_{ox}\mu_a e^{-\frac{E_B}{kT}}}{(1+\alpha_0(V_{gs}-Vt)}\{V_{gs}-Vt\}V_{ds} \text{ ---------(5.30)}$$

$$\alpha_0 = \frac{C_{ox}R_{off}W\mu_a e^{-\frac{E_B}{kT}}}{L} \text{ ----------(5.31)}$$

$$R_{off} = \rho\frac{L_{off}}{W} = \frac{L_{off}}{W\sigma} \text{ ----------(5.32)}$$

$$\alpha_0 = C_{ox}\frac{L_{off}}{LW\sigma}\mu_a e^{-\frac{E_B}{kT}} \text{ ----------(5.33)}$$

where σ is given by equation 5.13.

As the length of the offset increases, α_0 increases and the value of drain current decreases as indicated in figure (4.17). For a long channel TFT device with a short drain offset length, the offset resistance becomes negligible compared to the channel resistance. As a result, the effect of drain offset on the drain current will be negligible when $L>>L_{off}$ Equation 5.30 exhibits good agreement with experimental data, as indicated in figure 5.7.

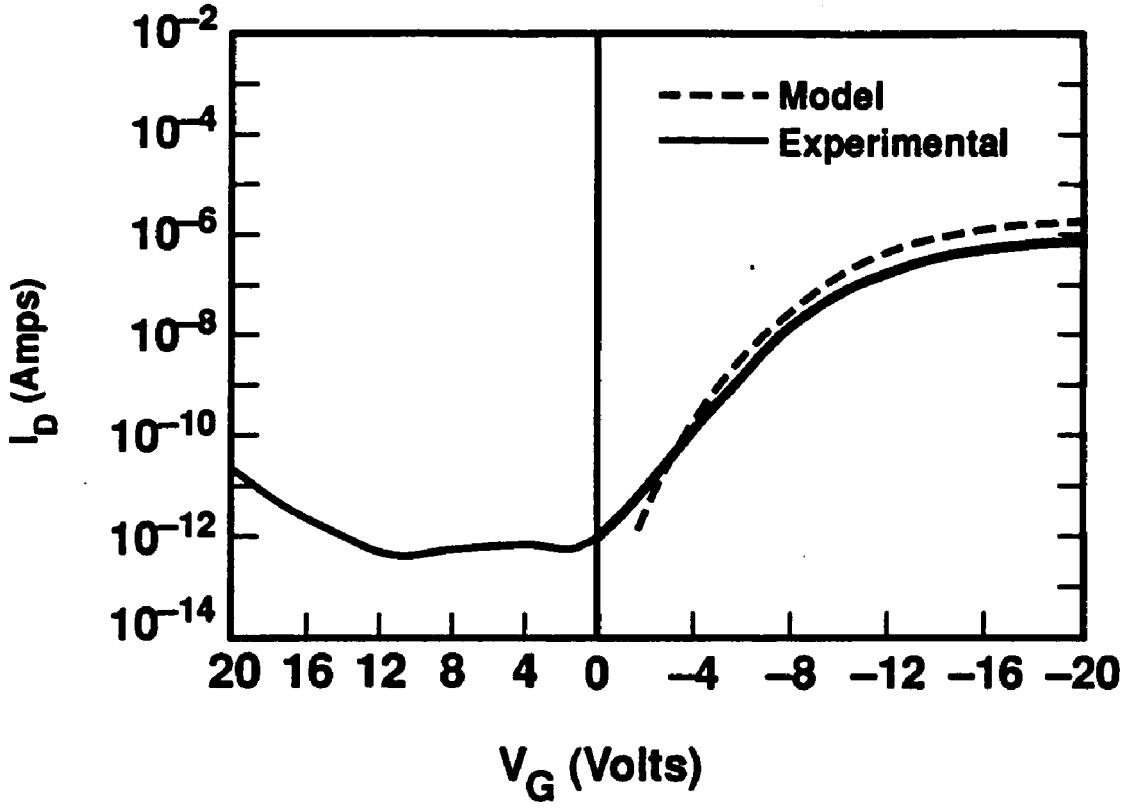


Figure 5-7. Log (Ids) vs Vgs which compares the experimental data with the analytical model. Experimental : L= 0.8μm, W = 0.6μm, Vds = -5.0 volts, Off = 0.35μm . Model: L=0.8μm, W = 0.6μm, Off = 0.35μm, Lg = 0.4μm, tox = 500Å Nt = 2E17 /cm^3.

In order to include the effect of the source and drain contact resistances and the symmetrical offsets, the R_{off} factor in the previous equation can be change to $2(R+R_{off})$. The factor of 2 accounts for these resistances on either side of the channel.

5.6 Drain current activation energy

The overall performance of the device characteristics can be deduced from the activation energy data as a function of gate voltage from the on to the off state. As previously mentioned in chapter 4, submicron polysilicon TFTs with n+ polysilicon gates were fabricated with various drain offset lengths. The activation energy was measured at a drain voltage of -0.1 volts in order to prevent large potential drops across the offset region and the source and drain regions. This precaution prevents potential variations across the channel. The drain current was measured at different temperatures (0°C → 175°C) and gate voltages (0 volts → -8 volts). The activation energy (Ea), figure 5.9, at each gate voltage for each drain offset length was obtained from the slope of the straight line of ln(Ids) versus (1/T), as shown in figure 5.8 or figure 4.13 for drain bias of -0.1 volts.

The plot of Ea versus gate voltage (Vg) for a 0.8μm inverted P-channel TFT with 180Å gate oxide and drain offset lengths ranging from 1.0μm to 0.1μm is shown in figure 5.9. For drain offset lengths ranging from 0.5μm to 0.1μm, the drain current activation energy decreases very slowly with gate voltage,

suggesting that the Fermi level moves slowly towards the valence band as the gate bias becomes more negative. This implies that there are trap states that are continuously being filled as the Fermi level moves towards the valence band, which suggests an existence of band tail states[60]. It is interesting to note that the added parasitic series resistance from the drain offset is very high for offset lengths longer than 0.5μm. In this case the Fermi level in the offset region is still located at mid-gap. Figure 5.10 shows the drain current of devices with longer offset length exhibiting resistive characterics since the offset region limits the device current.

An analytical expression for the on state drain current activation energy can be obtained by solving the one dimensional Poisson's equation for the surface potential[61] with the following assumptions:

i)the band tail states are evenly distributed throughout the film,

ii) the Fermi level is at the middle of the band gap and can be approximated by a step function, and

iii) only the exponential tail will be considered, with the zero energy level being at the valence band.

Figure 5.11 shows a schematic diagram of a TFT under the influence of a gate potential.

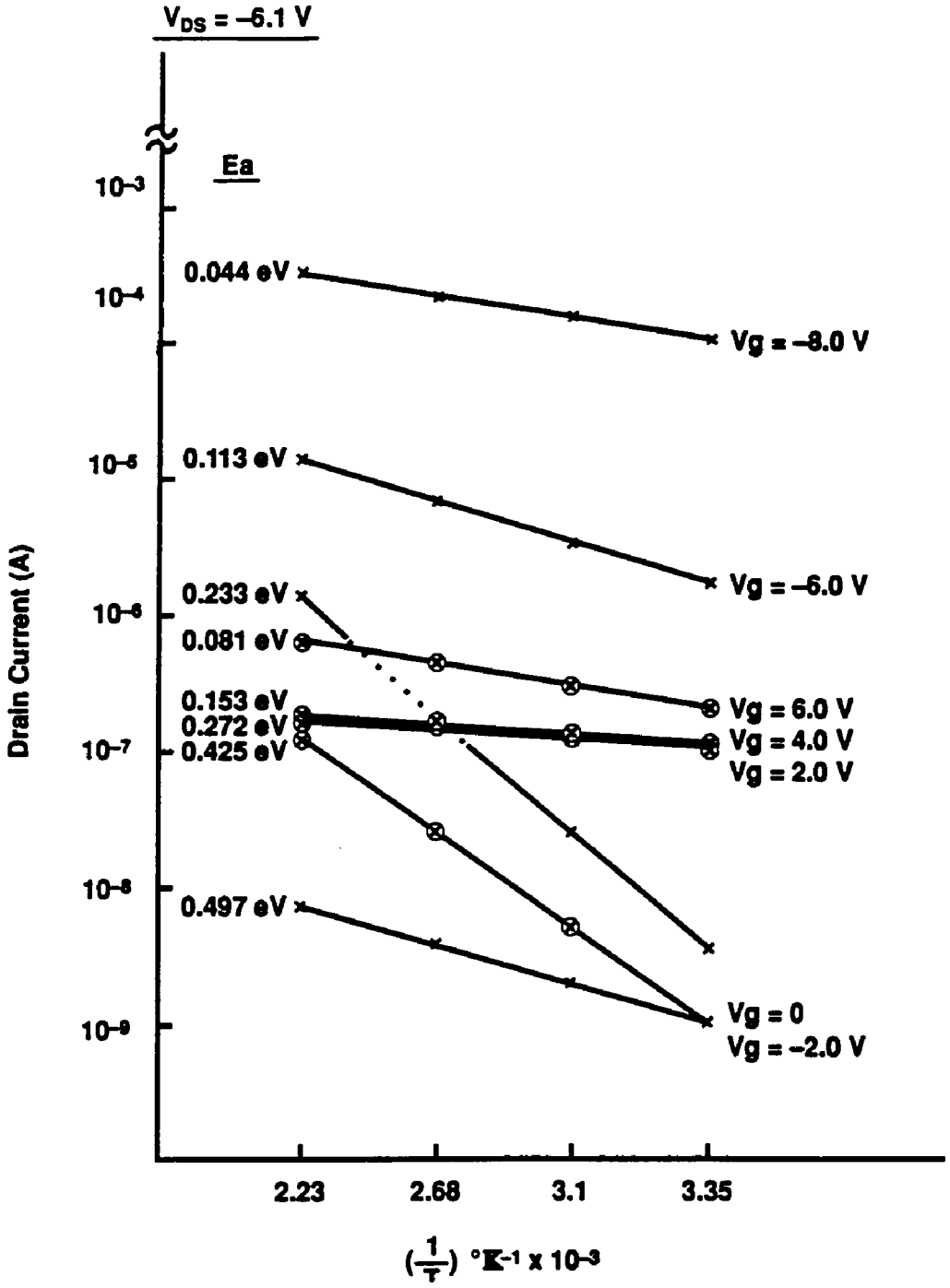


Figure 5-8. ln(Ids) versus (1/T) used to obtain the drain current activation energy.

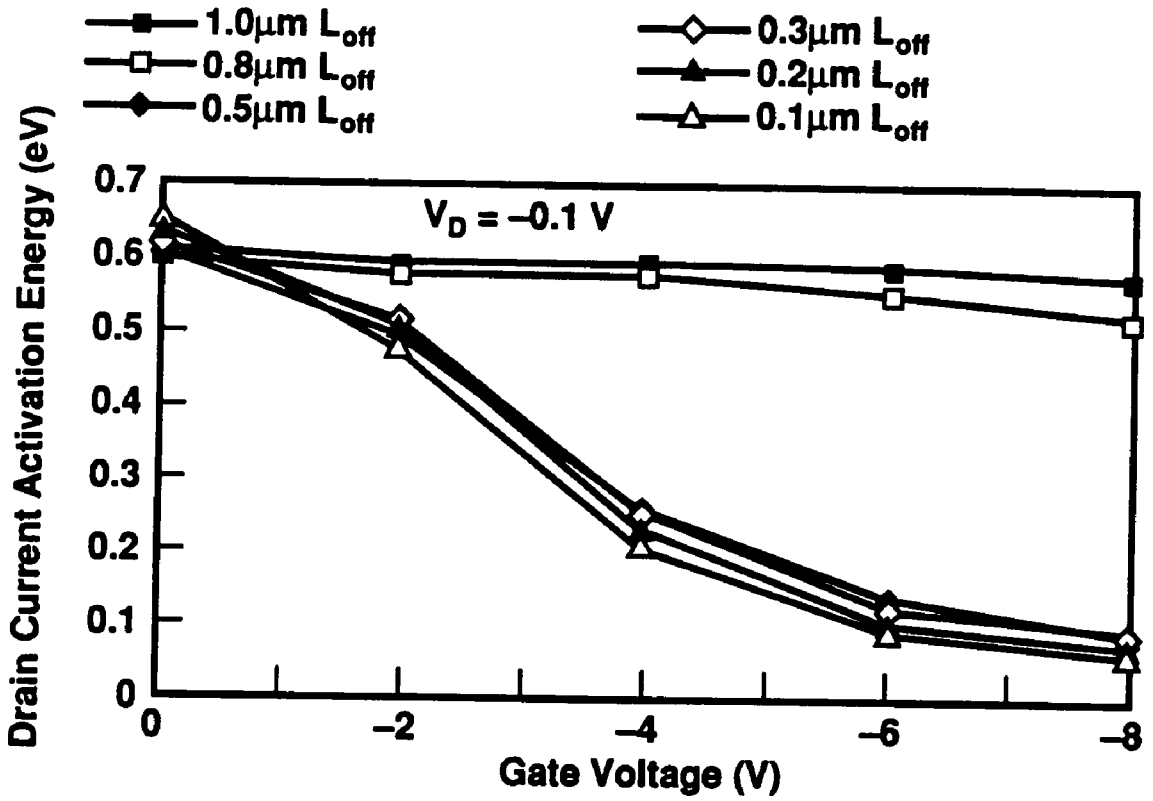


Figure 5-9. Activation energy versus gate voltage for various drain offset lengths.

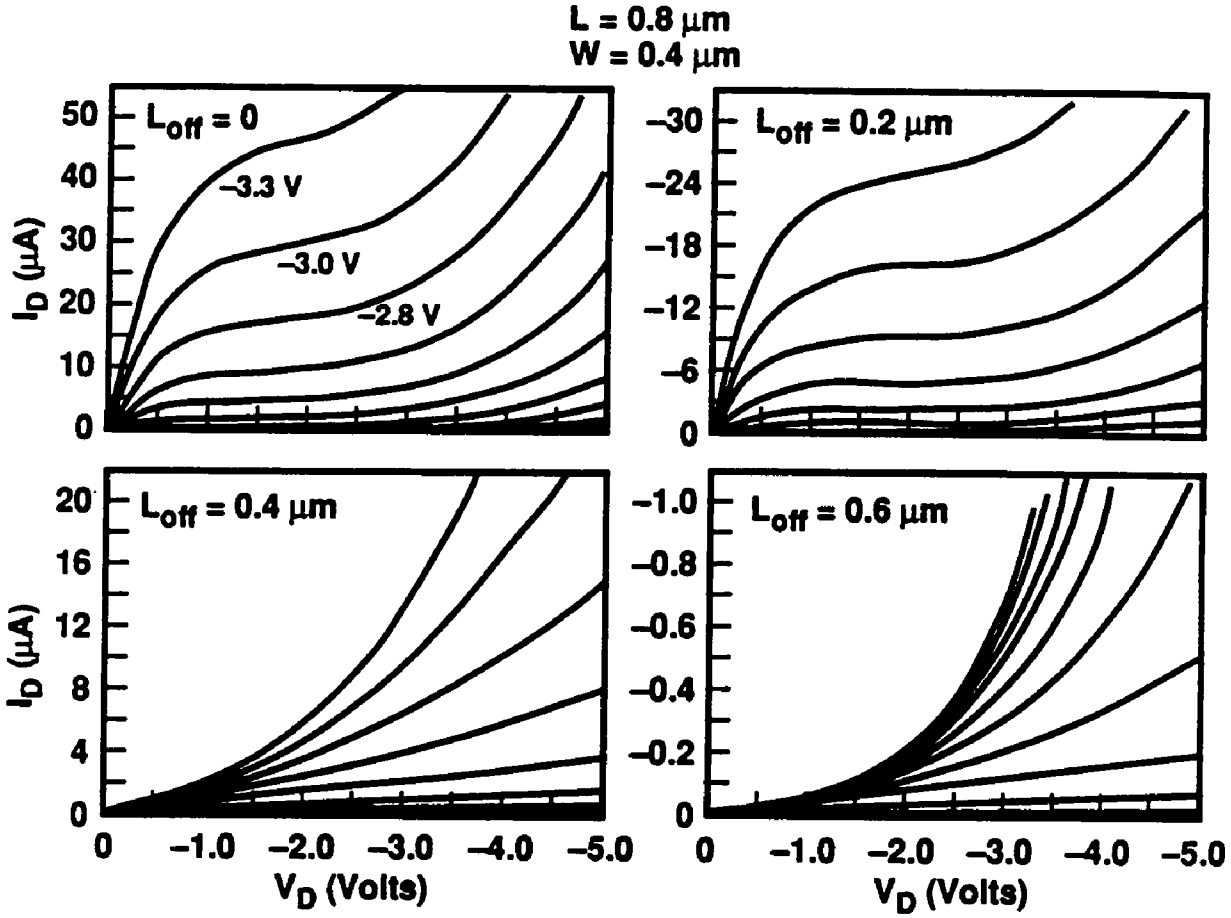


Figure 5-10. Drain current versus drain voltage showing a device with longer drain offset exhibiting resistive characteristics.

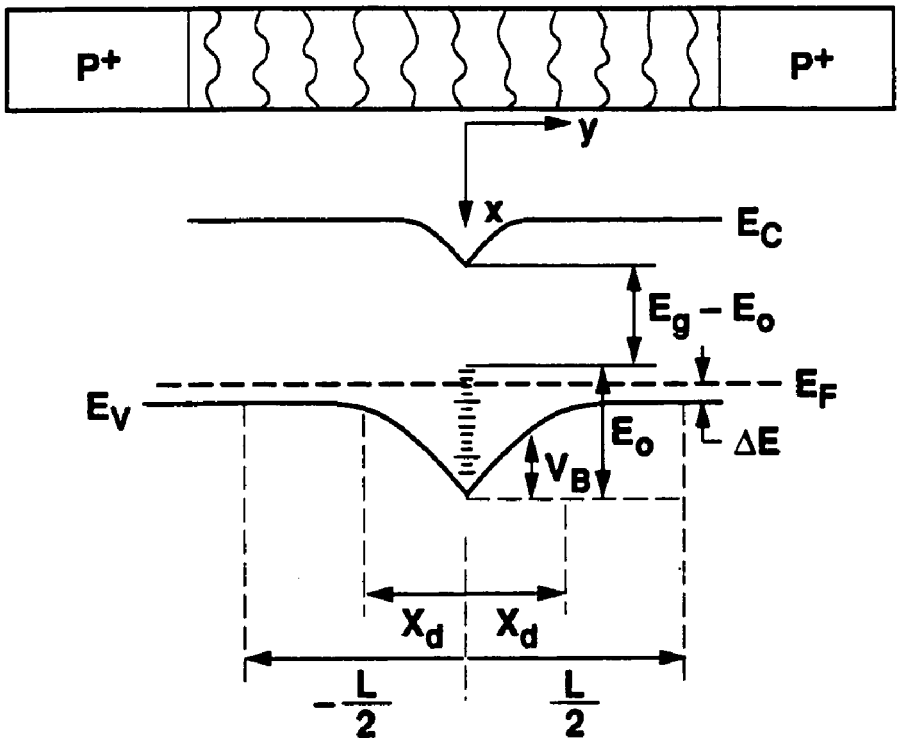


Figure 5-11. Schematic diagram of a TFT under the influence of gate potential[61].

If the band tail density is given by equation 5.34, where kT measures the spread of the band tail towards the intrinsic Fermi level,

$$g(\in) = Ne^{-\in/kT} \text{----------(5.34)}$$

With equation 5.34 the trap charge Qt can be estimated to be:

$$Qt = \int_{\frac{Eg}{2}+q\psi(x)}^{\frac{Eg}{2}} g(\in)d \in \text{----------(5.35)}$$

$$= kTN \in \{e^{-\frac{1}{2kT}(2q)}\} \text{----------(5.36)}$$

The surface potential can be obtained from a solution of the one dimensional Poisson's equation 5.35.

When kT >> -qψ, equation 5.37 can be approximated by:

$$\frac{\partial \psi}{\partial x^2} = -\frac{qQt}{\epsilon_s} = \Omega(1 - e^{-\alpha\psi}) \text{----------(5.37)}$$

where

$$\Omega = \frac{qNkT}{\epsilon_s} e^{-\frac{Eg}{2kT}} \text{----------(5.38)}$$

and

$$\alpha = \frac{q}{kT} \text{----------(5.39)}$$

where kT>> -qΨ, equation 5.37 can be approximated by:

$$\frac{\partial^2 \psi}{\partial x^2} = \sqrt{\frac{q\Omega}{kT}}\psi = a\psi \text{----------(5.40)}$$

The solution to equation 5.40 is of the form:

$$\psi = Ke^{-x(\sqrt{\frac{q\Omega}{kT}})} \text{----------(5.41)}$$

where K is a constant. The surface potential can be obtained by solving for K in equation 5.41 and by applying the condition of equation 5.42.

$$Vgs = \frac{\epsilon_s}{\epsilon_{ox}} t_{ox} + \psi(x=0) \text{----------(5.42)}$$

where

$$K = \frac{Vg}{((at_{ox} \frac{\epsilon_s}{\epsilon_{ox}}) + 1)} \text{----------(5.43)}$$

$$\psi s(x) = K \text{----------(5.44)}$$

For kT << -qψ,

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{q}{\epsilon_s}\{2ni\sinh(\frac{q\psi}{kT}) + N_t \tanh(\frac{q\psi}{2kT})\} \text{--------(5.45)}^{[60]}$$

$$\psi(x) \cong \frac{qN_t}{2\epsilon_s}(x - x_D)^2 \text{----------(5.46)}^{[60]}$$

$$x_D = \sqrt{\frac{2\epsilon_s|\psi(0)|}{qN_t}} \text{----------(5.47)}$$

$$\psi(0) = (V_{gs} - Vfb) - \frac{kTy^2}{2q}\{[1 + \frac{4}{y^2}(\frac{qV_{gs}}{kT} - \frac{qVfb}{kT} - 1]^{\frac{1}{2}} - 1\} \text{--(5.48)}^{[56]}$$

$$y^2 = 2(\frac{\epsilon_s t_{ox}}{\epsilon_{ox} L_D}) \text{----------(5.49)}$$

$$L_D = \sqrt{\frac{kT\epsilon_s}{2q^2 ni}} \text{----------(5.50)}$$

At a point 'xi' away from the surface (figure 5.11), $-q\psi(x) = kT$. Therefore, at a position $x < x1$, equation 5.46 will apply. Otherwise, equation 5.44 will apply. Therefore, the activation energy, Ea, is the difference between the valence band edge and the intrinsic Fermi level as indicated in figure 5.11, and it can be expressed as,

$$Ea = \frac{Eg}{2} + q\psi_s \text{----------(5.51)}$$

As shown in figure 5.12, the calculated Ea is about 0.1eV lower compared to the experimental data, and this, is attributed to the presence of the drain offset structure that is known to cause resistance to the flow of carriers from the source to the drain and possibly over-estimation of trap density. It was indicated in the previous section that the resistance of this offset region is directly proportional to its length (equation 5.33). As such, it is not surprising that the drain current activation energy value is very close to the intrinsic Fermi level for longer offset lengths.

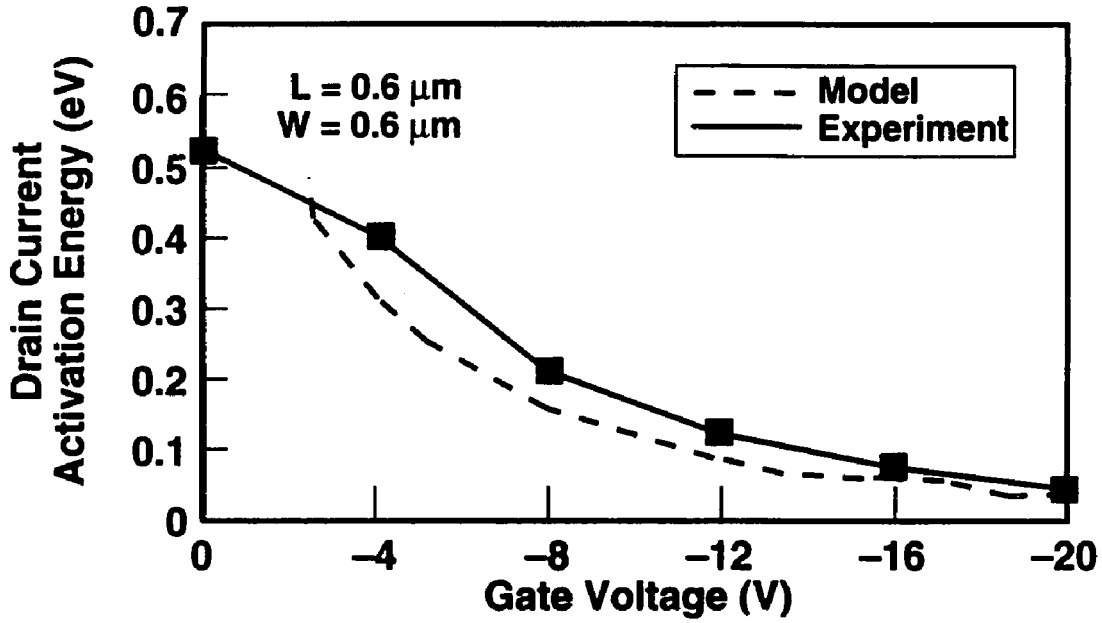


Figure 5-12. Calculated activation energy vs experimental data (gate dielectric is 500Å, Nt = 2E17 /cm^3).

5.7 Leakage current mechanism

Long channel polysilicon TFTs with relatively high ON/OFF current ratios are currently being fabricated[62] [63] . Despite this achievement, the leakage (off state) current still imposes a limit on the duration of video information that can remain on a pixel before it must be refreshed. Several models have been proposed. However, no single model can explain the leakage mechanism. This section will attempt to determine a relationship between the leakage current and off state drain current activation energy for short channel TFT devices. An example of the TFT leakage current as a function of Vgs, Vds is shown in figure 5.13

At low gate and drain voltages (low field), the leakage current is low and it varies almost linearly with the drain voltage (Vds) as was shown in figure 4.11. At higher fields, however, the leakage current varies almost exponentially with gate voltage, and it exhibits a dependency only on the channel width[64] . The dependency of the leakage current on the channel width suggest that carriers are being emitted from the drain space charge region. Additional insight, with regard to carrier emission, can be obtained from the temperature dependence of the drain current in the off state (Ea vs Vg in figure 5.14).

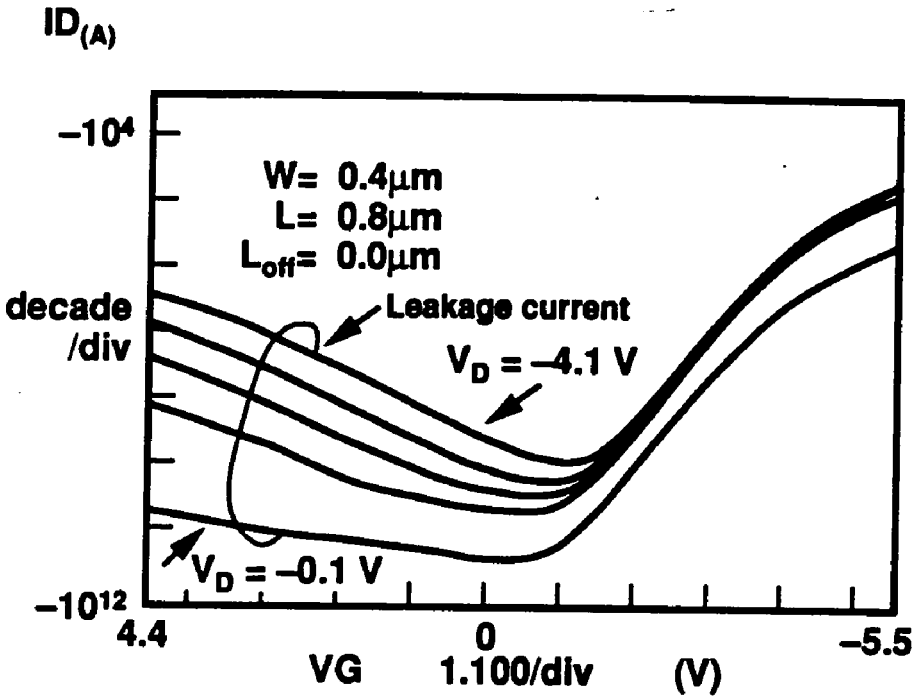


Figure 5-13. Log (Ids) versus Vgs showing leakage current for various drain voltages.

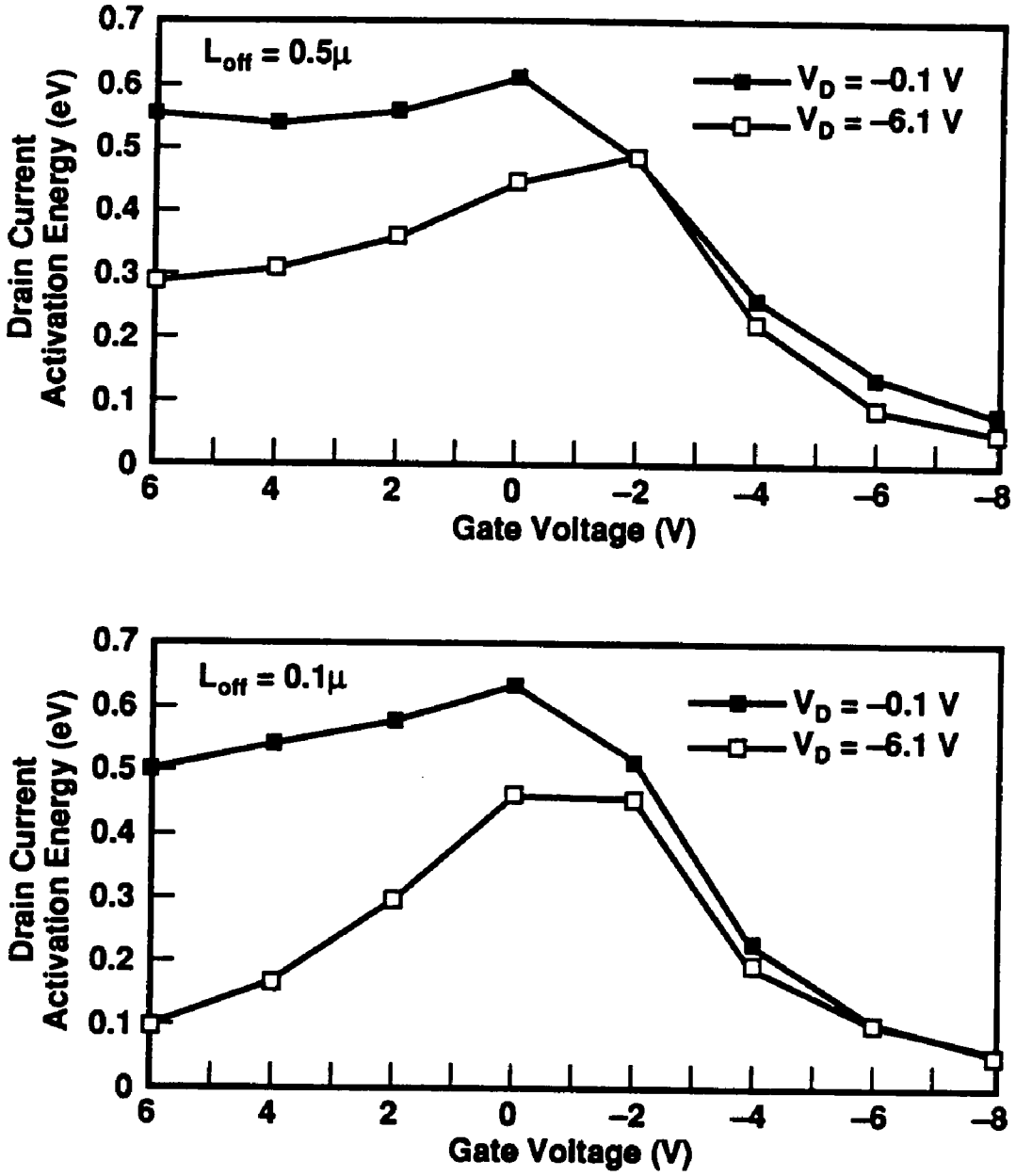


Figure 5-14. Off-state drain current activation energy for two drain biases at 0.5 μm and 0.1μm drain offset lengths.

Carrier generation play an important role in polysilicon TFTs because the polysilicon film contains a large density of midgap and band tail states. The role of the midgap state as a generation center dominates when the carrier level is below its equilibrium level ($np << ni^2$). This condition occurs in the off state. The capture of an electron from the valence band followed by the emission of the electron to the conduction band characterizes the recombination mechanism, and is most active at the midgap energy in the off state. Thus, states at the midgap are more active in supplying electron-hole pairs.

For the carriers to contribute to the leakage current, they must be freed from the trap sites. The most prevalent mechanisms are thermionic emission, tunneling or a combination of both. In figure 5.14, the drain current activation energy decrease as the drain bias is increased. This result suggest two generation mechanism, thermionic emission at low drain bias and thermionic field emission at high drain bias. These mechanisms will be explore next.

5.7.1 Thermionic field assisted carrier emission

Increasing the gate voltage (Vgs) increases the vertical electric field around the $Si:SiO_2$ interface in the drain space charge region which causes enhanced thermal generation of carriers. The thermal generation of carriers out of grain boundary trap states in the drain depletion region is enhanced by the Poole-Frenkel effect[65] [66] [67]. Figure 5.15 shows a one-dimensional Poole-Frenkel model as it

applies to a P-channel device with a drain offset structure under the influence of the drain and gate biases used in this study. The presence of an electric field results in band bending, which in turn reduces the potential energy required for generation. The potential barrier is lowered by ΔE such that carrier emission rate (e^m) can be described by:

$$e^m = e^p[e^{\frac{\Delta E}{kT}}] \text{----------(5.52)}^{65}$$

where e^p is the emission rate in the absence of an electric field.

The Poole-Frenkel leakage current (I_L) is exponentially dependent on the peak electric field (ε)[68] and has the form:

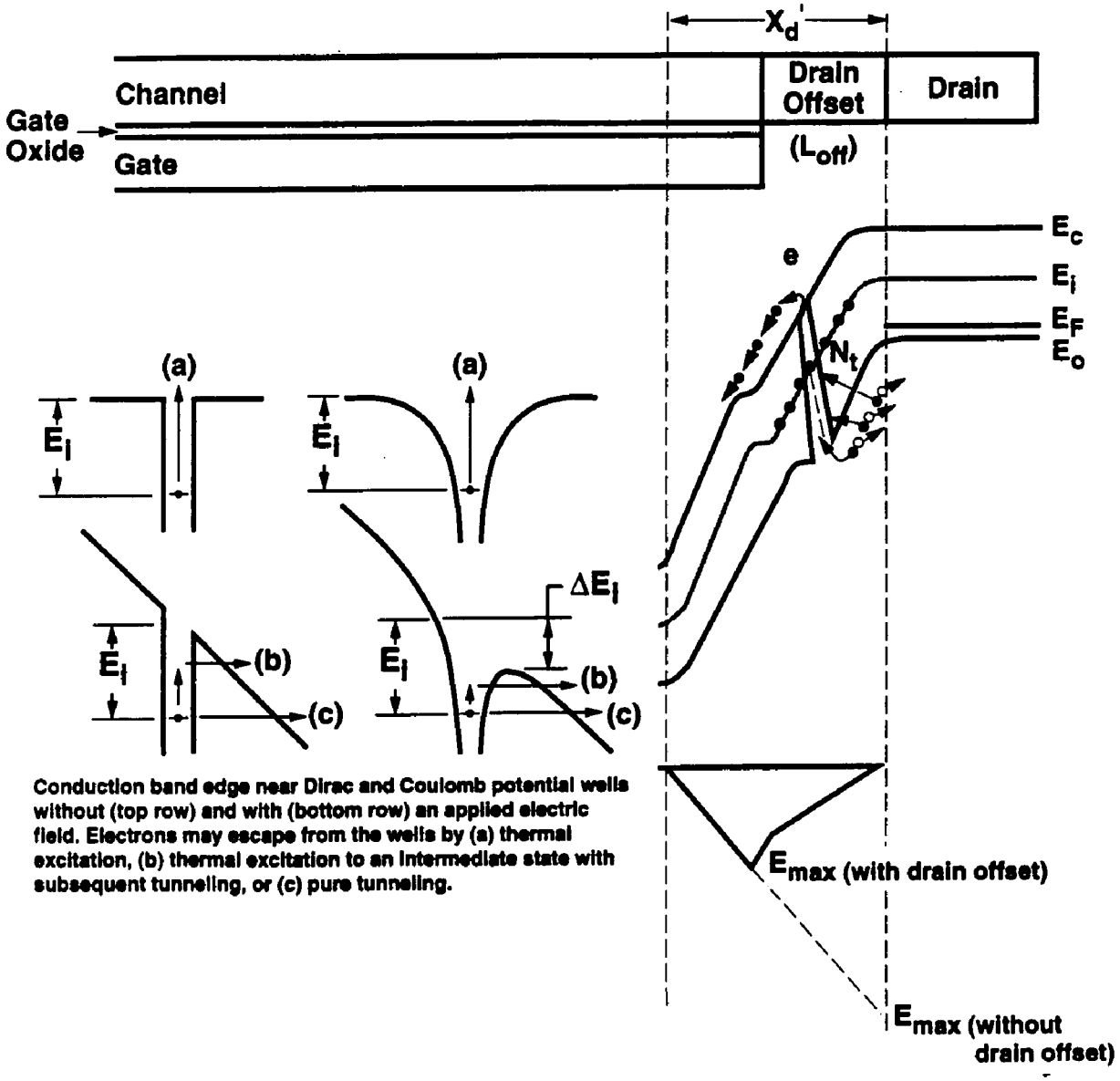
$$I_L = I_L(0)e^{\frac{a\sqrt{\varepsilon}}{kT}} \text{----------(5.53)}$$

where

$$a = \frac{q^{\frac{3}{2}}}{kT\sqrt{\pi \in_s}} \text{----------(5.54)}$$

and

$$\varepsilon = \frac{C_{ox}(V_{gs} - V_{ds} - Vfb)}{\in_s} \text{----------(5.55)}^{[67]}$$



Conduction band edge near Dirac and Coulomb potential wells without (top row) and with (bottom row) an applied electric field. Electrons may escape from the wells by (a) thermal excitation, (b) thermal excitation to an intermediate state with subsequent tunneling, or (c) pure tunneling.

Figure 5-15. Schematic diagram of the one-dimensional Poole-Frenkel model as it applies to a P-channel device with a drain offset structure under the influence of the drain and gate biases used.

where $I_{L(0)}$ is the leakage current at zero electric field.

The use of a drain offset lowers the electric field in the drain depletion region, thereby reducing the band bending and carrier emission rate. The effect of the drain offset on the thermionic field emission of carriers can be modeled as a resistive effect, as was done in section 5.6. Equation 5.53 can be modified to account for the effect of the offset by including the reduction in the voltage across the channel into equation 5.55. Equation 5.55 becomes:

$$\mathcal{E} = \frac{(V_{gs} - (V_{ds} - I_L R_{off}) - Vfb)C_{ox}}{\in_s} \text{----------(5.56)}$$

By substituting equation 5.56 into equation 5.53 and taking the first two terms of the Taylor series expansion and solving for I_L, equation 5.53 becomes:

$$I_L = \frac{\in_s - a^2 C_{ox}(V_{gs} + V_{ds} + Vfb)}{a^2 C_{ox} R_{off}} \text{----------(5.57)}$$

where R_{off} is previously given in equation (5.32).

5.7.2 Carrier tunneling

Figure 5.16 shows a schematic illustration of the band bending and the Dirac well under applied bias used to estimate the carrier tunneling probability.

The tunneling probability of hole from a trap site to the valence band is given by,

$$T_P = e^{-2\int_{-v}^{v}|K(x)|dx} \qquad \text{----------(5.58)}^{[56]}$$

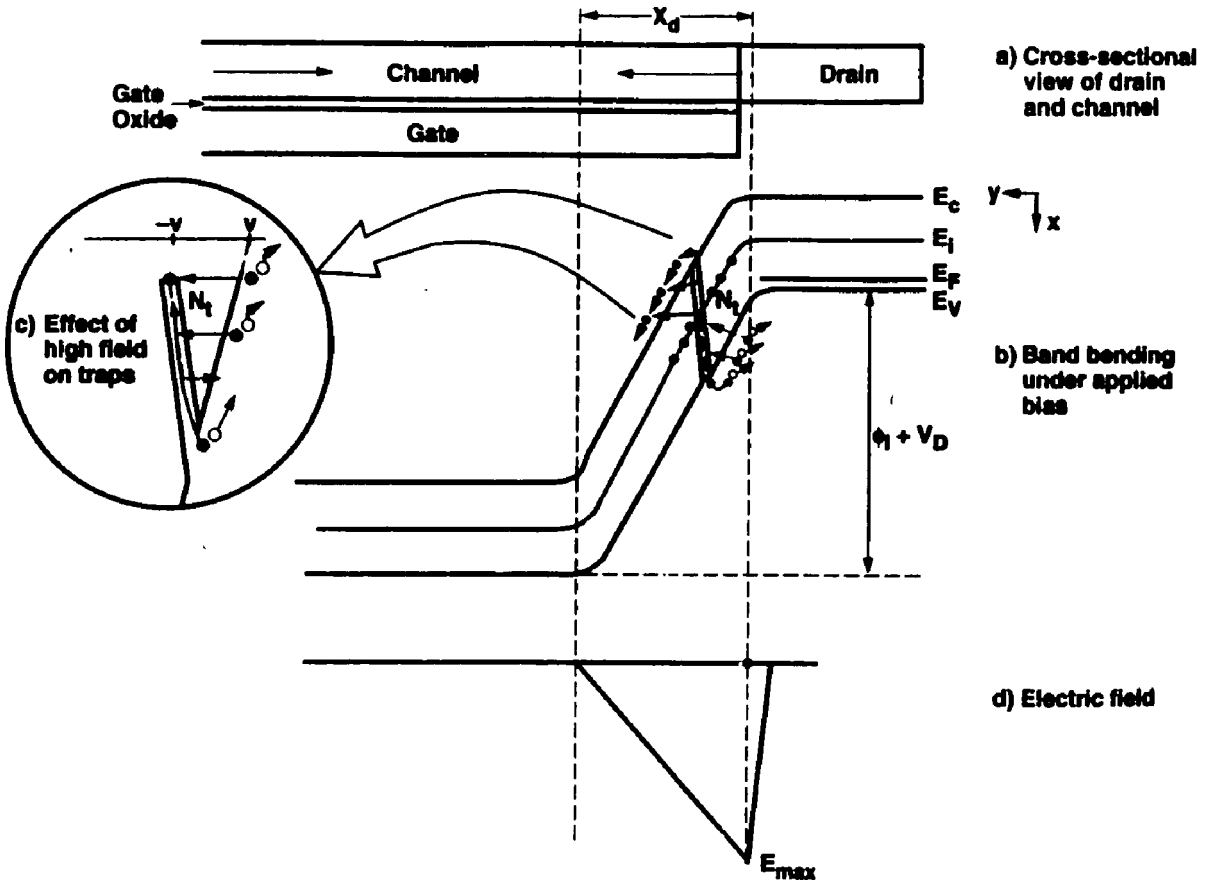


Figure 5-16. Schematic illustration of the band bending and the Dirac well under applied bias used to estimate the carrier tunneling probability.

where |k(x)| is the absolute value of the vector of the hole in the barrier, (-v) and (v) as indicated on figure 4.16. The tunneling of holes through a forbidden band is similar to particle tunneling through a barrier. Consider the triangular barrier formed from the band bending . Then k(x) is given as,

$$k(x) = \sqrt{\frac{2m^*}{h^2}(PE - E)} = \sqrt{\frac{2m^*}{h^2}(\frac{Eg}{2} - q\varepsilon x)} \text{----------(5.59)}$$

where

PE is potential energy,

Eg is bandgap energy,

ε is electric field, and

E incoming hole energy.

Substituting equation 5.59 into equation 5.58 gives

$$T_P = e^{-\int_{-v}^{v} \sqrt{\frac{2m^*}{h^2}(\frac{Eg}{4} - q\varepsilon x)}dx} \text{----------(5.60)}$$

$$T_P = \frac{4\sqrt{2m^*}}{3q\varepsilon h}(\frac{Eg}{4} - q\varepsilon x)^{\frac{3}{2}}|_{-v}^{v} \text{----------(5.61)}$$

at x = v, (Eg/4 -qεx) = 0 and at x = -v, (Eg/4 -qεx) = Eg/2. Using these conditions, equation (5.61) gives the probability of holes tunneling from trap sites at midgap to the valence band as

$$T_P = e^{-\frac{4\sqrt{2m^*}(\frac{Eg}{2})^{\frac{3}{2}}}{3hq\varepsilon}} \quad \text{----------(5.62)}$$

It can be inferred from figure 5.16 that the leakage current is a result of both carrier tunneling and carrier emission. However, it is not a simple addition of the two components. Since tunneling is more effective when the electric field is ≥ 10^6 V/cm, thermionic field emission will dominate below that value. As the field approaches 10^6 V/cm, tunneling will be the dominant leakage current mechanism. Therefore, there is a point where the probability of tunneling equals that of thermionic field emission. As such, both mechanisms must be included in the prediction of the leakage current. By considering the net current due to field-assisted hole emission from trap sites to the valence and conduction bands within an incremental thickness (dy) of the depletion region[69] [70] [71] figure 5.17, we can express the incremental leakage current as:

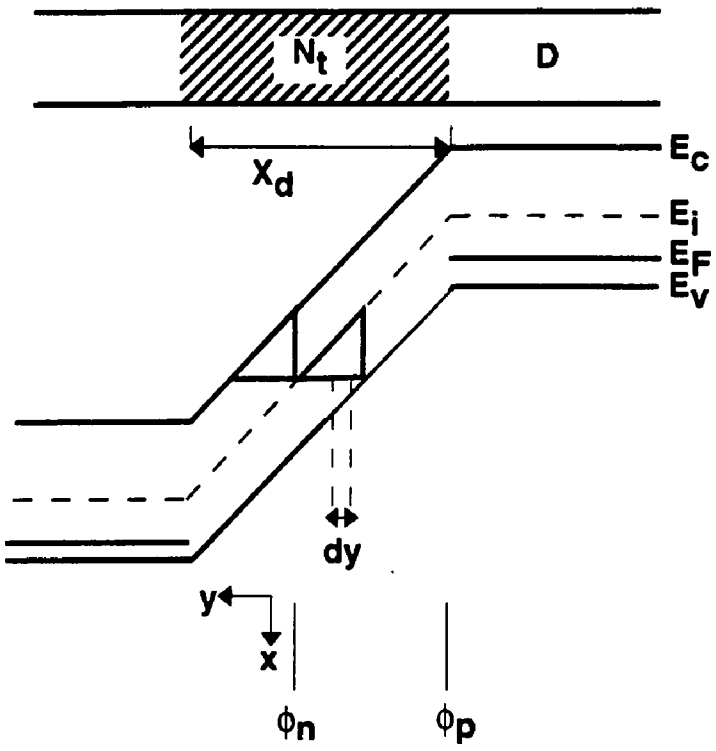


Figure 5-17. Energy band diagram along the surface between the electron inversion layer and the P+ drain in the off state.

$$dI_{L(E_t \rightarrow E_v)} = \frac{q(1-f(T))T_p NtWtch}{} dy \text{----------(5.63)}$$

$$d(-I_{L(E_t \rightarrow E_c)}) = \frac{qf(T)T_e NtWtch}{} dy \text{----------(5.64)}$$

where T_e is the electron tunneling probability. The expression for T_e is similar to that given by the hole tunneling probability, T_p, as given in equation 5.62. W and tch are the width, and the inversion layer thickness, respectively. f(T) is the electron occupancy factor. In the absence of thermal emission, equation 5.63 is equivalent to equation 5.64. From this identity f(T) can be expressed as:

$$f(T) = \frac{T_p + T_e}{T_e} \text{----------(5.65)}$$

If a constant electric field is assumed in the drain depletion region, the leakage current can be obtained by substituting equation 5.65 into equation 5.63.

$$I_L = \frac{qWtchT_t \varepsilon_y V_d}{} \int_{Ei-\Delta E}^{Ei+\Delta E} Nt(E)dE \text{----------(5.66)}$$

$$T_t = T_p + T_e$$

Since the electric field (ε_y) in the depletion region is assumed constant, it can be approximated by:

$$\varepsilon_y = \frac{\phi i + V_d}{X_d} \Rightarrow X_d = \frac{\phi i + V_d}{\varepsilon_y} \text{----------(5.67)}$$

Performing the integration of equation 5.66 yields the leakage current

$$I_L = \frac{qWT_t \varepsilon_y (\phi i + V_d)}{kT} \{N_{st} e^{-\frac{(E_{Fo} - 2\Delta E)}{kT}}\} \text{------(5.68)}$$

N_{st} is the trap density (/cm^3/eV).

For T_p, Eg/2 should be replaced with Et-Ev and for Te, Eg/2 should be replaced with Ec-Et. In equation 5.68, ΔE is the barrier lowering term defined as:

$$\Delta E = \sqrt{\frac{q\varepsilon}{\pi \in_s}} \text{----------(5.69)}^{65}$$

$$\varepsilon = \frac{C_{ox}(V_{gs} + |V_{ds}|)}{\in_s}$$

Equation 5.68 is compared to the experimental data in figure 5.18. From equation 5.68 the activation energy of the drain current in the off state discussed in chapter 4 can be expressed as:

$$Ea = -q\frac{\partial \ln I_L}{\partial \beta} \text{----------(5.70)}$$

$$\beta = \frac{q}{KT}$$

Equation 5.70 compares reasonably well with the experimental data in figure 5.19. The drain current activation energy (Ea) is defined by the exponential term in equation 5.69 as (E_{F0} - 2ΔE). At lower drain bias, the ΔE term is very small. Thus, Ea is approximately equal E_{F0}. E_{F0} is approximately half the band gap. As the gate and drain biases are increased, Ea is proportionally reduced as indicated on figure 5.19.

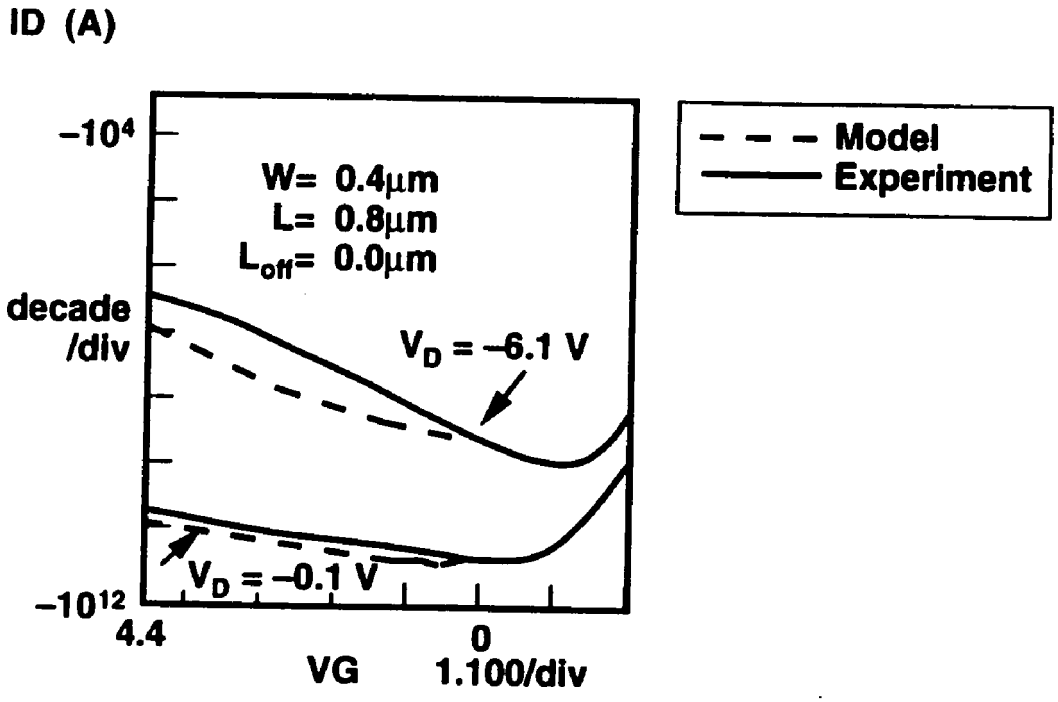


Figure 5-18. Comparison of experimental data to theory for drain current in the off state. Model assume Nst 2E17/cm^3 and180Å gate dielectric.

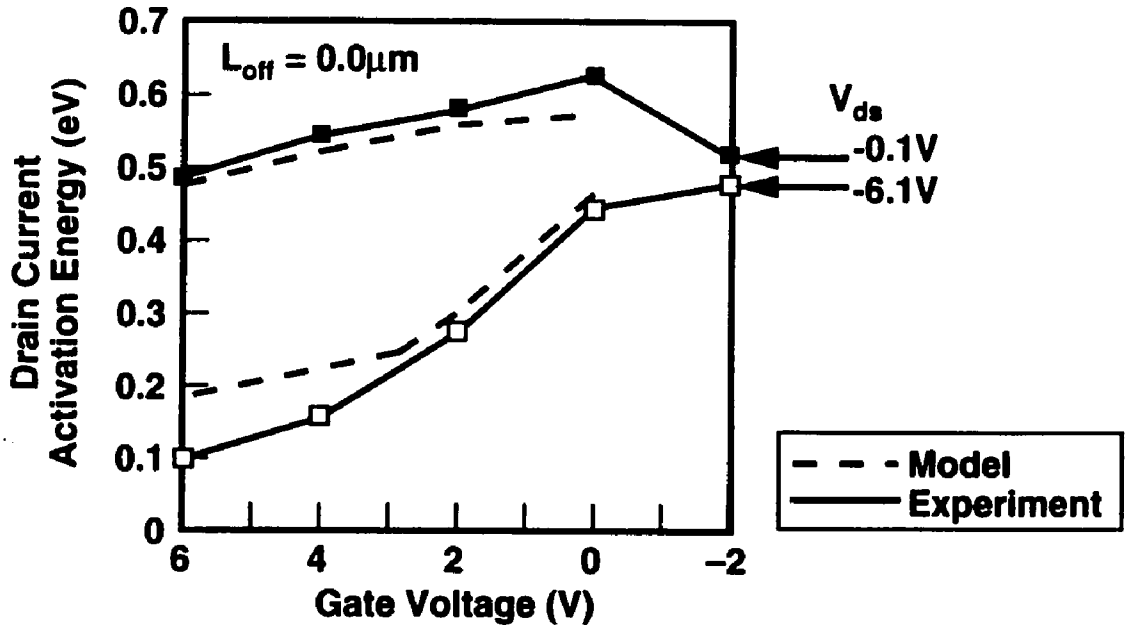


Figure 5-19. Comparison of experimental data to theory for drain current activation energy in the off state (Model assume Nst 2E17/cm^3, 180Å gate dielectric).

Chapter 6 CONCLUSION

This dissertation has described an investigation of the submicron polysilicon thin film transistor. Starting from the conduction properties of polysilicon, special attention was devoted to the "on" current as well as the leakage current. The specific impact of the drain offset structure on the drain current (leakage and "on" currents) characteristics were investigated.

The presence of grain boundaries in the channel influences the channel conductivity. The defects associated with the grain boundaries introduce midgap trap states which influence device performance. In the "off" state, these defects generate carriers that enhance the leakage current. However, when the device is "on", a large fraction of the carriers are trapped by the defect states. This is accompanied by the band bending which leads to the formation of grain boundary potential barriers. Thus, thermionic emission limits carrier mobility across the grain boundary potential barrier when the device operates in the on state. In order to have TFTs with low leakage current, high drive current and steep switching characteristics, it is advantageous to use polycrystalline material with the lowest possible defect density.

Submicron polysilicon TFT devices with channel lengths and widths $\geq$ 0.35μm has been successfully fabricated. The characteristics of these devices are comparable to long channel devices. The switching characteristics are much broader than that of a single crystal MOSFET devices. As a result, the effective

mobility was much lower. The on current was in the order of micro-amp while the leakage current was as low as 0.1 pico-amp. It was found that the leakage current increases as the channel widths are increased.

The drain offset was found to exhibit resistive behavior that tends to lower the TFT drive current as it reduces the leakage current. For the range of channel lengths studied (1.0μm to 0.35μm) the optimum drain offset length was 0.35μm. By modeling the drain offset region as a series resistance drain current equation that agrees well with experimental at Vgs > Vt was obtained.

The study of leakage current activation energy revealed that thermionic emission is the dominant mechanism at low drain bias while thermionic field emission dominate at moderately high drain bias. At -6.1 volts drain bias tunneling is the dominant leakage mechanism for devices with ≤ 3.0μm drain offset length. The insight from the leakage current activation energy was used to formulate a first order analytical expression that combined the effect of thermionic emission and hole tunneling probability to predict leakage current. The predicted leakage current and leakage current activation energy was lower than experimental. This could be attributed to the aerial trap density (1E12 /cm2) used.

Future research

In this work submicron polysilicon TFT was successfully fabricated. However effective mobility was low. This may be attributed to the poor uniformity

of trap density. One of the challenging aspect of polysilicon TFT today is the inability to obtain uniform distribution of grains. A good research work could investigate how some of the available techniques can be used to develop uniform grain polysilicon. With uniform distribution of grains and grain boundaries, it might be possible to solve the mobility problem, and adequately predict grain boundary trap density and also be able to improve device uniformity across wafer.

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Appendix A

Besides additional lithography step already discussed, the two TFT structures used in this study went through identical process sequences. The sequences are summarized below:

Step No	***Name***	***Description***
1	Substrate	5 inch diameter wafer
2	Cleans	1 minute HF clean 5 minutes H_2SO_4/H_2O_2 clean
3	SiO_2	4500Å LPCVD oxide
4	Densification	30 minutes 850°C anneal in N_2
5	Gate Poly	1200Å Gate Polysilicon deposition (LPCVD)
6	Implant	5E15, 35KeV, Phosphorous implant

Process sequence cont.

7	Gate Definition	Photoresist (PR) apply, expose and developed
8	Gate etch	Anisotropic polysilicon etch and PR strip 5 minutes H_2SO_4/H_2O_2 clean followed by 0.5 minute HF sidewall removal.
9	Gate oxide	LPCVD 180Å gate oxide deposition
10	Densification	30 minutes 850°C Nitrogen anneal
11	Channel α-Si	500Å α-Si deposition @ 500°C without delay from previous step.
12	Option	Optional channel implant to adjust threshold voltage
13	Anneal	15 hrs crystallization anneal @ 600°C in N_2

Process sequence cont.

14	Channel	PR apply, exposed and developed
15	Etch	Anisotropic TFT channel etch, PR strip and clean
16	Mask	Deposit 6000Å oxide mask
17	PR	Apply channel mask PR, exposed and developed. This step use source and drain mask.
18	Etch	Etch source and drain oxide mask (figure 3.1c).
19	Implant	Offset implant BF2 or Boron 1E12-1E14 20 KeV
20	Spacer	Deposit 4000Å oxide and etchback 4000Å to form spacer(figure 3.1d)

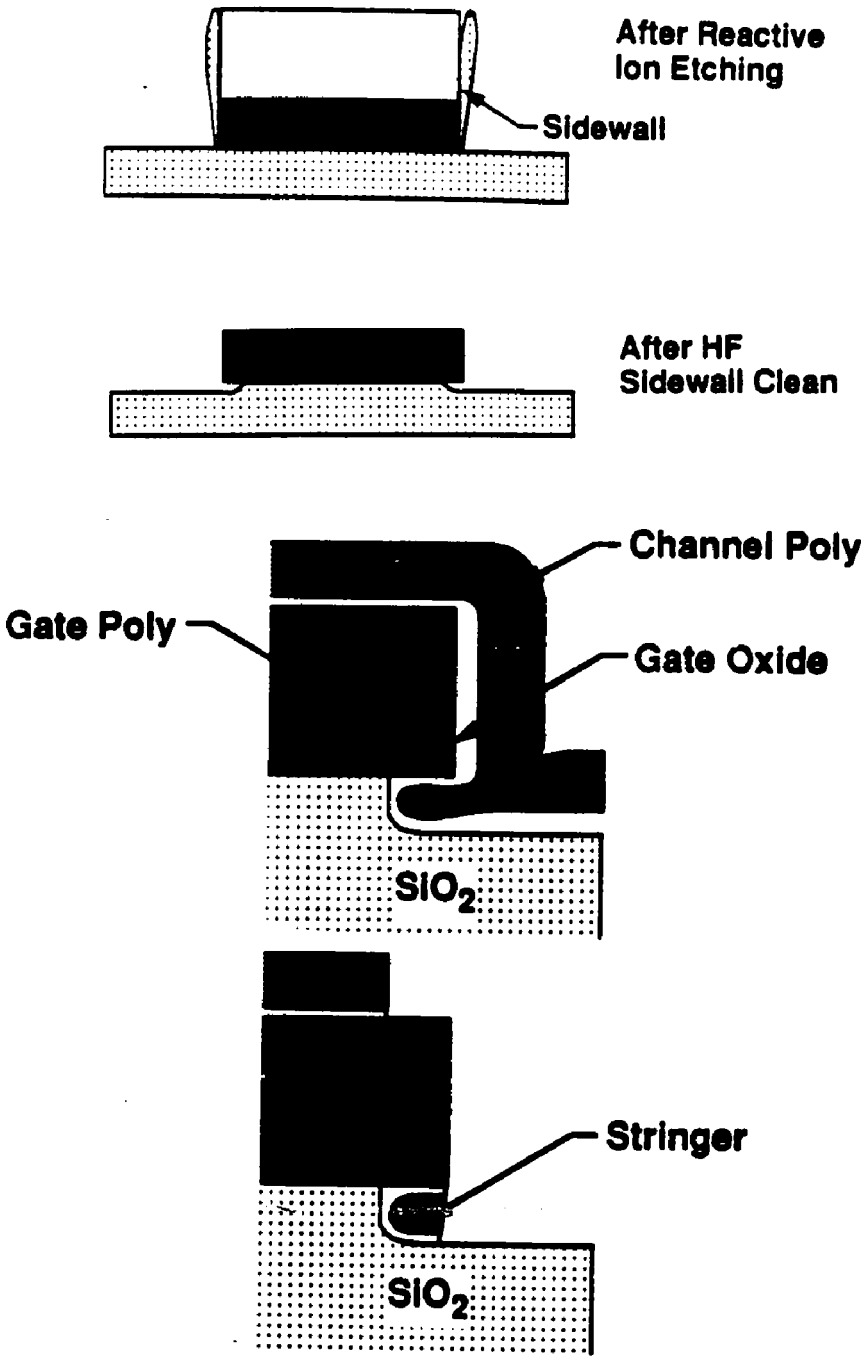
Process sequence cont.

21	Implant	S/D implant 1E15 BF2 20 keV
22*	Note	Steps 19&21 are defined with separate mask for drain only offset structure
23	Insulator	Deposit 1000Å undoped oxide + 4000Å doped glass
24	Anneal	30 minutes anneal @ 850°C in N_2 ambient. This anneal step also activate the dopant.
25	Window	PR applied, exposed and developed.
26	Etch	Window etched and PR stripped and cleaned.
27	Metal	5000Å Al-Cu deposition
28	PR	PR applied, exposed and developed

Process sequence cont.

29	Etch	Al-Cu etch, PR strip and clean
30	Sinter	Hydrogen sinter for 30 minutes @ 370°C.

Appendix B



igure 0-1. **Schematic illustration of gate and channel polysilicon showing process issues.**

VITA

Kolawole Rahman Olasupo was born in Ibadan, Nigeria. In May 1986, he received the BS Degree in Physics from Kutztown University of Pennsylvania. He began graduate study in Electrical Engineering and Computer Science at Lehigh University in January 1987 and he obtained MS Degree in Electrical Engineering in May of 1990. Kola joined AT&T Bell Laboratories in the Fall of 1986 to work on reactive ion etch techniques for submicron VLSI integrated circuits. He has worked on various aspects of VLSI integrated circuits device physics and integration. Kola holds three United State patents and several patent applications pending. He has published several internal and external technical papers.