Effects Of Silicides And Device Structure On The Characteristics And Circuit Performance Of Poly-silicon Thin Film Transistors For Active-matrix Liquid-crystal Displays.

INFORMATION TO USERS

This manuscript has been reproduced from the microfilm master. UMI films the text directly from the original or copy submitted. Thus, some thesis and dissertation copies are in typewriter face, while others may be from any type of computer printer.

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleedthrough, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send UMI a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, charts) are reproduced by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps. Each original is also photographed in one exposure and is included in reduced form at the back of the book.

Photographs included in the original manuscript have been reproduced xerographically in this copy. Higher quality 6" x 9" black and white photographic prints are available for any photographs or illustrations appearing in this copy for an additional charge. Contact UMI directly to order.

UMI

A Bell & Howell Information Company
300 North Zeeb Road, Ann Arbor MI 48106-1346 USA
313/761-4700 800/521-0600

Effects of Silicides and Device Structure on the Characteristics and Circuit Performance of Poly-Silicon Thin Film Transistors for Active-Matrix Liquid-Crystal Displays

by

Greg Sarcona

A Dissertation

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Doctor of Philosophy

in

Electrical Engineering

Lehigh University

1996

Certificate of Approval

Approved and recommended for acceptance as a dissertation in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

5/10/1996

(date)

M Hatalis

(Professor in Charge)

Accepted:

5/10/1996

(date)

Special Committee directing the

Doctoral work of

Greg Sarcona

M Hatalis

(Chairman)

To my parents, all five of them:

Ethel

Harold

Jane

Tom

Lilly

A doctoral committee in their own right.

And of course, to Diane:

"Hockey is as hockey does."

Science... is not what it appears to be. It is not objective and impartial, since every observation it makes of nature is impregnated with theory. Nature is so complex and so random that it can only be approached with a systematic tool that presupposes certain facts about it. Without such a pattern it would be impossible to find an answer to questions even as simple as 'What am I looking at?'

- James Burke

The Day the Universe Changed

"While we wait for a cab, I'll give you your lesson for today. Your lesson is this:

Don't listen to what your schoolteachers tell you. Don't pay attention to that. Just see what they look like and that's how you know what life is really going to be like.

You heard it here first."

- Woody Allen

Crimes and Misdemeanors

Acknowledgments

I would like to thank those people and organizations who have helped me through my graduate program. As a matter of course, I would like to thank my committee members who helped me in the classroom, laboratory, and hallway: Doctors Miltiadis Hatalis, my advisor; David Greve, from Carnegie-Mellon, who directed me to Lehigh; James Hwang, who showed me what it meant to do more than the expected; Ralph Jaccodine, whose wisdom helped me to keep perspective, and Marvin White, who allowed me early use of his lab, and initiated the softball team.

Acceptance of this dissertation concludes the "first generation" of students in the "Hatalite clan." I would like to thank the following who also survived their doctoral programs. Jerry Kung for his improvements to my golf swing, Fuyu Lin for suggestions to my techniques of haberdashery, Dimitrios Kouvatsos for arguing with me on the same side of so many discussions at Denny's ranging from oxidation mechanisms to capitalist theory. Tolis Voutsas for accentuating the difference between scientific and Romantic thought. And Patrick Mc Cluskey, honorary group member, who ensured that the outside world was occasioned to permeate the atmosphere of Sherman Fairchild.

And to the "second generation of students," Dave Fleischer, Rob Klamka, and Su-Heng Lin, I enjoyed imparting my experience upon you and watching you graduate before me. To the "third generation" of students, Mark Stewart, Rob Howell, and Xia Zhou, I bid you good luck, and keep me in mind for a spot on your committees.

I would also like to thank the cartoonists, the hockey team, and the people in the Kitchen. Hari Sathianathan, film critic extraordinaire. Ron Paulsen, who achieved his dream of being Married with Children, and always served plenty of Iowa Beef Burgers with Secret Spices. Amit and Savita Banerjee, who tried always to top the Secret Spices. Neil Cohen, Devils Fan, renowned for his air guitar-- see you in the Stanleys. Matt

Martin, Web&Brewmaster, is the man who knows too much.

Some special associates have earned accommodations and purple hearts. Neil "Torgo" Jenkins, Andy "Shadows" Dawson, Dave "Giggles" Buehrle, Eric "Ears&Nose" Boyle, Alec "Flash--oop" Mercer, and Ritu Bagla (yes, I did go to Smithtown HS West).

I would also like to thank the following people who have had no other reason to be friends other than their kindness. Mary Bowen, who always reminded me that people normally smile. Aida Cabassa, who will be invited to my wedding. Mary Jo Hill, who helped me eat at night. Joe Zelinsky, master craftsman, who always offered temporary asylum and good music. Raymond Filozof was particularly helpful. Bill Hattell of Advanced Energy was selfless, as was his wife during a dinner of RF generator repair.

During my career in the graduate school, I was honored to make the friendships of a few people who were cut from a higher grade of carbon, and offered more of themselves than I had seen by few others. Dr. Ingrid Parson was a dear compatriot. Cheryl and Bill Migatz dedicated themselves to one another and a higher cause of helping people. Athena Colager-Clifford, the first person I met at Lehigh, will always glow from the hope and strength she brought and inspired.

I would like to thank Sean Mc Intyre for his analysis of 500 Felines, and his artistically mathematical viewpoint. The philosophies and infinite optimisms of Whitney Howarth, Pawan Kapur, and Mary Coates were breaths of sweet air, even if only as far away as Moravian College. Dawn Cucco and Richard Mohr win Oscars and Tonys. Nadine and Robert Moses are like grape juice and wine-- always welcome at my table.

This project would be infeasible without the support of my parents. This work was supported by DARPA/ ARPA/ DARPA. But the conclusion was brought through the philosophy of Paul Proteus and Captain Yossarian, and the leadership of Diane Marotta and Mark Messier. And the hope that Opus will find Bridget Fonda.

If two pages is a long time to say thanks, imagine how grueling is octuple-overtime.

Table of Contents

List of Figures

List of Tables

Abstract

The leading technology in flat panel displays is active matrix addressed displays, with either amorphous or polycrystalline silicon thin film transistors as the pixel switching element. For cost and performance reasons, integration of display driver circuitry onto the display substrate is desirable.

This thesis focuses on devices for driver circuitry necessary for AMLCD operation. Circuits to control the data transferred to the pixels are discussed, and their timing constraints determined. The ability of amorphous and polysilicon Thin Film Transistors (TFTs) to meet the needs of the circuits is considered. The characteristics of the devices are examined to determine their utility in driver circuit design.

One of the major limitations of thin film transistors is their series resistance, which decreases the output current and slows the circuit response. In this work, self-aligned silicidation has been developed for thin film transistors to reduce the extrinsic resistance. The principles of silicidation are reviewed, and applied towards the development of cobalt and nickel silicide processes on thin polycrystalline and amorphous silicon and silicon-germanium films. The effect of the film on the electrical properties of silicide is studied.

Cobalt and nickel silicides are used on the source and drain of polysilicon TFTs, and their effects on the device characteristics are analyzed. Their impact is greatest on ultra-thin film polysilicon devices, where the high series resistance limits the current to about 1μA. With silicides, the output current is increased one-hundredfold. The improvement in AMLCD driver circuit performance by the incorporation of silicides is shown by circuit simulation.

The objective of this dissertation is to develop a silicidation process for polysilicon thin film transistors and determine the effects of this process on device performance, and project the improvements to AMLCD driver circuitry this process may provide.

Chapter 1
Introduction

This dissertation examines issues related to devices and circuits of active-matrix liquid-crystal displays (AMLCDs), with emphasis towards displays using poly-crystalline silicon thin film transistors and incorporating drive circuitry on the display substrate. Device performance, circuit design, and materials issues will be discussed. Silicon thin film transistors, both amorphous and polysilicon, are compared on the bases of process, device performance, and utility in integrated-drive AMLCDs. Methods for improving the drive current of polysilicon TFTs are explored.

The design of driving circuits for AMLCDs will then be discussed, with examples for a monochrome VGA panel with integrated scan driver, and data multiplexer. The electrical "load" of the display will be determined and used in the mathematical analysis of driver circuit design. Other circuits which are incorporated in state-of-the-art data driving circuits-- digital-to-analog converters and amplifiers-- will be presented. It will be shown that the most important factor of the drive circuits is the temporal response. This motivates the circuit design and the device process towards maximizing the TFT drive current, and places constraints on the materials viable for signal lines in the display.

Incorporation of silicides to increase the drive current and reduce the duration of the display signal transients will be explored. The basics of silicidation will be presented, followed by a comparison of processes and films of various silicides for use in both the device process and panel manufacture for AMLCDs. A self-aligned silicidation process for polysilicon TFTs will be presented, and device results will be presented.

The fundamentals of each of these areas is discussed in this Chpater.

1.1 Active Matrix Liquid Crystal Displays

The term "flat panel display" covers a wide range of products and technologies. A flat display is any display which is flat; these can include thin CRTs. Flat display technologies include: plasma emission, light-emitting diodes, electroluminescence, field-emission, and liquid crystal. Liquid crystal technologies include twisted-nematic, supertwisted nematic, polymer dispersed, ferroelectric, and cholesteric [1].

Liquid crystal displays (LCDs) emerged on the consumer market on wristwatches in the early 1970s. The display used twisted nematic liquid crystal, and was reflective, using ambient light reflected from the backside of the display as its light source. The advantages of LCDs over CRTs are many; they are lightweight, space-efficient, and can have higher resolution. Quickly, their definitive advantages were combined with promised advantages of low-cost manufacture to promise the "television hanging on the wall." While this has not occurred, and may still be far away [2], the advantages of LCDs have produced new products and applications for displays: laptop computers, hand-held personal devices, video viewfinders, projection displays, virtual reality, and a wealth of consumer products. LCDs have replaced CRTs in niche applications, including dashboard and cockpit assemblies [3].

Although the display applications and technologies are numerous, they share the same few fundamentals: pixels and addressing. Pixels compose the array of elements which must produce the image. When they are addressed, the pixels are given the information used to create the image. In passive addressing, the pixel voltage is held by a capacitor between the scan and data lines. However, the pixel is sensitive to crosstalk of the data written to the neighboring pixels. And, the capacitor may exhibit high leakage, which would degrade the image quality throughout the frame period. In active addressing, the pixels are switched by a transistor. The pixel voltage is sensitive to the data voltage on its data line when the switching element is on (scanned). Since this thesis concentrates on

devices for twisted nematic active-matrix liquid crystal display technologies, the discussion below of pixels and their addressing will be be specific to this display technology.

In active matrix liquid crystal displays (AMLCDs), the pixels are individually controlled by a switching element which is addressed by a controller external to the display. Most displays use silicon TFTs as the pixel switching element. In the silicon TFT-LCD arena, there is continuing competition between amorphous and polycrystalline (poly) silicon TFTs. For large area substrates, glass is used as an inexpensive substitute for quartz. Since glass has a much lower thermal limit (~ 600°C, and even lower for cheaper glasses), amorphous silicon TFTs is the dominant technology for mass-production items, like laptop computer displays. The low-temperature process is inexpensive and ideally suited to amorphous silicon technology, and easier than polysilicon processing technology. However, the inferior mobility of the amorphous TFT requires that all control be supplied from connections to external drivers, using chip-on-glass (COG) or flexible tape-automated bonding (TAB) connectors [4]. For a color VGA display, there could then be 2400 connections: 640 for each vertical line in red, green, and blue, and 480 horizontal lines. These connections would be arranged around the perimeter of the glass substrate.

For high-definition and small-area displays, like liquid crystal light valves for projection applications there may not be enough peripheral area for the connections. Hence, control circuitry must be included on the display substrate. Also, small area displays can be made on quartz substrates, allowing polysilicon processing. In direct-view displays, the issue between the two technologies of amorphous and polysilicon TFT LCDs is in the middle ground, where the cost of the addition of external drivers may offset the costs due to yield loss when polysilicon driver circuitry is integrated into the

display. Chapter 6 will explore integrated drive circuits, and show that the key factors in driver design are sheet resistances of the signal lines and of the devices.

1.1.1 Active Matrix Liquid Crystal Display Panel Construction

The liquid crystal display is assembled from essentially four components: the front and back glass panels, the liquid crystal filling the gap between them, and the backlight. Figure 1-1 shows a typical flat panel AMLCD assembly. On the outer surfaces of the glass panels are polarizers. The inner face of the glass panels are covered with a thin, transparent metal film. The film on the front glass panel is unpatterned and connected to a fixed voltage. The other panel, the "active panel," has its transparent film patterned into an array of electrodes. The electrodes delineate the pixels. On the periphery of the active plate are either on-display driver circuits or connections to external driver circuits.

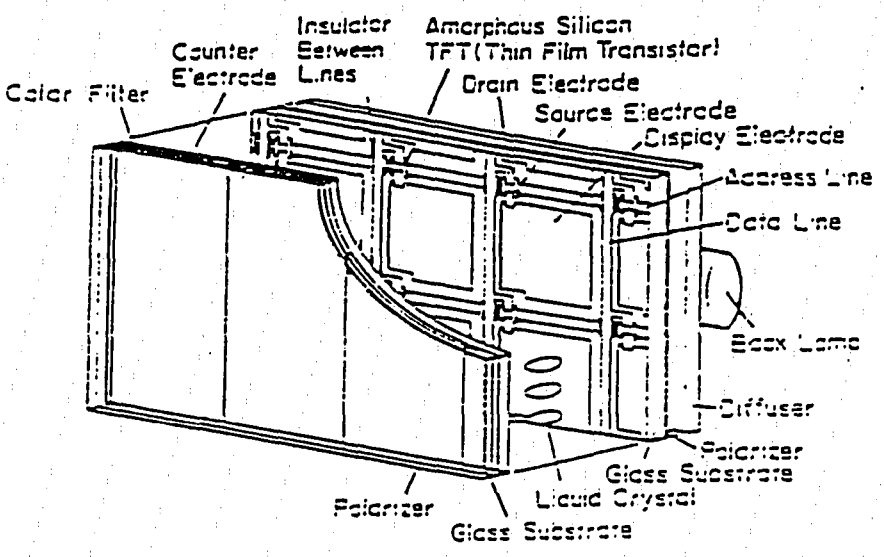


Figure 1-1. Assembly of AMLCD components. [Kung, 5]

An active matrix display is similar to a capacitor-based DRAM. Each pixel consists of a transistor and a capacitive element, composed of the capacitance of the liquid crystal between the transparent metal electrodes and a "storage" capacitance (described below). The pixels are addressed by their row (or *scan*) line and column (or *data*) line. In a thin film transistor (TFT) liquid crystal display, the pixels are isolated by a TFT pass transistor between the data line and the pixel electrode. Figure 1-2 shows the physical layout of a TFT-switched pixel and its circuit equivalent.

When a row is turned on, or is scanned, the voltage on the scan line turns all of the TFTs of that row on. The data line voltage can then be passed through the pixel TFT onto the pixel electrode. The voltage difference between that of the pixel electrode and the common voltage on the opposing glass plate creates an electric field across the liquid crystal within the area of the pixel. The transmission of light through the pixel area is modulated by the applied data voltage, as shown in the transmission-voltage curve in Figure 1-3 [6].

The transmission of light through the pixel is modulated by the field across the liquid crystal. In the twisted nematic (TN) LCD, the liquid crystal is in the nematic phase, where the molecule is rod-shaped, and there is a 90° rotation of these molecules from one side of the cell to the other, as shown in Figure 1-4. The liquid crystals are oriented by a polymer layer which is "rubbed" to produce an alignment direction. The liquid crystal molecules gradually twist from bottom to top to accomodate the alignment of the two polymer layers. On the side facing the light source, the polarizer is parallel to the bottom plate rub direction.

Light is linearly polarized to match the direction of the nematic molecules. If there is no field across the liquid crystal, the liquid crystals gently twist 90° in rotation. The light transiting the cell is rotated, and exits the liquid crystal with the same linear polarity as the top rub layer. In a normally-on device, the top polarizer is parallel to the upper plate rub

direction, and the light is transmitted through the polarizer. If an electric field exists across the cell, the nematic liquid crystal molecules point in the direction of the field, and are less able to rotate the light. Thus, when it reached the top polarizer, it has the wrong polarity, and is not passed.

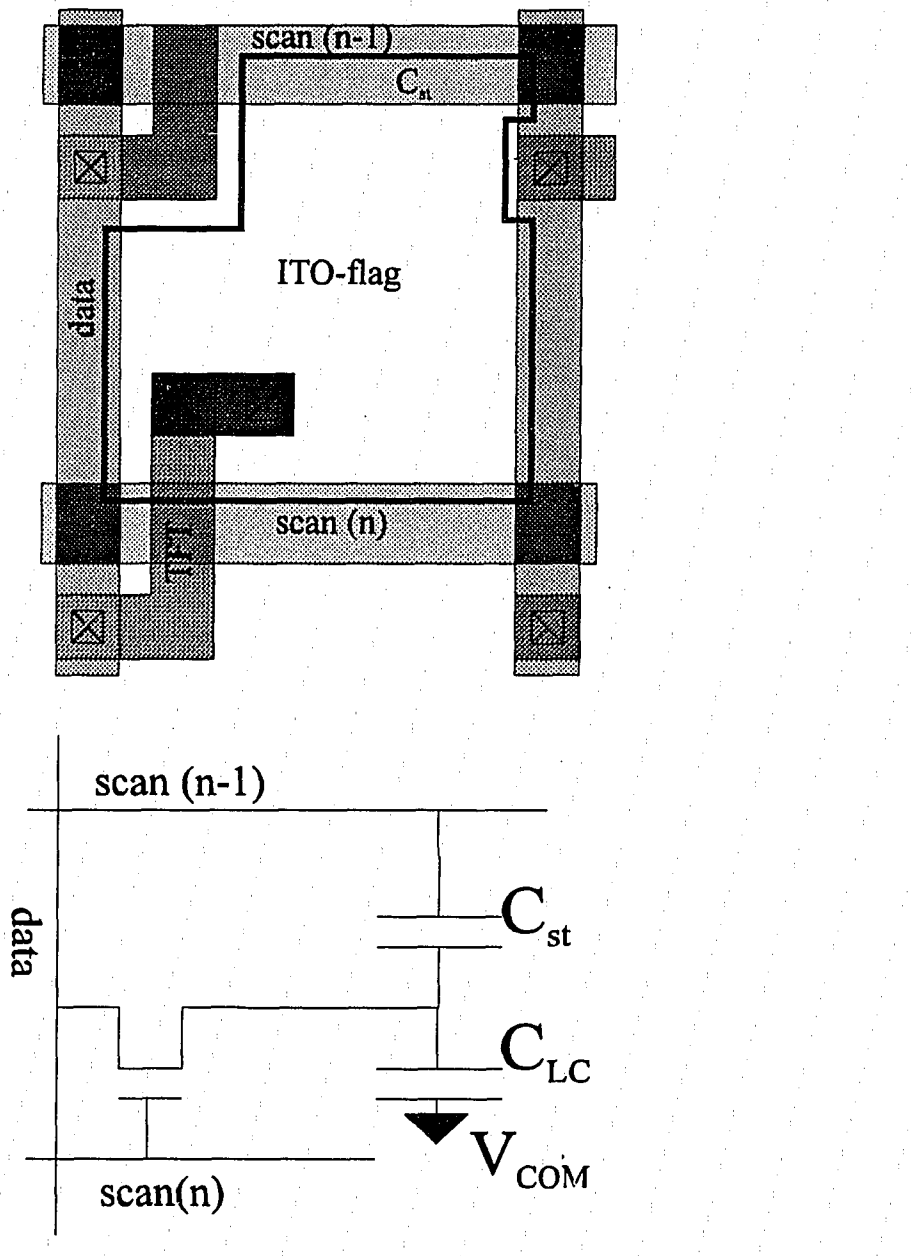


Figure 1-2. Layout and equivalent circuit of pixel in TFT-LCD.

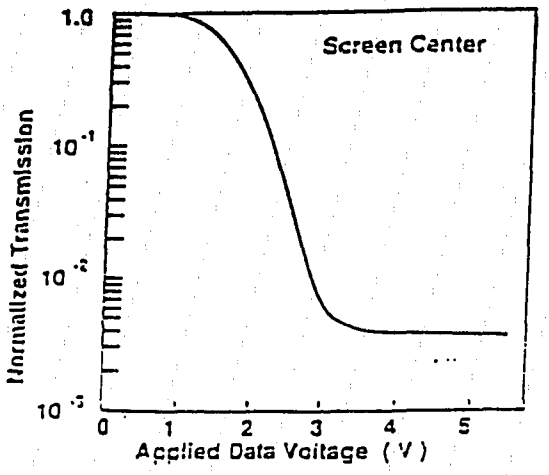
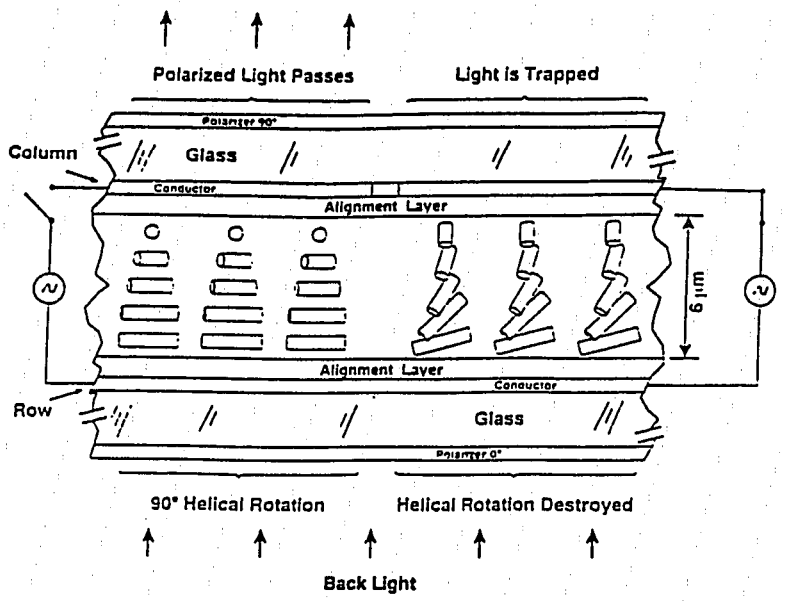


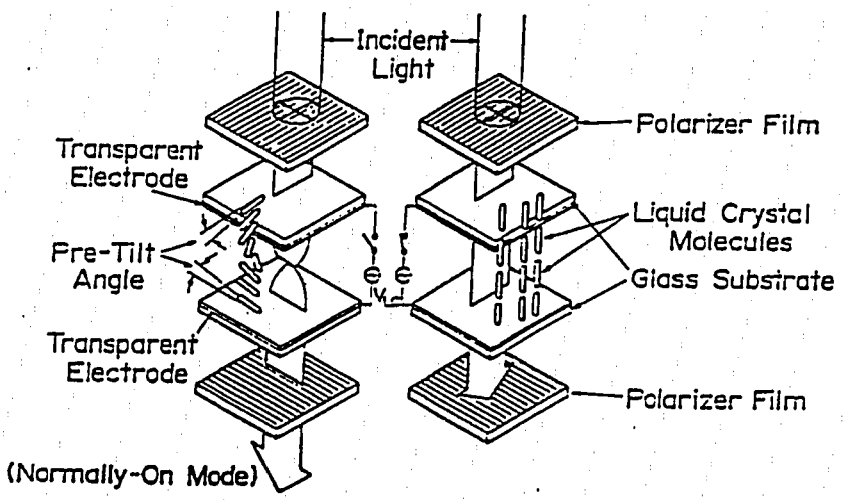
Figure 1-3. Transmission vs. Voltage curve for Normally-On Twisted Nematic liquid crystal cell. [Takafuji, 6]

Since the transmission curve of the TN cell is a gradual function of voltage (as shown in Figure 1-3), gray scales can be produced by applying pixel electrode voltages between those which produce white and black states. A color pixel group (figure 1-5) can be created by placing over the top glass plate a color filter which repeats red, green and blue regions each over cells, and applying appropriate gray scales to each sub-pixel in the color group to provide the proper intensity of red, green, and blue light. The collective intensity of red, green, and blue light gives the viewer the appearance of a color dot.



White State Black State

(a) Cross-Sectional View



White State Black State

(b) Operational View

Figure 1-4. Twisted Nematic Liquid Crystal Cell: white and black states. [Kung, 5]

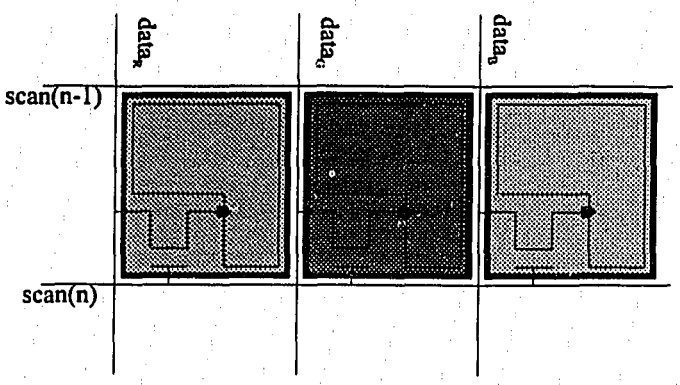


Figure 1-5. Composition of a color pixel.

1.1.2 Pixels in AMLCDs

The pixels are the fundamental elements of the display area. They are connected to the drivers by the scan and data lines. The components of a pixel are: data line connection, scan line, pixel TFT, storage capacitor, and the ITO flag. The layout and circuit equivalent schematic of a pixel are shown in Figure 1-2. Pixel design issues directly affecting the aperture ratio center around the pixel pitch, the amount of storage capacitance required, and the size of the TFT. Storage capacitance and TFT sizing will be discussed in Chapter 6, Display Design.

1.2 Thin-Film Transistors

1.2.1 Overview

Thin film transistors (TFTs) are fabricated by depositing a thin (< 2000 Å) layer of silicon on an insulating substrate. The devices are isolated by defining each into a discrete island on the substrate. TFTs are field-effect devices, similar to MOSFETs, but having

no substrate terminal (see Figures 1-6(a) and 1-7(a)). Since the silicon under the gate is typically undoped, the "type" of the TFT is determined by the doping of the source and drain, which are to produce blocking contacts to the channel. For example, an n-TFT has n-type source and drain regions. When a positive voltage is applied to the gate, the island beneath it is depleted. As the gate voltage increases, electrons are attracted to the surface, forming a conducting layer. Because the source and drain are n-type, electrons are able to be extracted and supplied for current. The electron layer is often called the "inversion layer" as in MOSFETs. In the off state, the gate voltage is negative with respect to the source, holes from the intrinsic channel silicon would be attracted to the gate. However, holes which would be collected at the surface under the gate would be blocked by the n-type doping of the source and drain, so that they cannnot contribute to conduction. The TFT is not an ambipolar device.

1.2.2 Amorphous Silicon Thin Film Transistors

Amorphous silicon thin film transistors are fabricated in a thin amorphous silicon film typically deposited by plasma enhanced chemical vapor deposition (PECVD) at low temperatures, ranging 300°C to 400°C. Gate dielectrics and insulators, SiO_2 and SiN_x are also deposited by PECVD [7,8]. The temperature range of all of these processes is within the thermal processing window for large-area, low cost glass panel substrates. This, and the applicability of the PECVD technique to large area substrates, and the low current in the off-state are the main advantages of amorphous silicon technology for AMLCDs.

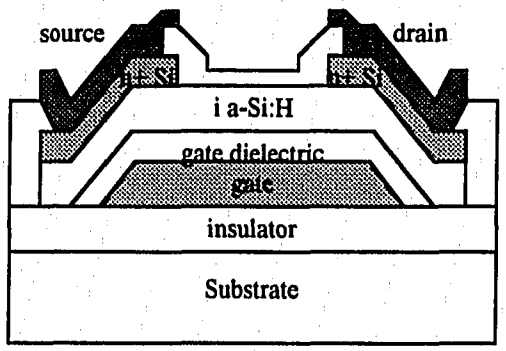
The source and drain regions are formed by patterning a deposited n^+ layer on top of the island. Figure 1-6 shows the amorphous silicon transistor structure and device characteristic. Note that the off-current is quite low. In the display array, the off-current of the pixel switching elements has a strong impact on the pixel design and image quality.

The main disadvantage of the amorphous TFT is its low mobility, typically about or below 1 cm^2/V-sec. In order to achieve a high drive current in the on-state, a device needs a large width. The large width increases the gate capacitances of devices in circuits composed of amorphous TFTs, causing them to be slow. These factors make the incorporation of drive circuitry with amorphous silicon TFTs difficult to realize [4].

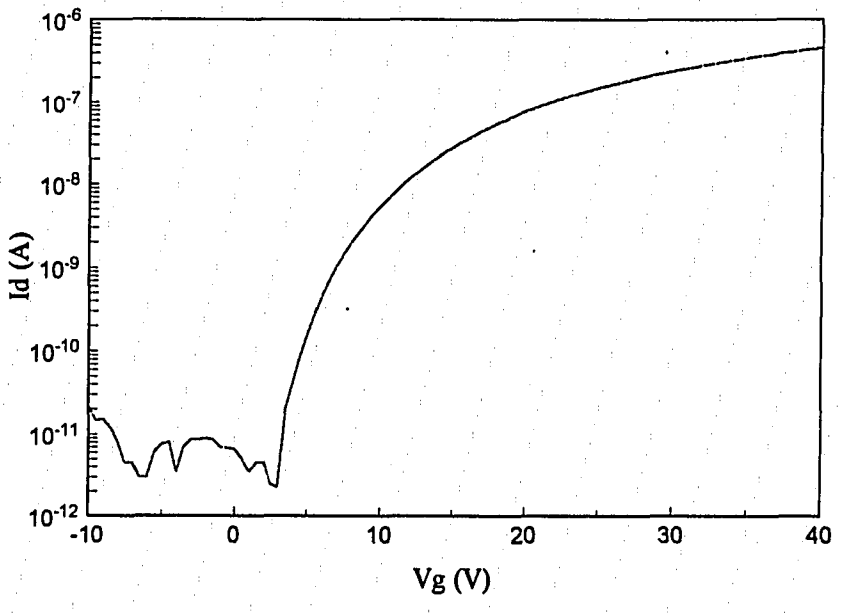
1.2.3 Polycrystalline Silicon Thin Film Transistors

Polycrystalline silicon (polysilicon) films can be produced on glass and quartz substrates by many methods. Low-pressure chemical vapor deposition (LPCVD) is commonly used to deposit polycrystalline silicon. The silicon can be deposited in the amorphous, microcrystalline, or polycrystalline states [9,10]. The amorphous or mixed-phase films can be crystallized into polycrystalline films by furnace annealing, rapid-thermal annealing, or laser-annealing [11,12]. The gate dielectric can be either a PECVD or a thermally-grown SiO_2 film, or SiO_2-SiN_x multilayer dielectrics [13,14,15]. Source and drain regions are formed by ion implantation. Grain boundary defects are passivated by forming gas annealing (*e.g.* post-metal anneal) and by plasma hydrogenation.

The polysilicon film structure, device structure, and processing treatments have a dramatic affect on the polysilicon TFT device parameters and characteristics, *e.g.* on-current, off-current, threshold voltage, mobility, and subthreshold swing [14]. Furnace annealed devices easily achieve mobilities over 40 cm^2/V-sec. Excimer laser annealed polysilicon TFTs have been reported to have mobilities over 200 cm^2/V-sec [12]. Since n-type and p-type polysilicon TFTs (n-TFT and p-TFT) can be formed, CMOS-design based circuits using TFTs can be fabricated on the display substrate, allowing for integrated drive circuitry [16]. A polysilicon n-TFT and its device characteristics are shown in Figure 1-7. Because the source and drain regions are thin, they exhibit high series resistance, which degrades the drive current.

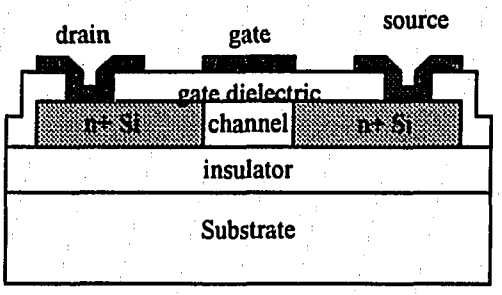


(a) Device Structure.

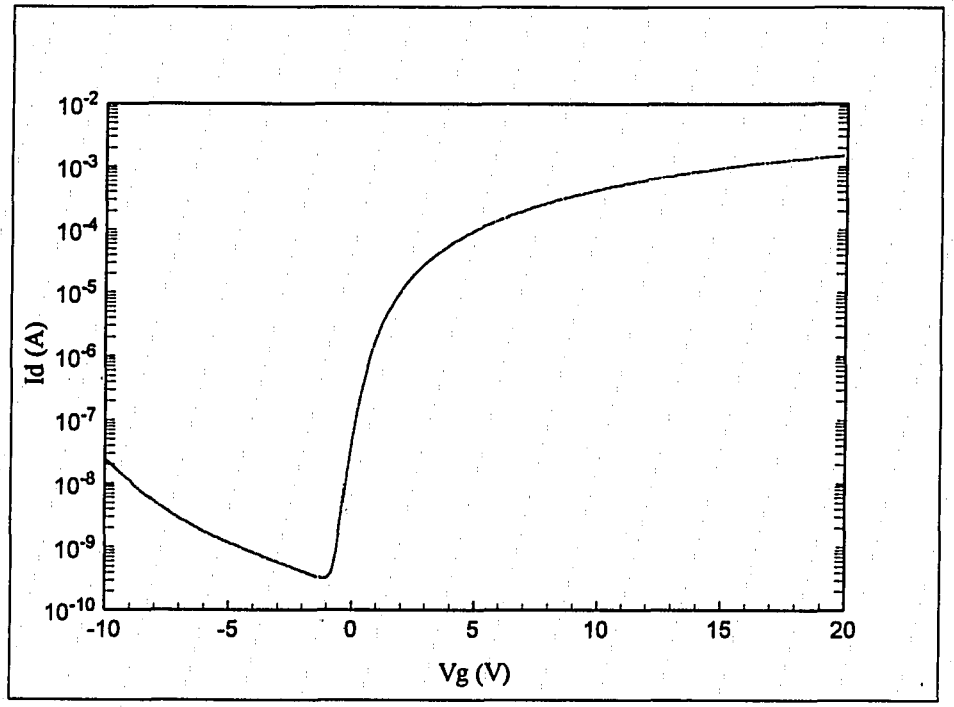


(b) Device Characteristics

Figure 1-6. Amorphous silicon TFT (a) structure and (b) device characteristics.



(a) Device Structure



(b) Device Characteristics

Figure 1-7. Polysilicon TFT structure and device characteristics.

1.3 Silicide Principles

Silicides have low resistivities, approaching those of refractory metals. Silicides can be formed by many methods, but the most common is by annealing metal on silicon. The temperature required for the anneal is dependent on the metal specie; nickel will silicidize at 400°C, whereas titanium requires annealing above 800°C to form the lowest-resistance phase. Silicide resistivities range from 15μΩ-cm to 100μΩ-cm, depending on the metal and the fabrication process [17]. Silicides are chemically resistant, and are compatible with device process temperatures. For comparison, the resistivity of aluminum is 4μΩ-cm, but cannot withstand device process temperatures and chemicals. Heavily doped polysilicon has a resistivity greater than 300 μΩ-cm.

Silicides have long been incorporated in single-crystal silicon CMOS circuit technologies. Self-aligned silicides (salicides) increase device current and thus circuit speed by reducing parasitic external resistances associated with the device terminals (the source and drain) and the wiring between them and the driven gate. Silicides have not yet been applied to TFTs technology, but have been used as the scan line in AMLCD technology [18]. In this dissertation, a silicidation process will be developed for TFT technology.

1.4 Organization

The objective of this dissertation is to develop a silicidation process for polysilicon thin film transistors and determine the effects of this process on device performance, and project the improvements to AMLCD driver circuitry this process may provide.

In Chapter 2, silicidation principles, fabrication technologies, characterization methods will be reviewed. The theoretical effect on device performance will be discussed.

In Chapter 3, the silicidation process for cobalt and nickel silicides developed at Lehigh University's Display Research Laboratory will be presented. The electrical characteristics of the silicides will be presented.

In Chapters 4, amorphous silicon and silicon-germanium thin film transistors with ion-planted source and drain regions will be presented.

In Chapter 5, the effects of device structure and process on polysilicon TFTs will be explored. Devices with diffused and ion-implanted source and drain regions will be compared. The effect of the polysilicon island thickness will be examined. Salicided TFTs of both thick and thin polysilicon islands will be analyzed. The improvements silicidation gives device performance will be determined.

Chapter 6 will describe AMLCD drive circuitry and pixel design. The electrical load of the display array will be derived. Scan circuits, including the shift register, level shifter, and drive buffer, will be constructed using polysilicon TFT parameters for nMOS and CMOS processes. The achitecture of data drivers will be illustrated. Digital-to-analog converters will be designed using four different methodologies. Data multiplexers of both nMOS and CMOS will be compared. The effect of silicidation on the speed performance of the driver circuits will be illustrated through simulations.

In Chapter 7, the work presented herein will be summarized, and directions for continuing work will be itemized.

In the Appendix, descriptions of the process sequences for silicide and device fabrication will be detailed.

Chapter 2
Principles of Silicides in MOS-Based Technologies

2.1 Introduction to Silicides

For increasing device density and speed, scaling rules require narrower gate and interconnection lines and shallower junctions. Interconnection of devices becomes difficult in the areas between devices. The gate metallization layer is often used as the first wiring layer. Scaling issues produce high resistance source and drain regions, and gate stripes, often made from doped polysilicon. As the device gate area decreases, the speed of CMOS circuits becomes dominated by the resistances involved in connecting the devices: parasitic series resistance, contact resistance, and wire resistance.

Silicides are formed by reaction of metal with silicon during heating. Silicides provide a thermally and compositionally stable low-resistance ohmic contact to silicon. Self-aligned silicidation (salicide) processes which selectively silicidize the source and drain regions reduce the extrinsic resistance of devices. Silicides have resistivities ranging from 15 μΩ-cm to 100 μΩ-cm [17]. These values are much lower than highly-doped polysilicon (around 1mΩ-cm), and similar to thin films of refractory metals (*e.g.* chromium, tantalum, tungsten). Silicides have been shown to be diffusion sources for shallow junctions, or can be used to make contact to them [19,20].

The desired properties of a silicide are many. The primary characteristic is the silicide's resistivity. This material parameter dictates the range of sheet resistance the silicide can achieve, depending on its thickness. The circuit designer, determining a maximum sheet resistance for a wiring layer, may require a silicide to have an impractical thickness; in this case, a different metal must be used for silicidation.

Considerations for which silicide to incorporate into a process depend on the metal and its resulting silicide. The metal should form silicide at a temperature below the

process limit imposed by junction rediffusion or substrate warpage. The silicidation reaction should occur easily, with as little dependence on surface cleanliness and doping as possible. The silicidation process should result in a smooth silicide surface and silicide-silicon interface. For shallow junction applications, the silicide should consume as little of the underlying silicon as possible during the silicidation process. For use as a contact, the silicide should make ohmic contact to silicon. Some silicides, *e.g.* platinum, form Schottky junctions. The silicide should have good adhesion with low interfacial stress. Poor adhesion and high stress may cause peeling of silicide wiring layers [21]. High stress of a silicide gate stripe can create electronic defect states [22].

The silicide should be resistant to chemicals used after the silicidation process step. This includes HF and fluorine plasmas used to open contact windows through the insulating dielectric. The silicide should resist oxidation, since surface oxides may increase the contact resistance to the overlying metallization wiring layer.

2.2 Silicide Fabrication

2.2.1 Effect of Metal Type on Silicidation Process

The silicidation process is dependent on the metal used. Noble metals (cobalt, nickel, palladium, platinum) form silicides at temperatures below 700°C. In these films, metal atom migration dominates growth. These films as such are less likely to form silicides with SiO_2, and less likely to form bridging shorts between the gate and the source and drain upon silicidation. Refractory metals (tungsten, titanium, tantalum, molybdenum) form silicides at high temperature, above 800°C, where silicon atom diffusion dominates growth. In these films, silicon precipitates may form at the edges of the silicide, silicon void formation under the silicide is possible, and there may be a metal reaction with SiO_2. These films are more susceptible to bridging shorts due to silicon migration along the gate sidewall spacer. Figure 2-1 shows the effects of silicidation temperature on the physical

structure of the silicide. Note that the higher temperature silicidation exhibits silicon precipitates [17].

The growth of the silicide is also dependent on the metal. During the silicidation process, the metal-silicon ratio changes according to the phases-- or layers of phases-- formed. Most metals ultimately form their lowest-resistance phase in the disilicide (MSi_2) phase, which forms at the highest temperature, as shown in Figure 2-2 [23]. This is the thermally stable phase, and subsequent annealing will not affect the silicide. To form the disilicide phase, metal-rich phases are formed first. Depending on the metal specie, and the amount of metal deposited, the film will entirely change phase, or will form layers of phases, as illustrated in Figure 2-3 [24]. Table 2-1 lists common metals used for silicides in CMOS processes, and their characteristics [17,25].

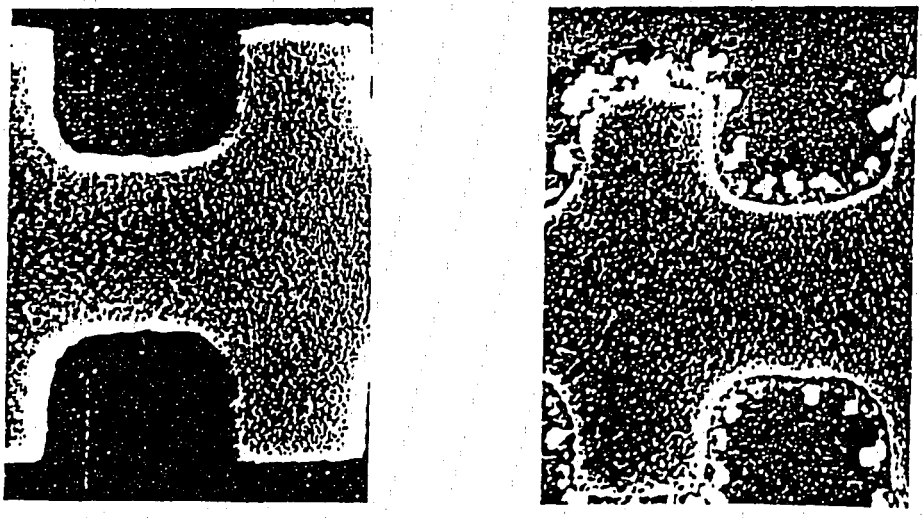


Figure 2-1. Effect of temperature on silicide film. [Murarka, 17]

metal	metal resistivity ($\mu\Omega$-cm)	lowest resistance silicide phase	silicide resistivity ($\mu\Omega$-cm)	silicidation temperature (°C)
W	5	WSi_2	20 - 70	> 1000
Mo	5	$MoSi_2$	15 - 100	1000
Ta	14	$TaSi_2$	30 - 50	900
Ti	45	$TiSi_2$ (C54)	13 - 25	800
Co	6	$CoSi_2$	13-20	600 - 700
Pt	11	PtSi	30	450
Ni	8	NiSi	14	300-400
Pd	11	Pd_2Si	30	~ 300

Table 2-1. Metal and Silicide Data Table.

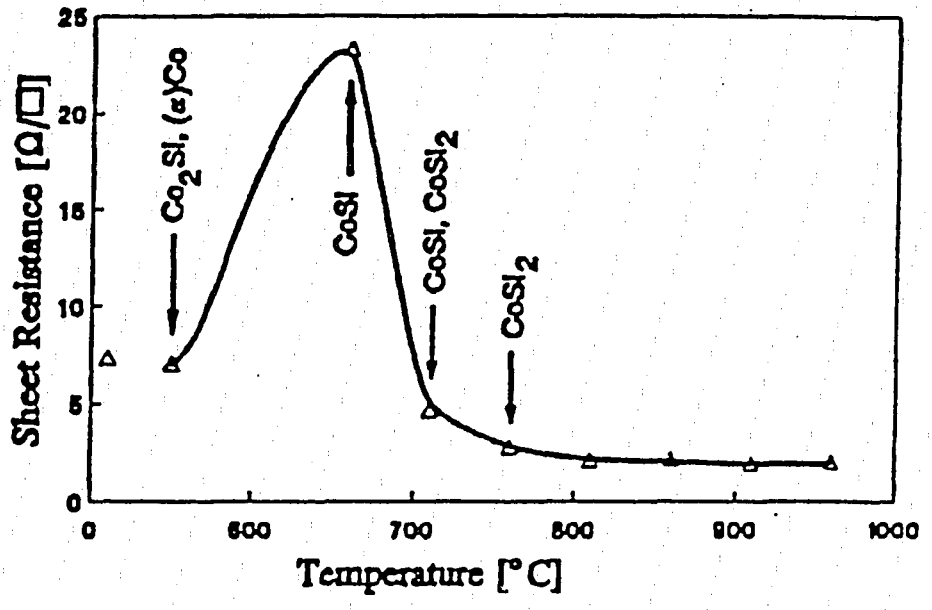


Figure 2-2. Effect of Temperature on Phase and Sheet Resistance of $CoSi_2$.

[Niewohner, 23]

Phases indicated by XRD after annealing by RTP for 12 s at different temperatures of samples of series A with 30- and 100-nm-thick Co films.

Temperature (°C)	30 nm Co	100 nm Co
350	Co	Co
400	Co	Co
450	Co/Co_2Si	Co
500	Co/Co_2Si	Co/Co_2Si
550	Co_2Si/CoSi	Co/Co_2Si/CoSi
600	Co_2Si/CoSi	CoSi
650	CoSi/$CoSi_2$	CoSi/$CoSi_2$
700	$CoSi_2$	CoSi/$CoSi_2$
750	-	$CoSi_2$
800	-	$CoSi_2$
850	-	$CoSi_2$
900	$CoSi_2$	-

Figure 2-3. Transition from Metal to Disilicide Phase. [Freitas, 24]

2.2.2 Effect of Deposition Method on Silicide Film

Silicides can be fabricated by depositing either the metal and annealing, or depositing the silicide directly. Annealing a metal film deposited either by sputtering or evaporation produces a purer silicide film, which has a lower resistivity. Silicide would be formed on all exposed silicon. The resistivity in general is dependent on the temperature and duration of the anneal. Since these silicidation processes require annealing, the silicide interface may be rough. Silicides can be patterned, typically by etching in HF-containing solutions.

The window-masked selective silicidation process, illustrated in Figure 2-4, is the easier of the methods described. In this process, windows are opened in a deposited oxide layer to expose silicon where silicide is desired. Following an HF-dip, metal is then

deposited and annealed in a furnace, or a rapid thermal lamp system. The specifics of this anneal are metal dependent. In cobalt silicide technology, the silicidation anneal at 600°C to 700°C is followed by a metal etch to remove any remaining metal-rich phases at the surface, and any unreacted metal. In titanium silicide technology, after the titanium deposition, a mixing anneal in nitrogen below 700°C is performed to predeposit high resistance TiSi and $TiSi_2$(C49 phase). Titanium and titanium nitride are etched from the oxide layer, leaving silicide within the windows. The titanium silicides are then annealed at or above 800°C in Ar to finalize the $TiSi_2$ in the low-resistance C54 phase [26].

Metal and silicon can be sputtered from two targets, simultaneously, in the co-sputtering process. This process is used for hard, refractory metals which either cannot be evaporated, or require very high silicidation anneal temperatures. The advantages of this process are good metal to silicon ratio control, and a smooth interface. However, this process has poor step coverage, and lacks selective deposition capability.

Silicides can be sputtered from a single, silicide alloy target. WSi_x is commonly deposited by sputtering. While composition control is easily maintained, step coverage is difficult, and the target may have incorporated contaminants [18].

Chemical vapor deposition [27] and molecular beam epitaxy [28] have been used to deposit tungsten and cobalt silicide films. Step coverage is excellent, but the surfaces are rough, and the films have poor adhesion.

2.2.3 Effect of Anneal Method on Silicide Films

Annealing can be performed in a furnace or by a lamp system, *e.g.* rapid thermal annealing. Furnace anneals are more uniform on the wafer, and since multiple substrates can be annealed simultaneously, have higher throughput and better wafer-to-wafer uniformity. The ramp-up and ramp-down (cooling) cycles of lamp systems may create non reproducible results, especially for short anneals. Also, the radiation of the lamp

system may not be uniform, causing spatial nonuniformities of the silicide on any given substrate.

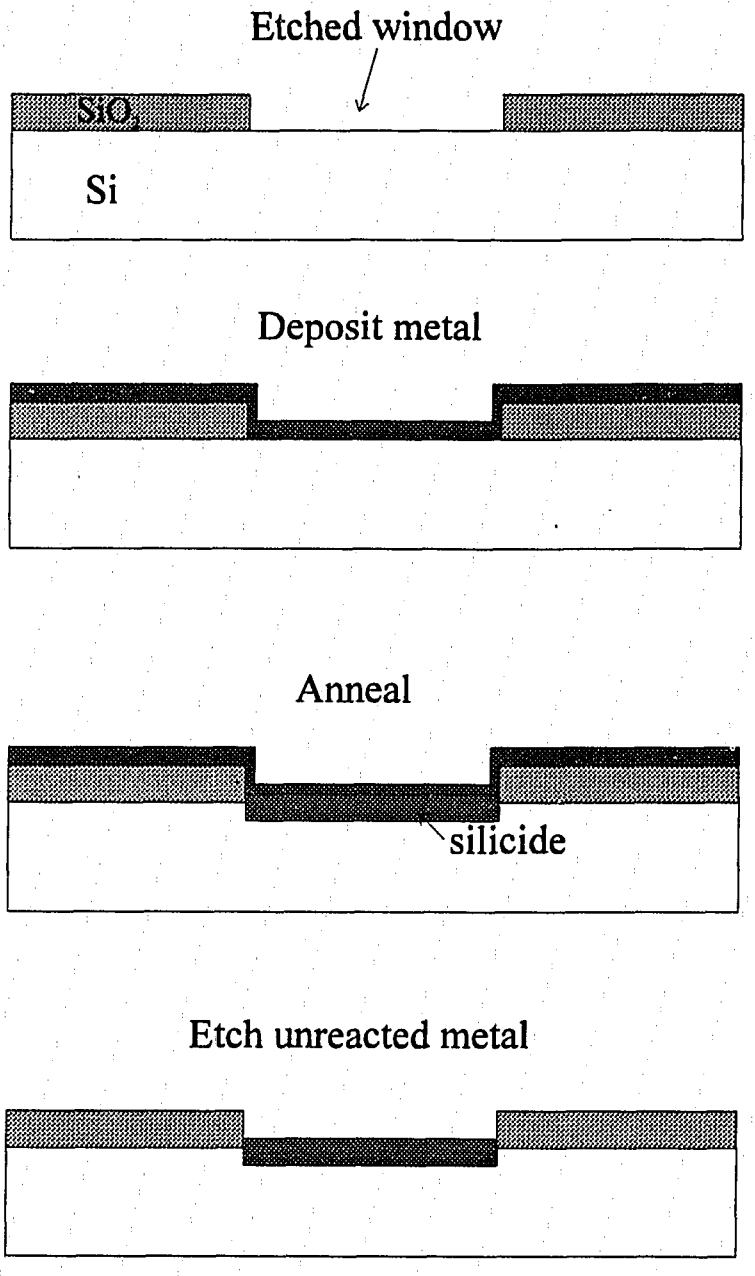


Figure 2-4. Process Sequence for Window-Patterned Silicidation Requiring One Anneal

However, lamp annealing is often faster than furnace annealing. A furnace anneal may require an hour, whereas a lamp anneal requires only a few minutes to form a silicide. The shorter thermal cycle causes less dopant redistribution and lateral growth of silicides [29,30].

2.3 Physical Characterization of Silicides

Physical characteristics important to analysis of silicide films are the thickness, composition, and crystal structure. Since films in contemporary processes are below 1000Å thick, thickness is obtained by cross-sectional transmission electron microscopy (TEM). Diffraction-mode TEM can be used to provide phase and crystal structure information. Figure 2-5 shows TEM and diffraction-TEM photos of cobalt germanosilicide, formed by annealing cobalt on heteroepitaxial SiGe on Si [31].

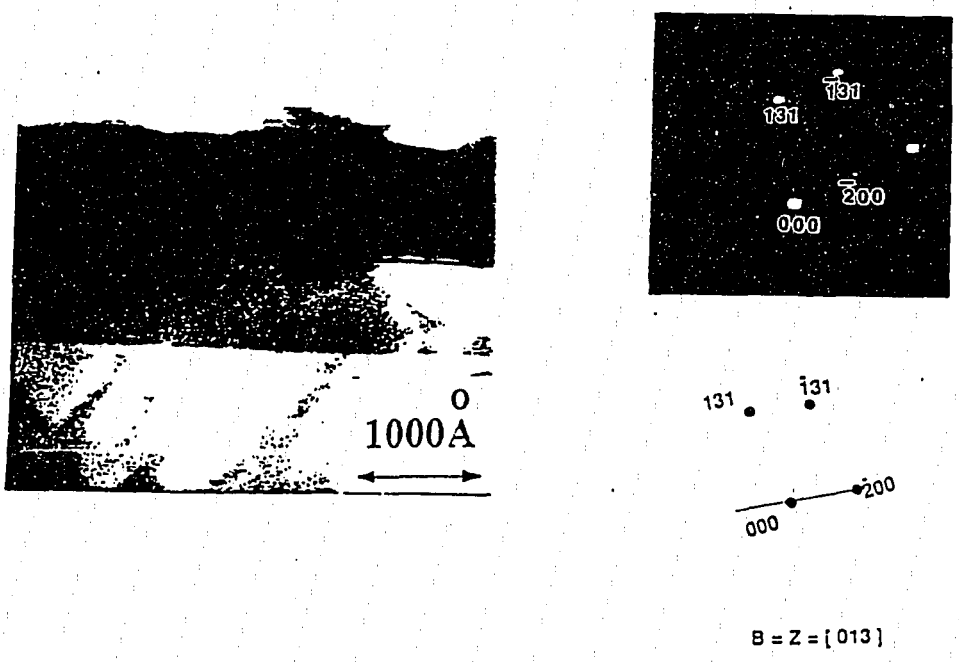


Figure 2-5. Cross-section of cobalt germanosilicide and diffraction pattern. [Lin, 31]

Film composition can also be obtained from energy dispersive electron analysis, Rutherford backscattering, and sputtering Auger electron spectroscopy. Figure 2-6 shows energy dispersion analysis of the cobalt germanosilicide layer atop the SiGe epilayer from Figure 2-5. The peaks indicate the presence of cobalt, silicon and germanium [32].

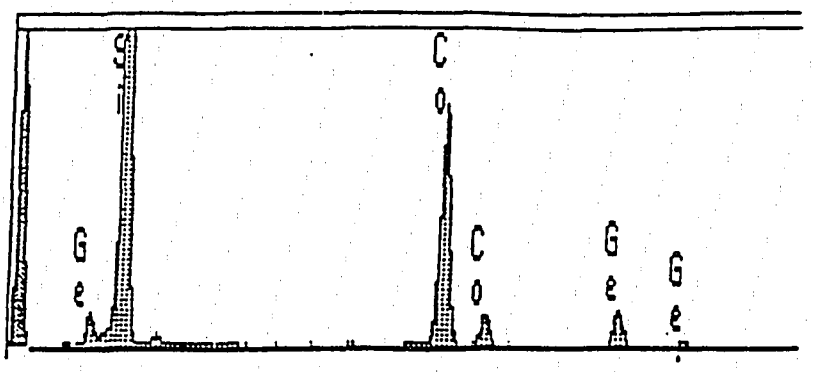


Figure 2-6. Electron Energy Dispersion Analysis of
Cobalt Germanosilicide on SiGe/Si. [Sarcona, 32]

2.4 Electrical Characterization of Silicides

The important electrical parameters of silicides are their resistivity and specific resistance. The resistivity is a material parameter, and can be used to determine the phase of silicide, and its purity. Electrical parameters useful to circuit designers are the sheet and contact resistance, which are functions of the resistivity and specific contact

resistance and the dimensions of the silicided feature. These values are dependent on the width, length, area, or thickness of the feature.

2.4.1 Sheet Resistance

The resistivity, ρ, is typically on the order of 10^{-6} Ω-cm, and is reported in units of $\mu\Omega$-cm. Silicides have resistivities in the range of 10 to 100 $\mu\Omega$-cm, depending on the metal specie and anneal temperature. For comparison, the resistivity of aluminum is 3$\mu\Omega$-cm, and n^+ polysilicon is around 300 $\mu\Omega$-cm.

The sheet resistance, R_S, measured in $\Omega/\square$, is defined as:

$$R_s = \frac{\rho}{x} \tag{2.1}$$

Note that the sheet resistance is a function of the film thickness, x, in cm.

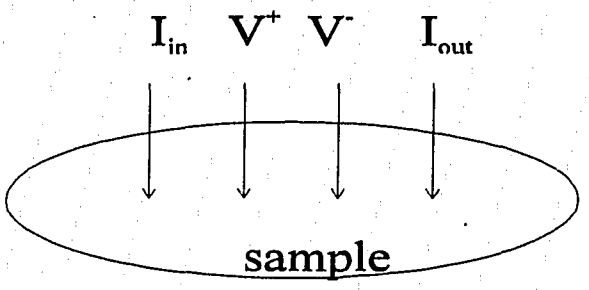
The resistance of a silicide line, R, measured in Ω, is determined by the length, L, and the width, W, of the feature:

$$R = R_s \frac{L}{W} = \frac{\rho}{x}\frac{L}{W} \tag{2.2}$$

Hence, for a design with a resistance limit, the silicide can be made thicker or wider for a given length. If the geometry cannot be accommodated, the resistivity can be decreased by using a silicide with a lower resistivity.

The resistivity is determined by measuring the sheet resistance and thickness. The sheet resistance can be measured by a simple four-point probe setup, as illustrated in Figure 2-7. Four evenly-spaced probes are placed on an unpatterned sample, and current is driven through the outer probes. A voltage is measured through the two middle high-impedance probes. This probe voltage is multiplied by a geometric factor; for large

samples, where the probe spacing is much smaller than the sample area, and much larger than its thickness, that factor is 4.53.

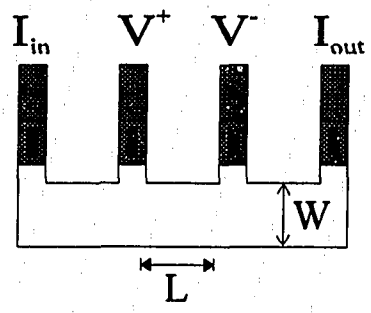


$$R_s = 4.53\frac{V}{I}$$

Figure 2-7. Four-point Probe Measurement of Sheet Resistance

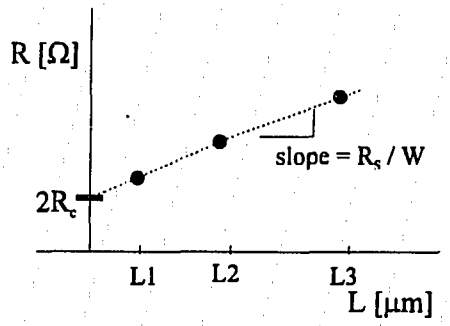
On processed wafers, the four-point probe measurement can be made by using a four-point probe structure, as shown in Figure 2-8. A bar of material is patterned to have four contacts: two outer contacts for current, two for measuring the voltage drop. The sheet resistance is simply the voltage divided by the current, multiplied by the inverse of the aspect ratio of the portion of the bar between the voltage monitor contacts.

The transmission-line, or multi-tapped resistor, method uses different lengths of a stripe of material to determine the sheet resistance. Since only two probes are used to measure the resistance, the measured resistance is the sum of the sheet and contact resistances for that length. Assuming the contact resistances are the same for each contact pad to the stripe, the sheet resistance can be deduced by the difference in resistance of two lengths of the stripe, as illustrated in Figure 2-9.



$$R_S = \frac{W}{L}\frac{V}{I}$$

Figure 2-8. Four-point Probe Structure to Measure Sheet Resistance of Patterned Silicide.



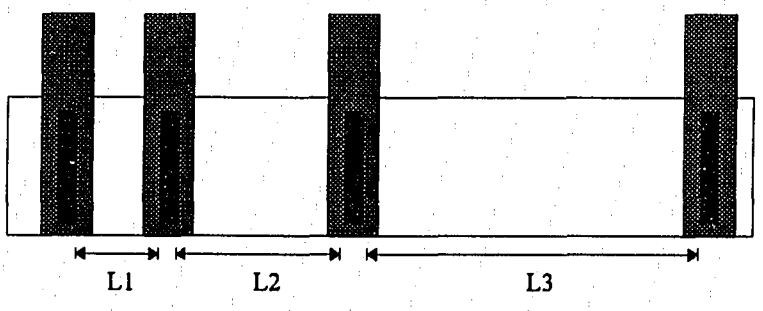


Figure 2-9. Transmission Line Method for Measuring Sheet Resistance.

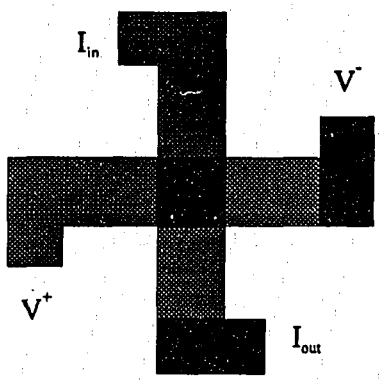
2.4.2 Contact Resistance

The contact resistivity, ρ_C, for competitive technologies is about 1 $\mu\Omega$-cm^2. Aluminum makes contact to n^+Si with a resistivity of about 3$\mu\Omega$-cm^2 or less. Silicides in our lab have been measured to make contact to silicon with a resistivity of about 1 - 100 $\mu\Omega$-cm^2 and in contact to aluminum at less than 1$\mu\Omega$-cm^2. The contact resistance, R_C, is a function of contact area, A_C, in cm^2. The contact resistance is also greatly affected by the measurement technique [33].

$$R_c = \frac{\rho_c}{A_c} \tag{2.3}$$

The transmission-line method of Figure 2-9 can be used to determine the contact resistance. Plotting the resistance as a function of length, the resistance-intercept, where L=0, will give $2R_C$. Another method to measure contact resistance is the four-terminal, or Kelvin, resistor, in Figure 2-10.

In this structure, current is forced between two probes, and voltage measured by two high-impedance probes. The current-in probe, and one of the voltage probes, are the silicide or metal atop the contact. The current-out probe, and the voltage reference node, are at the bottom of the contact. Hence, the voltage drop is measured from the top to the bottom of the contact; division by the current gives the contact resistance, R_C. It is important to note that the contact area, A_C, is the surface that the silicide shares with the silicon. It may be the area of the contact window cut, or more, should the interface be roughened by annealing. It has been shown that annealing can cause contouring of the surface region, causing an increase of the contact area of aluminum/silicon contacts [34].



$$R_c = \left(\frac{V^+ - V^-}{I_{out}} \right)$$

$$\rho_c = R_c A_c$$

Figure 2-10. Four-terminal Resistor Structure for Measuring Contact Resistance

2.5 Silicides in MOS Device Applications

Silicides were first introduced into MOS technology in 1977. Tungsten and molybdenum silicide were used for interconnect lines and gate metals by silicidizing polysilicon [35-38]. The incorporation of silicides in MOS technology has reduced the parasitic resistances of the devices and their contacts to the wiring layers, introduced a low-resistance wiring layer at the gate stripe level, promoted further scaling of devices by aiding the fabrication of shallow junctions [39], and increasing device packing density to permit more complex circuits in a smaller area [40,41]. All of these factors increase the speed of integrated circuits by reducing RC delays of the devices and interconnection, and increase yield.

Though molybdenum and tungsten were first examined, their high silicidation temperatures (1000°C and 1100°C, respectively) caused them to be replaced by tantalum and titanium. Titanium has long been the dominant metal for silicides in MOS technologies. It is more tolerant of oxide impurities at the interface with silicon, and its silicide is easily wet chemically etched [42]. In the titanium process, as described in

Section 2.2.2, two anneals are required: a C49 $TiSi_2$ mixing anneal in N_2 at 700°C, followed by a phase finalization anneal in Ar at or above 800°C to produce low resistance C54 $TiSi_2$. Between the anneals, a TiN etch is performed. Cobalt, however, requires only one anneal above 600°C [43]. As thermal budgets of MOS technologies are reduced for shallow junction concerns, cobalt is becoming more popular. However, the silicon surface needs to be more "clean" to produce a uniform cobalt silicide. Processes where bilayers of cobalt atop titanium are being developed to produce thin cobalt silicide films, where any interfacial oxide is gettered by titanium. [42,44,45,46]

For applications and processes where a low thermal budget is required, *e.g.* AMLCDs on glass substrates, titanium is above the thermal limit, and cobalt is at the maximum of the process window (650°C). Other metals, with lower silicidation temperatures may need to be pursued for new processes and their limitations. Nickel is the next candidate, whose silicidation temperatures range from 300°C to 500°C, depending on the phase. Oddly, the lowest resistance phase of nickel, NiSi, formed at 400°C, is not the thermodynamically stable phase. Higher temperature, or long anneals will transform NiSi to $NiSi_2$, which has a significantly higher resistivity [48].

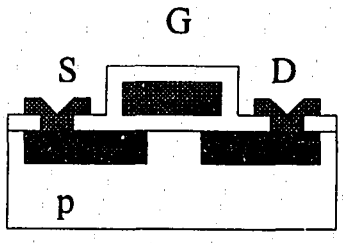
2.5.1 MOS Device Structures Using Silicides

Before the use of silicides, MOSFET devices were constructed as shown in Figure 2-11 (a), with a metal gate and another mask to select diffused or implanted source and drain regions. Since the source and drain contacts are patterned on the same photomask as the gate, there must be a photolithographic and etch spacing between the gate stripe and the source and drain contacts. This long spacing introduces a series resistance between the contact and the channel, R_{SD}. To reduce gate overlap capacitances to the source and drain, refractory metal silicides (Figure 2-11 (b)) were used as the source and drain implant mask. Drawbacks of this technology are many. Patterning the silicide is

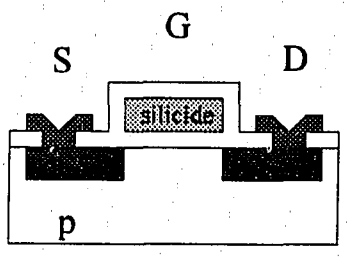
often difficult, as many silicides are relatively chemically resistant. The stress at the silicide/SiO_2 interface translates to an increase in the defect states at the gate dielectric-channel interface [22]. Adhesion of refractory metal silicides to SiO_2 is also a non-trivial concerns, as tungsten in WSi_2 is oxidized, and evaporates at the temperatures encountered in doping anneals [49]. The lithographic spacings between the gate and the source and drain contacts lead to high series resistance. The overlap of the gate to the implanted source and drain regions creates high gate-source and gate-drain capacitances.

Polysilicon gate technology is an alternative to the refractory metals and their silicides for self-aligned source and drain processes. In this process, the polysilicon gate would be doped during the source and drain implant. In CMOS technology this would introduce a pn junction in the polysilicon were it to be used as a wiring layer between nMOS and pMOS devices. Either a metal strap needed to short them together, or the polysilicon would receive a strong implant prior to the source and drain implant step, leading to a counter-doping of the polysilicon gate of one of the device families.

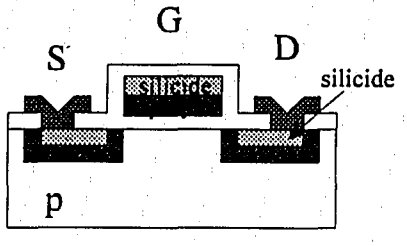
With oxide spacers between the gate stripe and the source and drain regions to selectively mask silicidation, a silicide could be formed simultaneously on the source and drain regions, and the gate stripe, producing a device shown in Figure 2-11 (c). This salicide process, illustrated in Figure 2-12, provides a low series resistance and source and drain contact resistance. Also, the spacers are suited for formation of lightly-doped drain (LDD) regions for the reduction of hot-electron effects. Since all of the gate polysilicon is electrically shorted by the silicide, it can be used as a wiring layer. Unlike the silicide gate process, the polycide gate process leaves silicon atop the gate dielectric. Hence, the separate p and n implants in the CMOS process can be used to adjust the threshold voltages of the devices by controlling Φ_{ms}.



(a) metal gate with implant mask.

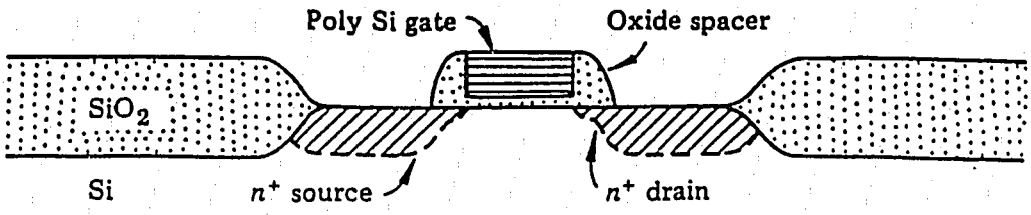


(b) refractory metal silicide gate with self-aligned source and drain implant.

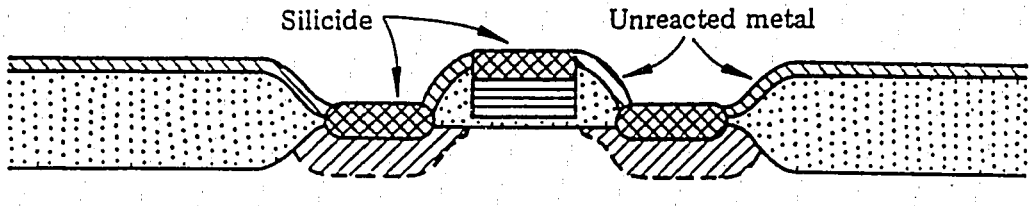


(c) salicide device with silicidized poly gate.

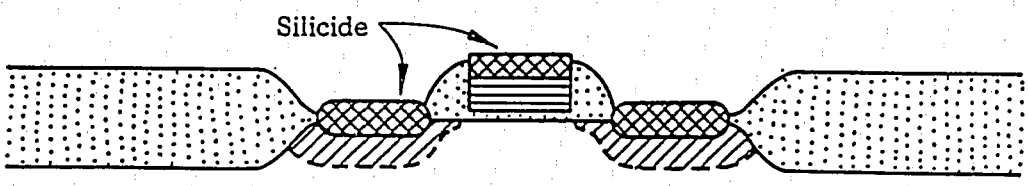
Figure 2-11. MOS Device Structures Using Silicides.



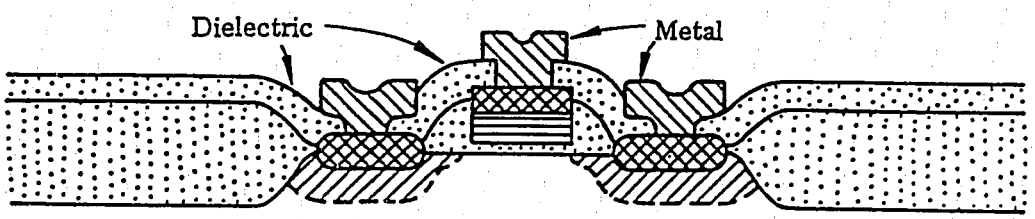
(a) n-channel MOS with poly Si gate.



(b) Deposit metal, anneal to form silicide.



(c) Selectively remove unreacted metal.



(d) Deposit and pattern dielectric layer and metal.

Figure 2-12. Salicide Device Process Sequence. [Maex, 48]

2.5.2 Shallow Junctions

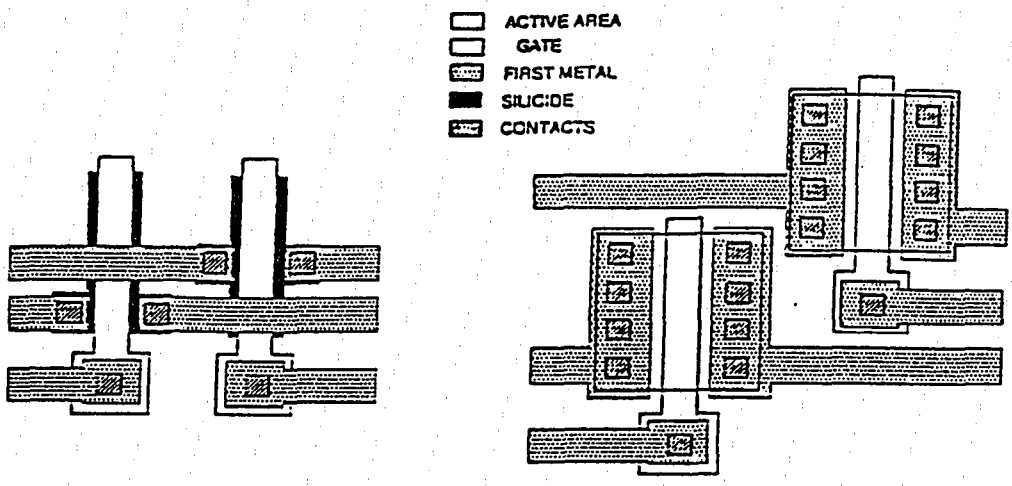
Scaling of devices requires that junction depths be reduced to minimize capacitance. Ion implantation is preferred to diffusion for formation of shallow junctions. A careful treatment of the methods of shallow silicided junction was performed at North Carolina State University [19,20,49]. Methods include implantation through the formed silicide, implantation followed by the activation anneal and the silicidation process, and implanting through the deposited metal film [50], followed by the silicidation and activation anneals. Implanting through the silicide requires a higher energy for the dopant ions, producing an impurity profile with a wide spread. Silicidation after the doping process produced junctions which were pushed by the silicidation anneal both due to thermal rediffusion and by the production of vacancies and interstitials [49,51].

In the case where the dopants are implanted through the deposited metal film before silicidation, the activation anneal and the silicidation anneal is the same thermal step. In this process (SADS), the silicide acts as the diffusion source for the shallow junction. It has been shown that implantation amorphizes the metal-silicon interface, enhancing the silicidation reaction and producing a smoother interface [50,51]. The drawback of this process is that the unreacted metal film is exposed to implantations. Implantation through the metal may induce metal knock-in. And the unreacted metal may oxidize before the silicidation anneal, producing a poor silicide, if any [52].

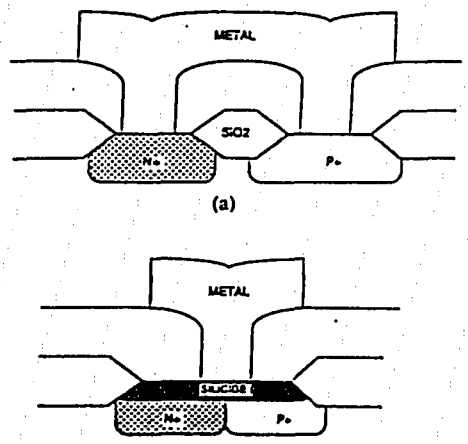
2.5.3 Local Interconnect Technology

If the oxide etch step before silicidation were considered a contact window etch, then silicides can be viewed conceptually as a contacted layer for wiring, while saving one photolithographic step. In conventional metal-contacted source and drain regions, the source and drain must be extended areas for the contact cuts and metal, across the entire width of the active area. With silicides, only a small portion of the silicide needs to

contact the wiring layer to the device region; the nature of the silicide and its formation will provide contact to the entire active area upon which it was formed. A comparison of the area needed to contact conventional metal and silicide-contacted devices is shown in Figure 2-13 (a) [52]. Figure 2-13(b) illustrates the use of silicides to make contacts to other device areas, *e.g.* the output node of a CMOS inverter. This process uses silicides as a "local interconnect," which is used for proximal wiring [51].



(a) Contacts to Device Source, Gate, and Drain.



(b) Local Interconnection of the Output Node (Drains) of a CMOS Inverter.

Figure 2-13. Reduction in Circuit Area by Local Interconnect Process. [Levy, 52]

In Figure 2-14, the local interconnect (LI) process sequence is described [40]. Beginning with the standard CMOS process sequence with spacers, a polysilicon film is deposited and patterned into the local wires. This poly film is to be entirely consumed in the silicidation. Before metal deposition, any oxide on the local interconnect poly and the source and drain regions is etched. After metal deposition, silicide is formed on the source, drain, and gate, and the local interconnect polysilicon has been transformed into a silicide. Note that the "ends" of the LI silicide consume into the source and drain nodes it connects, ensuring a low resistance contact.

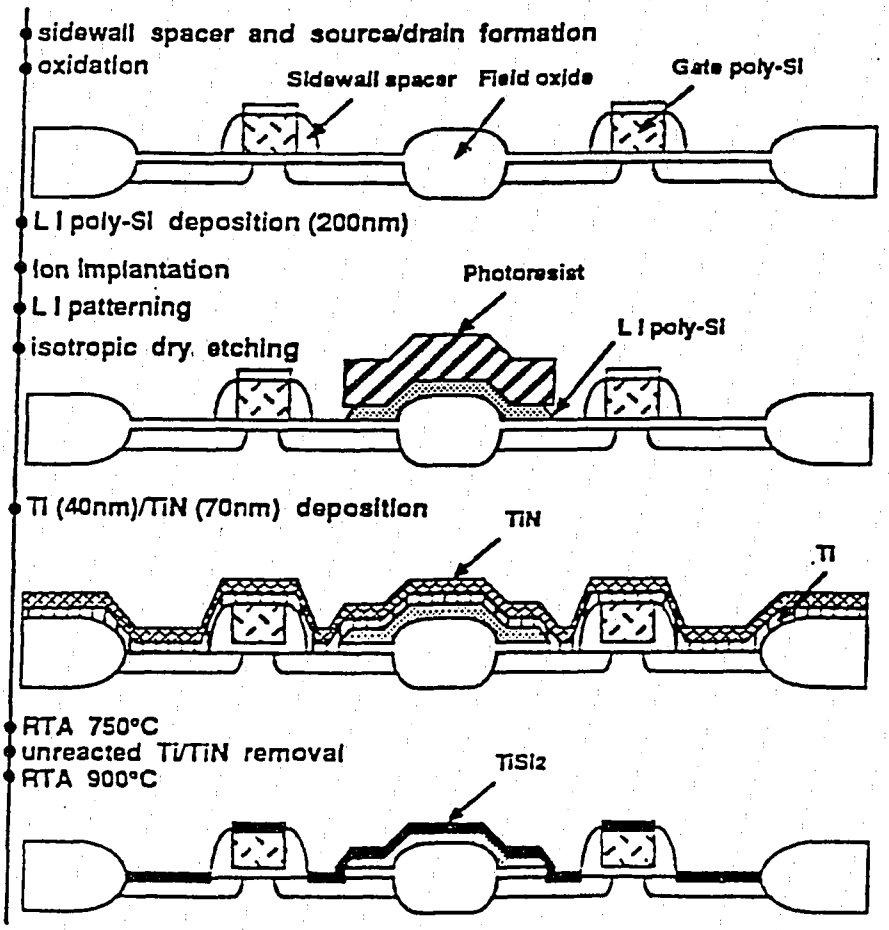


Figure 2-14. Local Interconnect Process. [Hayashida, 40]

2.6 Effect of Series Resistance in MOS Devices

Series resistance at the source and drain, between their contacts and the channel, effect a voltage drop reducing the effective V_{DS}, reducing the current the device delivers. The effective mobility, derived from the transconductance in the linear region and given by equation 2.4, is decreased by the reduction in current.

$$\mu = \frac{L}{W}\frac{g_m}{C_g V_{DS}} \tag{2.4}$$

where the transconductance, g_m, is defined as $\frac{\partial I_{DS}}{\partial V_{GS}}$.

2.6.1 Device Level Model of Resistance

Figure 2-15 shows a resistance model of a MOS device, illustrating the channel, contact, and series resistances. The extrinsic resistance is the sum of the contact resistances and the series resistances of the source and drain, as given by:

$$R_{ext} = 2(R_C + R_{SD}) \tag{2.5}$$

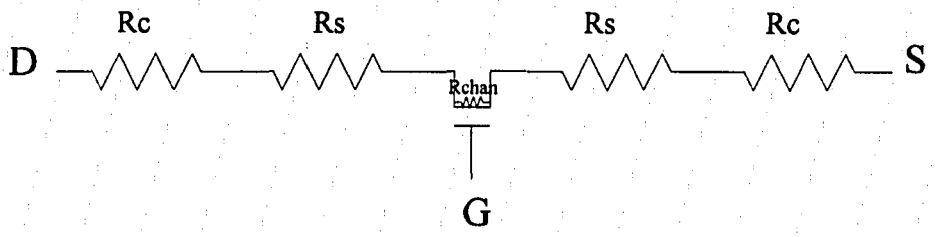


Figure 2-15. Resistances of MOS Device.

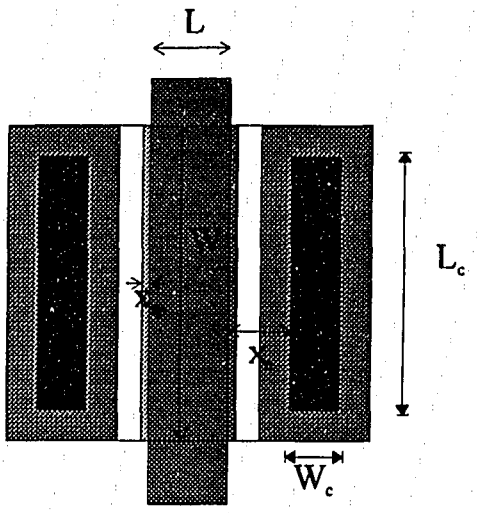


Figure 2-16. Extraction of Device Resistances from Layout

The contact resistance, R_C, is given by equation 2.3. However, the area of the contact is not the entire surface area of the silicided region. It has been shown that in low-resistance contacts, crowding of the current occurs. The transfer length of the contact, L_T, is defined as the length of the contact from the channel which conducts the current. This length is about 1μm in silicided contacts on highly doped silicon [33]. Hence, the contact area is defined by the transfer length and the device width. The series resistance of the source and drain regions, R_{SD}, is given by equation 2.2, with L and W are those of the area between the contact cuts and the channel, as shown in Figure 2-16.

The channel resistance, R_{chan}, is the resistance of the inversion layer. Assuming a uniform sheet of charge under the gate, the channel resistance can be determined by the inversion charge:

$$R_{chan} = \frac{\rho_{chan}}{x_{chan}} = \frac{L}{W}\frac{1}{qn_s\mu_{chan}} \tag{2.6}$$

The channel charge density, n_S ($\frac{1}{cm^2}$), is given by:

$$n_s = \frac{C_{ox}(V_G - V_T)}{q} \tag{2.7}$$

For a device with a gate SiO_2 thickness of 1000Å, a threshold voltage of 2V, and gate voltage of 10V (typical values for a TFT in an AMLCD driver), the channel charge density is $1.75 \times 10^{12}/cm^2$. The channel resistance for a single-crystal device, with mobility μ = 400 cm^2/V-sec, and aspect ratio of 5, is 1786Ω. In a TFT fabricated in thermally recrystallized polysilicon, with mobility μ = 20 cm^2/V-sec, the channel resistance is 35.7kΩ. Without additional resistance limitations imposed by the source and drain, the maximum current this device can deliver at V_{DS} = 10V is 0.28 mA, which may be sufficient for logic operation, but is quite small for display drivers.

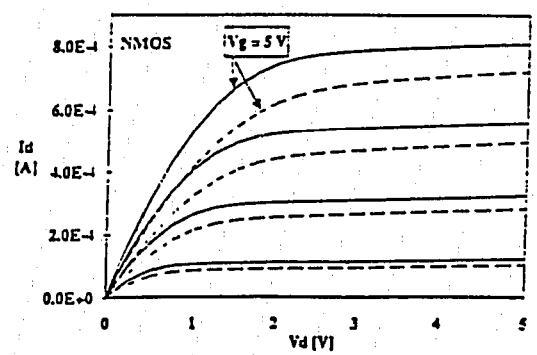
2.6.2 Impact of Extrinsic Resistance on MOS Device Performance

Extrinsic resistance will reduce the device current, thus reducing the derived effective mobility. Reduction of the resistance will increase the current, but a halving of the extrinsic resistance will not double the current, as the channel resistance will be unchanged.

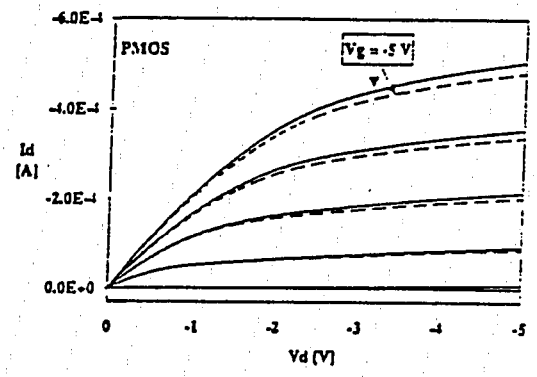
As a comparison, consider device parameters as listed in Table 2-2. The parameters refer to those described in Figure 2-16. The source and drain series resistance of a device without silicides would be 10Ω, whereas a silicided device would exhibit only 0.067Ω. The contact resistances of the non-silicided and the silicided devices would be 10Ω and 11Ω, *resp.* The total extrinsic resistance of the non-silicided device would be 40Ω, and the silicided device only 22Ω. Note that the channel resistance would be 1786Ω in both devices.

$W = 5\mu m$	$W_c = 3\mu m$
$L = 1\mu m$	$L_c = 1\mu m$
$n_{SD} = 10^{20}/cm^3$	$\mu_{channel} = 400\ cm^2/V\text{-}sec$
$\rho_{SD} = 200\ \mu\Omega\text{–}cm$	$\rho_{silicide} = 10\ \mu\Omega\text{–}cm$
$\rho_{c,metal} = 0.3\ \mu\Omega\text{–}cm^2$	$\rho_{c,silicide} = 1\ \mu\Omega\text{–}cm^2$
$x_j = 2000Å$	$x_{silicide} = 500Å$
$x_c = 3\mu m$	$x_{spacer} = 1000Å$
$V_T = 2V$	$x_{ox} = 1000Å$

Table 2-2. Device Parameters for MOS Extrinsic Resistance Values.



(a) nMOS



(b) pMOS

Figure 2-17. Comparison MOSFET Transfer Characteristics with and without Salicide. [Ronkainen, 53]

Although it appears that the reduction in series resistance is negligible in comparison to the channel resistance, the voltage drop associated with the series resistance reduces V_{DS} across the channel. Device current is proportional to the V_{DS} in the linear region, and the square of V_{DS} in the saturation region. Also, the reduction in extrinsic resistance leads to a higher conductance in the linear region. The unequivocal improvement of silicides on nMOS and pMOS device performance is illustrated in Figure 2-17, comparing transfer characteristics with and without salicides [53].

The drain current of a device with series resistance is reduced because of the IR voltage drop between the source and drain contacts and the ends of the channel. For drain bias V_{DS0}, in saturation, the current through a device without series resistance is the ideal I_{DS0}, described in equation 2.8.

$$I_{DS0} \equiv \mu_{eff} \frac{W}{L} C_{ox} (V_{GS} - V_T - \frac{V_{DS0}}{2}) V_{DS0} \tag{2.8}$$

The drop of the drain bias due to series resistance is:

$$V_{DS} = V_{DS0} - I_{DS0} R \tag{2.9}$$

Because $V_{DS0} = V_{GS}-V_T$, the drain current of the series-resistance affected device can be written as:

$$I_{DS} = \mu_{eff} \frac{W}{L} C_{ox} \left(V_{DS0} - \frac{V_{DS0} - I_{DS0} R}{2} \right) (V_{DS0} - I_{DS0} R) \tag{2.10}$$

where R is the series resistance. Equation 2.10 simplifies to

$$I_{DS} = \mu_{eff} \frac{W}{L} C_{ox} \left(\frac{V_{DS0}}{2} - \frac{I_{DS0} R}{2} \right) (V_{DS0} - I_{DS0} R) \tag{2.11}$$

and by negelecting the second-order term, becomes

$$I_{DS} = \mu_{eff} \frac{W}{L} C_{ox} \left(\frac{V_{DS0}^{\ 2}}{2} - \frac{I_{DS0} R V_{DS0}^{\ 2}}{V_{DS0}} \right) \tag{2.12}$$

Using equation 2.8, the decrease from the ideal current due to series resistance can be determined:

$$I_{DS} = I_{DS0} - I_{DS0} \frac{R}{V_{DS0}} \tag{2.13}$$

which can be used to determine the resistance, R:

$$R = \frac{V_{DS0}}{I_{DS0}} \left(\frac{I_{DS0}}{I_{DS}} - 1 \right) \tag{2.14}$$

2.6.3 Impact of Extrinsic Resistance on TFT Devices

Table 2-3 lists polysilicon TFT parameters typical of AMLCD driver devices. The channel resistance is 17.9kΩ. In a non-silicided device, R_{SD} and R_C are 23.5Ω and 2.3Ω, giving a total R_{ext} of 72Ω. (In practice, the resistance values for this device are much higher.) For a salicided device, the series resistance is negligible, calculated to 1μΩ. The contact resistance calculates to 1Ω. Although the channel resistance is much higher than the extrinsic resistances, the silicided device has a higher current as well, as shown in Figure 2-18.

$W = 40\mu m$	$W_c = 32\mu m$
$L = 10\mu m$	$L_c = 4\mu m$
$n_{SD} = 10^{20}/cm^3$	$\mu_{channel} = 40\ cm^2/V\text{-}sec$
$\rho_{SD} = 1.56\ m\Omega\text{-}cm$	$\rho_{silicide} = 10\ \mu\Omega\text{-}cm$
$\rho_{c,metal} = 3\ \mu\Omega\text{-}cm^2$	$\rho_{c,silicide} = 1\ \mu\Omega\text{-}cm^2$
$x_j = 1000Å$	$x_{silicide} = 500Å$
$x_c = 6\mu m$	$x_{spacer} = 1000Å$
$V_T = 2V$	$x_{ox} = 1000Å$

Table 2-3. Device Parameters for polysilicon TFT Extrinsic Resistance Values.

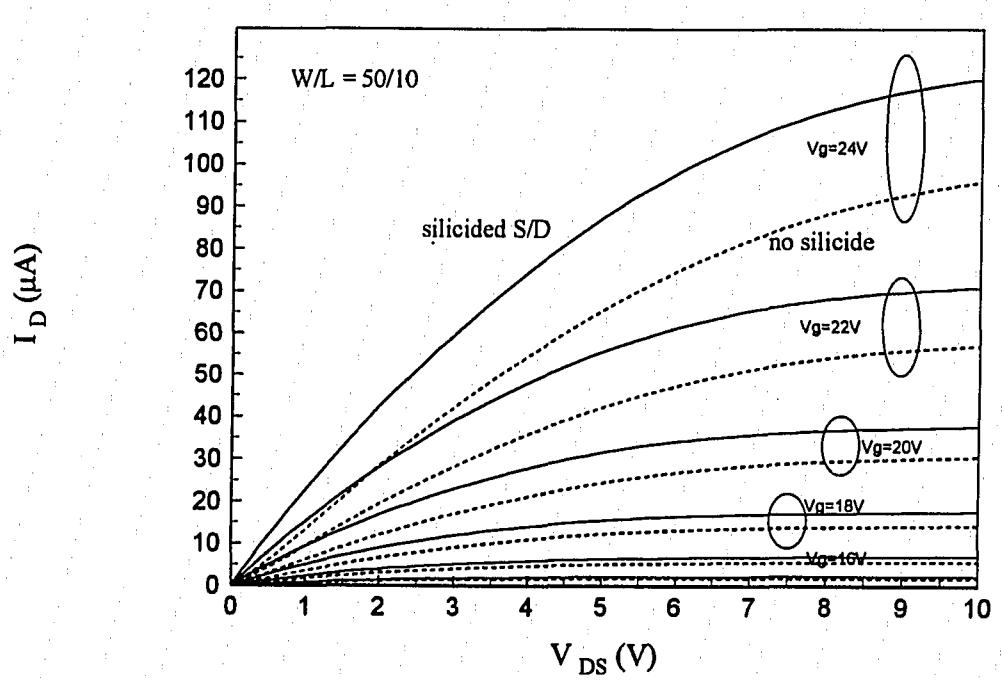


Figure 2-18. Comparison of nTFT Transfer Characteristics with and without Silicided Source and Drain Regions.

2.7 Effect of Silicides in MOS Circuits

Silicides make their primary impact on circuits by: reduction of parasitic resistances at the wiring and device levels; allowing for flexibility in device connection; providing a wiring layer without the need for vias; and reduction of layout area. Wiring and interconnect are becoming the dominant factors in circuit design [40]. As will be shown below, the speed of a circuit is highly dependent on the wiring a signal must travel. Since a signal should traverse as short a wire as possible to maximize speed, routing algorithms have tremendous impact on the speed of the circuit.

The resistance in MOS circuits is composed of contact resistance between devices and the interconnect, via resistance between two wiring layers, and the resistance of the wires themselves. Contact resistance is inverse to the square of the contact area, as shown in Equation 2.3. The contact resistivity between wiring metal (*e.g.* aluminum) and silicide is quite small. Hence, the dominant contact resistance is that to the device. The resistance of a wire, illustrated in Figure 2-19, is described in equation 2.15.

$$R_{wire} = R_s \frac{L}{W} = \frac{\rho_{wire}}{x_{wire}} \frac{L}{W} \tag{2.15}$$

The capacitance of the wire is:

$$C_{wire} = LW \frac{\varepsilon_{ox}}{x_{ox}} \tag{2.16}$$

The RC-delay of the wire is the product of R_{wire} and C_{wire}:

$$\tau_{wire} \equiv (RC)_{wire} = L^2 \frac{\rho_{wire}}{x_{wire}} \frac{\varepsilon_{ox}}{x_{ox}} \tag{2.17}$$

The delay of the wire is dominated by the length, and characterized by the resistivity of the wire. The linear relationship with resistivity is the reason for replacing heavily-doped polysilicon wiring with silicided polysilicon (polycides). The length dependence is the motivation behind local-interconnect silicide. Local interconnect technology permits connection of two nodes without having to go through the upper wiring levels, which involve contact resistances and routing which may significantly increase the true length of the interconnection.

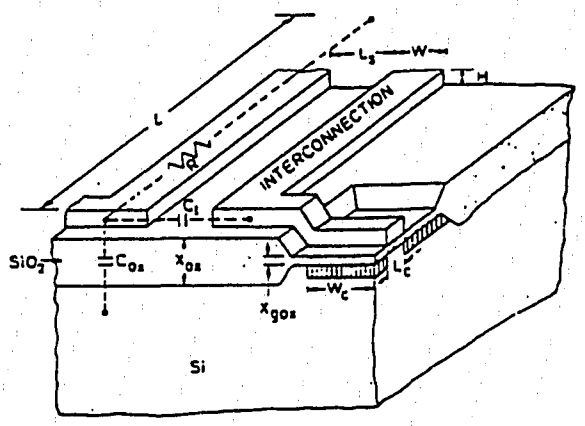


Figure 2-19. Model of a Wire in MOS Circuit. [King, 54]

Although these issues seem directed towards VLSI and ULSI single-crystal silicon CMOS integrated circuits, many of the same considerations of series resistance and wiring apply to their relatively low-complexity polysilicon TFT circuits in AMLCDs. It was shown in section 2.6.2 and 2.6.3 that silicides can improve TFT performance, which would increase the overall speed of the TFT circuit, and the drive capability of display

line drivers. The performance of the display, and the design of the drivers, are highly dependent on the drive characteristics of the TFTs. Reductions in TFT series resistance, *per se*, would increase the effective mobility of the device, reducing the required widths of circuit and driver devices. Width reductions have the added benefit of reducing the gate capacitance, hence again increasing the speed of the circuit. In the next chapter, the silicidation process and characterization of silicides on polysilicon films is described. In the chapters thereafter, device characteristics of TFTs with silicides are analyzed, and compared to devices without silicides.

Chapter 3
Fabrication of Cobalt and Nickel Silicides for Thin Film Transistor Technologies

Cobalt and nickel were explored for their use in TFT technologies because of their glass compatible silicidation temperatures. Cobalt was used for polysilicon TFT devices. Nickel was explored for its use in both polysilicon and amorphous TFT technologies.

3.1 Surface Preparation Technique

The silicidation temperature and electrical characteristics of the resulting silicide are dependent on the preparation of the silicon surface prior to metal deposition. The optimal surface is oxide-free. However, in the fabrication of devices, there is an oxide layer which would retain water. This water could desorb during deposition, providing oxygen to the ambient. This oxygen could oxidize the substrate silicon surface, or contaminate the target surface or deposited metal film.

It has been long known that HF not only removes any oxide from the silicon surface, but passivates it so that it will not be quickly oxidized in atmosphere. It has been observed that isopropanol (IPA) can be used to remove water from substrate surfaces [55,56]. It was found that a prolonged pump down in the load lock, and the main deposition chamber, were required prior to the ignition of argon plasma in order to obtain metal and silicide films with reproducible electrical characteristics.

The effect of the sample preparation was explored by using different preparation methods and substrates, and measuring the sheet resistance of deposited metal film and reacted silicide. To determine the effect of preparation on the deposited metal, blank silicon wafers were used, and the sheet resistance of the deposited layer were measured. After RCA cleaning, the preparation methods of metal-deposition test samples were: no HF-dip; HF-dip followed by DI water rinsing; HF-dip followed by nitrogen blow-drying

(without DI water rinse); and HF-dip followed by DI water rinsing, 1 minute IPA immersion, and nitrogen blow-drying. The HF-dip solution was 25:1 H_2O:HF.

Silicides were grown on substrates with different surface conditions. Blank silicon wafers were used as reference standards. Wafers with 1000Å polysilicon, deposited by SiH_4 at 200mtorr, 580°C, in a CVD reactor, on 1000Å SiO_2 grown by dry oxidation at 1000°C were used as "thick" polysilicon samples. Also, wafers which had a patterned 1μm oxide film grown by wet oxidation simulated the active substrate of an LCD. After RCA cleaning, the samples received HF-dip, followed by one of the following treatments: DI-water rinsing; nitrogen blow-drying; IPA immersion followed by nitrogen-blow-drying. The HF-dip solution was 25:1 H_2O:HF. After silicidation, any remaining metal or metal-rich phases were etched. The sheet resistance was then measured using a four-point-probe setup. The blank silicon wafers had a sheet resistance above the range of the measuring voltmeter (> 4 kΩ/□) and did not reduce the sheet resistance when in contact with the metal or silicide film.

3.1.1 Cobalt Deposition and Silicidation

Cobalt was deposited by RF-sputtering at 250W using a 6" diameter target, in Ar at 9 mtorr. The target-to-substrate distance was 6". The sputter time was 1 min; the deposited film thickness was about 60Å. The sheet resistance of the cobalt film deposited on silicon wafers with different preparation is listed in Table 3-1. The no-HF sample had about double the sheet resistance of the other samples. All samples which were HF-dipped had similar sheet resistance, regardless of the remainder of the preparation. Hence, water rinsing and IPA drying did not affect the purity of the deposited film.

no HF	HF-DI	HF-N_2	HF-DI-IPA-N_2
58	24	22	24

Table 3-1. Sheet Resistance (Ω/□) of Cobalt on Silicon with Different Preparation

The silicide films were formed by in-situ lamp annealing the cobalt-coated samples immediately following deposition, after evacuation of the Ar ambient and without breaking vacuum. The anneal was done for 10 min at 700°C. Remaining cobalt was etched with 3:1 H_2O_2:HCl. The silicide results are listed in Table 3-2. Though all of the samples had similar sheet resistance, there was a difference in the ease of preparation. For the HF-dipped-only sample, the acid was directly blown from the sample. This can be hazardous to the operator, especially for substrates which are nominally hydrophilic, like device wafers, which are mostly oxide-covered. For the methods without IPA drying, the acid or water required prolonged nitrogen drying. The load lock required a lengthy pump-down in order to fully remove any remaining water droplets. However, the IPA-dried samples dried immediately under the nitrogen. This is the most practical for device wafers and display panels because they are hydrophilic. It is important to note that the sheet resistance using this method is similar to the silicon standard. Hence, DI rinsing followed by IPA drying does not degrade the silicidation process.

	HF-DI	HF-N_2	HF-DI-IPA-N_2
silicon blank	12.7	12.9	12.7
patterned oxide	12.6	12.6	11.6
polysilicon			14.6

Table 3-2. Sheet Resistance (Ω/□) of Cobalt Silicide with Different Preparation

The resistance of the polysilicon sample is slightly higher. This may be due to a lack of silicon, producing a M/S ratio less than 2, which would increase the sheet resistance of cobalt silicide as described in the previous chapter. Or, the polycrystalline nature of the silicon may have caused a different physical structure to be formed in the polycide. This issue is further explored in silicidation on thin (1000 Å and 180 Å) polysilicon films, in Section 3.2

3.1.2 Nickel Deposition and Silicidation

Examination of the effects of nickel deposition and silicidation on sample preparation were performed in the same manner as described above. Nickel was deposited by RF-sputtering at 250W using a 6" diameter target, in Ar at 9 mtorr for 2 min. The target-to-substrate distance was 4". The sheet resistance of the nickel film deposited on silicon wafers with different preparation is listed in Table 3-3. The no-HF sample had about triple the sheet resistance of the other samples. All samples which were HF-dipped had similar sheet resistance, regardless of the remainder of the preparation. Hence, water rinsing and IPA drying did not affect the purity of the deposited nickel.

Nickel silicide was formed by in-situ lamp annealing immediately after deposition and evacuation of the Ar ambient. The anneal was 10 min at 400°C. The remaining nickel was etched with 3:1 H_2O_2:H_2SO_4. The sheet resistances of the silicidations are listed in Table 3-4.

no HF	HF-DI	HF-N_2	HF-DI-IPA-N_2
28	9.3	10.1	9.9

Table 3-3. Sheet Resistance (Ω/□) of Nickel on Silicon with Different Preparation

	HF-DI	HF-N_2	HF-DI-IPA-N_2
silicon blank	9.3	9.8	10.2
patterned oxide	9.3		9.3
polysilicon			9.9

Table 3-4. Sheet Resistance (Ω/□) of Nickel Silicide with Different Preparation

Again, the metal deposition without HF-dip was higher. The HF-dipped substrates all gave nickel films with about 10Ω/□ sheet resistance. The nickel silicides showed that the HF-DI-IPA-N_2 preparation method produces a low sheet resistance silicide with easy processing. That the values of the silicide and the metal are similar is coincidence. The nickel metal was thoroughly etched from the silicided samples; the oxide-covered regions of the patterned substrate showed infinite sheet resistance, or, absence of any nickel layer.

3.2 Cobalt Silicidation Process

Cobalt silicide was examined for temperatures equal to and below 700°C. Silicides were prepared on single-crystal silicon wafers and polysilicon layers on SiO_2. The polysilicon layers were deposited by CVD, with film thicknesses of 1000Å and about 180Å. The fabrication process was RCA cleaning, followed by 25:1 H_2O:HF dip for 30 sec after the silicon surface became hydrophobic, DI water rinsing, IPA immersion for 1 min, then nitrogen blow-drying immediately prior to loading into the load-lock of the sputtering system. The load lock was pumped down to 100 mtorr by mechanical pumps, then to 60 μtorr for 5 min with a cryopump. The sample would then be loaded into the main chamber of the sputtering system, where it would be pumped down via the cryopump to less than 1μtorr, or 5 min, whichever was longer. Then, the RF Ar plasma would be ignited, and the target pre-sputtered at 250W for 5 min at 9mtorr. Cobalt would be sputtered onto the sample for 1 min (60Å), except for the samples where the effect of cobalt film thickness was examined-- these samples were sputtered to thicknesses of 15 and 30 Å. After sputtering, the plasma was extinguished, and the Ar evacuated. When the pressure was below 1μtorr, the sample was in-situ lamp-annealed for 10 to 30 min. over temperatures ranging from 600 to 700°C. After cooling in N_2 in the load lock, the samples were removed and were etched in 3:1 H_2O_2:HCl. The sheet resistance was then measured using a four-point probe setup.

The effect of silicidation temperature on the sheet resistance of cobalt silicide formed on single-crystal and polycrystalline silicon is shown in Table 3-5. For 10 min. anneals, the transition temperature from the monosilicide to the disilicide phase is at 650°C. However, the disilicide phase is fully realized at 600°C when annealed for 30 min. The thick (1000Å) polysilicon sample has only a slightly higher sheet resistance than the single-crystal sample. The thin (180Å) polysilicon sample, annealed at 700°C, showed again a slightly higher resistance.

T (°C)	x-Si	1000Å poly-Si	180Å poly-Si
600	216 (13.4)	268 (13.2)	
650	13.2	13.5	
700	12.5	14.6	16.6

Anneal Time = 10 min, (30 min).

Table 3-5. Effect of Temperature on Cobalt Silicide Sheet Resistance.

To determine whether the polysilicon samples were bordering on silicon-rich silicides as an explanation for their higher sheet resistances, thinner cobalt films were deposited. Cobalt was sputtered for 15 and 30 sec, corresponding to about 15 and 30Å-thick films. The films were annealed at 700°C for 10 min. The sheet resistances are listed in Table 3-6. Note that the 15Å cobalt sample for crystalline silicon showed high error. This condition was run thrice to determine the reproducibility of the sputter and anneal, considering the unexpected difference in values for the thick and thin polysilicon sample. The conclusion must be that the short sputter at the low sputter rate does not put a continuous and reproducible film of cobalt on the substrate. However, the 30Å cobalt sputter did provide useful results; the values were about twice those of the 60Å sputter (repeated), indicating a film of half the thickness. Note that the single-crystal and thick

polysilicon samples converge on sheet resistance, though the thin polysilicon sample is still slightly higher.

It had been observed that a thin polysilicon sample would "dissolve" into the silicide if the cobalt film were too thick, and the entire film would be removed in the cobalt etch. Since this did not happen in the 1 min. cobalt on thin polysilicon sample, it seems reasonable that there is not excessive silicon in the 30Å cobalt on thin polysilicon sample, and certainly to neither of the thick polysilicon samples. Hence, the increased sheet resistance is due to structural differences of polysilicon, not silicon supply to the silicidation reaction. This explains the increased sheet resistance of silicides on polysilicon in Table 3-2.

	Cobalt thickness		
	15 Å	30 Å	60 Å
180Å poly Si	141	30.4	16.6
1000Å poly Si	72	24.8	14.6
single-crystal Si	94, 115,.134	24.4	12.5

Table 3-6. Effect of Cobalt Thickness on Sheet Resistance (Ω/□) of Cobalt Silicide

The $CoSi_2$/Si contact resistivity was measured using the transmission-line and Kelvin resistor methods described in the previous chapter. The extrapolated contact resistance in the transmission-line structure was 15.2Ω, with the contact area 50x10μm^2, giving a contact resistivity, ρ_c, of 76 $\mu\Omega$-cm^2. The contact resistance of the 25x25 μm^2 contact area of the Kelvin resistor was 12.9 Ω, giving a contact resistivity of 81$\mu\Omega$-cm^2.

3.3 Nickel Silicidation Process

3.3.1 Nickel Silicide for Polysilicon TFT Technology

Nickel silicide was examined for temperatures ranging from 250°C to 600°C, where the sheet resistance was found to increase due to the transition to the monosilicide phase [47]. Silicides were prepared on single-crystal silicon wafers and polysilicon layers on SiO_2, in the same manner as described for cobalt silicidations. Nickel was RF-sputtered from a 6" diameter target at 250W in 9 mtorr Ar. Nickel was sputtered to a thickness of 86Å, except for the samples where the effect of nickel film thickness was examined--these samples were sputtered to 43Å. After sputtering, the plasma was extinguished, and the Ar evacuated. When the pressure was below 1μtorr, the sample was in-situ lamp-annealed for 10min. over temperatures ranging from 250 to 600°C. After cooling in N_2 in the load lock, the samples were removed and were etched in 3:1 H_2O_2:H_2SO_4. The sheet resistance was then measured using a four-point probe setup.

Figure 3-1 shows the sheet resistance values of nickel silicides on various substrates formed by nickel sputtering, followed by 10 minute anneals. The nickel silicide film exhibited the low-resistance monosilicide phase in the temperature range from 400 to 500°C, with values of 8.4 and 8.7 Ω/□ for single-crystal silicon, and 7.9 and 8.2 Ω/□ for thick polysilicon. The dinickel phases are evident at 250 and 300°C. At 600°C, the disilicide phase transition is evident from the increased resistivity. Table 3-7 shows the effect of nickel thickness on the resulting silicide on different substrates.

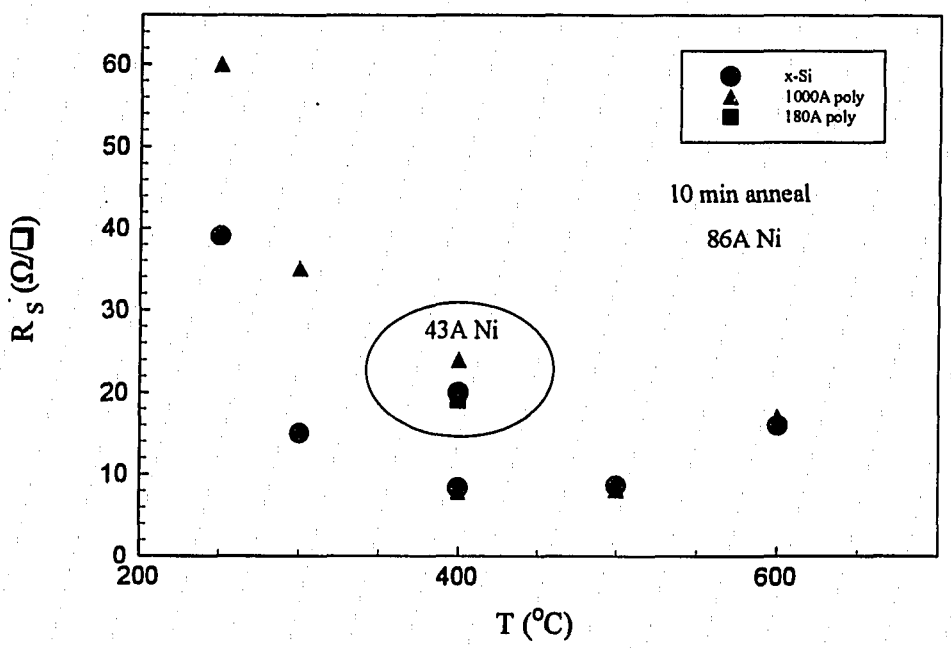


Figure 3-1. Effect of Temperature on Nickel Silicide Sheet Resistance.

	Nickel thickness	
	43Å	86Å
180Å poly Si	24	
1000Å poly Si	20	7.9
single-crystal Si	19	8.4

Table 3-7. Effect of Nickel Thickness on Sheet Resistance (Ω/□) of Nickel Silicide

The sheet resistances of the polysilicon samples showed a greater dependence upon the silicidation temperature compared to the single-crystal samples, and was typically higher. The thin (180Å) polysilicon sample showed a significantly higher sheet resistance than the thicker polysilicon and the single-crystal silicon samples. Since there was a strong substrate-dependence on the silicide, there may be a silicon *vs.* nickel supply concern in forming the low-resistance monosilicide, especially since it is the higher-resistance disilicide phase which is thermodynamically stable in the Si-Ni system [47].

In cobalt, a lack of silicon supply to the M/S ratio increases the sheet resistance because the lowest-resistance phase is the disilicide (M/S = 2). However, the nickel monosilicide phase has the lower resistivity. If there were a lack of silicon, it would appear as an excess of nickel when forming nickel monosilicide. The excess nickel of the 86Å samples would produce either unreacted nickel or a nickel-rich alloy, both of which would be etched. To determine whether there was nickel or nickel-rich alloy on the surface, the sheet resistance of the films when measured before etching. The measured sheet resistances were unchanged by the etch, indicating that there was not an excess of nickel. Hence, either the polycrystalline nature of the thin silicon samples is the cause of the increased sheet resistance.

The contact resistivity of the nickel silicide to polysilicon was measured using the transmission-line and Kelvin resistor methods described in the previous chapter. The transmission line method gave a contact resistance of 12.7Ω, indicating a contact resistivity of 80 $\mu\Omega$-cm^2. The Kelvin resistor method gave a contact resistance of 6.4 to 9.3 Ω, indicating contact resistivities of 40 to 58 $\mu\Omega$-cm^2. The difference in the values can be attributed to the contouring of the contact, possibly at grain boundaries, which can aid metal atom diffusion. These structures have been found to provide differing values for a given contact system for this reason, among others including direction of current flow and geometry of the contact [33].

The specific contact resistivity, ρ_i, is a measure of the contact resistivity, though is often less than ρ_C [57]. The specific contact resistivity is defined as:

$$\rho_i \equiv \left.\frac{\partial V_c}{\partial J}\right|_{V_c=0} \tag{3.1}$$

where V_C is the contact voltage, and J is the current density through the contact. For high doping levels, the current is tunneling dominated, and the specific contact resistivity can be written as:

$$\rho_i = \frac{k}{TA^*} e^{\frac{2\sqrt{m^* \varepsilon_s}}{\hbar} \frac{\Phi_B}{\sqrt{N_D}}} \tag{3.2}$$

where $A^* = 100\ A/cm^2K^2$, the Richardson constant.

Assuming that the electrically active concentration of phosphorous is saturated due to the $POCl_3$ diffusion process, $N_D = 3x10^{20}/cm^3$ [58].

The specific contact resistivities for aluminum, cobalt silicide, and nickel silicide on highly-doped n-type silicon are compared to the measured contact resistivities in Table 3-8. The trend supports the analysis, where the contact resistivity decreases as a function of contact barrier height, also listed in Table 3-8.

	barrier height	single-crystal Si	polysilicon
metal	Φ_B (eV)	ρ_i ($\mu\Omega$–cm^2)	ρ_C ($\mu\Omega$–cm^2)
Al	0.72	6.03	4000 [34]
$CoSi_2$	0.64	2.58	77 ± 2
NiSi	0.4	0.202	50 ±10

Table 3-8. Comparison of Theoretical to Measured Contact Resistivities

3.3.2 Nickel Silicide on Amorphous Silicon and Silicon-Germanium for a-TFTs.

Because nickel silicides can be formed at temperatures compatible with amorphous TFT technologies, nickel silicidation was attempted on amorphous silicon and silicon-germanium (20 at%Ge) films with thickness averaging 600Å. The external resistance of amorphous TFTs is extremely high, as will be shown in Chapter 4; reduction of parasitic resistance by incorporation of silicides may improve device performance.

Amorphous silicon and silicon-germanium (20 at%Ge) samples were 3:1 H_2O_2: H_2SO_4 cleaned for 10 min, followed by 25:1 H_2O:HF dipping for 30 sec, 1 min. immersion in IPA, and nitrogen blow-drying. Nickel was sputtered using the same conditions as the single- and polycrystalline samples, to thickness of 43Å only. Samples were annealed for 10 and 30 minutes at 250 and 300°C. The samples were nickel-etched in 3:1 H_2O_2: H_2SO_4 for 30 sec. after cooling. The sheet resistance was then measured using a four-point probe setup.

The sheet resistances of the nickel silicides formed on amorphous silicon and silicon germanium are listed in Table 3-8. Compared to the silicon sample, germanium inhibited silicidation at 250°C, and slowed down the silicidation reaction at 300°C. The sheet resistances of the nickel silicides (which may be nickel germanosilicides) after 30 min. annealing is less than twice those of the minimum resistance of the nickel silicide annealed at 400°C. The resulting low-resistance silicides of nickel on amorphous silicon and silicon germanium may be useful for amorphous TFT technology. The reduction in the series resistance may improve TFT performance by increasing the drive current, potentially increasing the viability of amorphous TFTs for integrated drive circuitry.

	250°C	
	10 min	30 min
a-Si:H	76	15
$a\text{-}Si_{0.8}Ge_{0.2}$	57	43
	300°C	
	10 min	30 min
a-Si:H	21	11
$a\text{-}Si_{0.8}Ge_{0.2}$	57	14

Table 3-9. Sheet Resistance (Ω/□) of Nickel Silicide on Amorphous Silicon and Silicon-Germanium

3.4 Conclusions

Using a fabrication procedure applicable to TFT and AMLCD processing, low-resistance silicides of cobalt and nickel were fabricated on polysilicon with thicknesses as low as 180Å with sheet resistances as low as 24 Ω/□. Films with lower resistances were formed on thicker polysilicon samples: 8 Ω/□ NiSi, and 14.6 Ω/□ $CoSi_2$. The structure, and possibly the thickness, of the silicon underlayer affects the sheet resistance of the reacted cobalt silicide. With nickel silicides, the structure did not impact the silicide sheet resistance in the monosilicide phase. There may be a thickness-limitation effect on the nickel silicide, when compared to films formed on single-crystal silicon substrates. The contact resistances of the cobalt and nickel silicides to doped polysilicon smaples were lower than aluminum contacts to the polysilicon.

Nickel silicides were also formed on amorphous silicon and silicon germanium at temperatures compatible with amorphous TFT technology (≤ 300°C). Although germanium inhibited the silicidation reaction, low-resistance nickel silicide films were formed at 300°C after 30 min. annealing. The nickel silicide on amorphous silicon has a sheet resistance which is low, 11 Ω/□, and may enhance amorphous TFT device performance.

Chapter 4
Amorphous Silicon and Silicon-Germanium Thin Film Transistors

4.1 Introduction

Amorphous thin film transistors are compatible with the low temperature processing requirements of commercial glasses [59]. Amorphous thin film transistors are typically formed by deposition of n^+ layers for source and drain contact areas, as shown in Figure 1-1. This device structure is suitable for bottom-gate devices. However, bottom-gate structures are not as compatible with circuit technologies as top-gate structures, where the source and drain regions are formed by ion implantation. The deposited contact layer may also exhibit an interfacial layer, which has been shown to produce poor device performance [54]. Recently, amorphous silicon TFTs have been implemented to construct integrated drivers; however, the low hole mobilities limit the circuit architecture to nMOS design [6,60]. Circuits built using nMOS design are slower and dissipate more power.

Although amorphous silicon is already in use for displays, amorphous silicon-germanium has many proposed advantages over amorphous silicon. Dopant impurities are activated faster in silicon-germanium [61]. The bandgap is tunable by the content of germanium, making the material useful for solar cells [62] and image sensors [63]. Amorphous silicon-germanium is more resistant to light-induced defects than amorphous silicon (Staebler-Wronski effect) [61], and exhibits a lower density of bandgap states [64]. The hole mobility in silicon-germanium is higher than in silicon [32,54].

This Chapter will explore the use of amorphous silicon and silicon germanium transistors for driver devices using a top-gate structure, where the source and drain regions are formed by ion implantation would would eliminate interfacial resistances of a

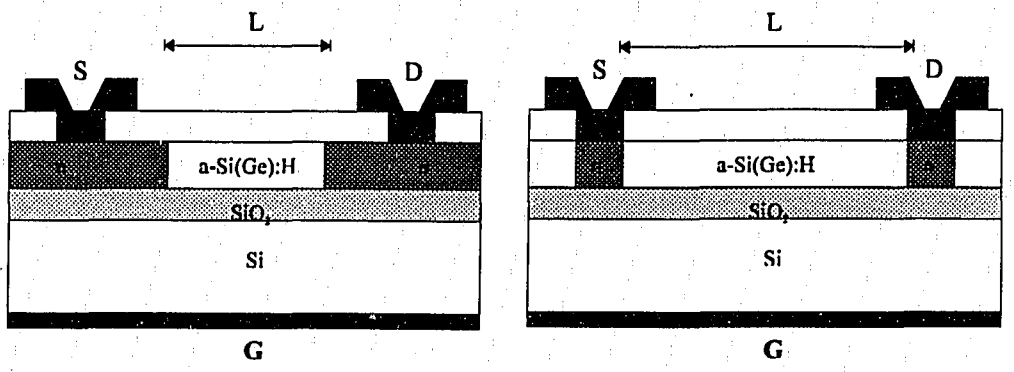
contact layer [54], and permit the use of standard single-crystal CMOS design techniques and the incorporation of self-aligned silicides as described in the previous chapter. The effect of time and temperature of the activation anneal is examined. Thin film transistors are compared by their subthreshold swing, threshold voltage, electron saturation mobility, and the ON-OFF currents and their ratio. The mobility is then corrected for external resistance and channel length effects using three correction methods.

4.2 Fabrication Process

Hydrogenated amorphous silicon and silicon-germanium films of various alloy content were deposited by plasma-enhanced chemical vapor deposition on p-type silicon substrates having 1000Å thermally-grown SiO_2. The average film thickness was 600Å. With photoresist on the device side, the back oxide was etched in HF since the substrate served as the gate electrode, as shown in Figure 4-1. Islands were defined by plasma etching in SF_6. The source and drain regions were doped by ion implantation while the channel region was protected by photoresist. Two device structures were fabricated as a result of the implantation mask. In one structure, the implant was masked by a gate-stripe to define the source and drain regions which extend beyond the metal contacts, providing channel lengths of 5, 10, and 20 μm. Figure 4-1(a) shows this "SD" structure. In the other device structure, the implant is through the contact-window mask, providing for channel lengths of 40 and 56 μm. Figure 4-1(b) shows this "CW" structure. Phosphorous was implanted with a dose of $2x10^{15}/cm^2$ and energy of 30 keV. The resist was removed in oxygen plasma. The samples were then cleaned in 5:1 H_2O_2 : H_2SO_4 for 10min, DI water rinse, followed by 5:1:1 H_2O - H_2O_2 - HCl for 5 min, and a DI water rinse.

In the first phase of the study, devices were annealed in forming gas to determine optimal conditions for the implant activation and post-metal annealing conditions as a

function of germanium content [65]. Also, optimal post-metal annealing conditions were determined for the devices. Since the samples were to be repeatedly annealed, measured, recleaned, and annealed, the measurements were made without metallization. Once optimal conditions were found, metallization was performed by evaporation of aluminum after cleaning and an HF-dip. The second phase of the study, device performance, was then performed, as described in sections 4.4 through 4.6.



(a) SD: Source-Drain Implant (b) CW: Contact Window Implant

Figure 4-1. Amorphous TFT Structures in Ion Implantation Study

4.3 Implant Activation

Activation of impurities implanted into amorphous silicon has been observed to be less than 10% [66]. Two tests were required to determine optimal implant annealing: temperature and duration. The 15 at%Ge sample was used to determine the optimal anneal temperature. All three of the samples were used to determine the optimal time as a function of germanium content.

4.3.1 Anneal Temperature

A 15 at%Ge sample was annealed at 260°C, 300°C, 350°C, and 400°C. The effect of temperature on the device was monitored by changes in the saturation mobility, subthreshold swing, and threshold voltage. The methods for measurement are described

in section 4.4. The threshold voltages for annealing at 300°C was above 20V, and for annealing at 350°C, was above 25V. These voltages were considered too high to provide useful devices. The sample annealed at 400°C gave no device action. Thus the optimal anneal temperature was determined to be 260°C. The device parameters for annealing at 260°C are tabulated in Table 4-1.

	15 min	30 min	60 min	120 min
μ (cm^2/V-sec)	$5.7x10^{-4}$	$9.4x10^{-4}$	$2.3x10^{-4}$	$1.5x10^{-4}$
V_T (V)	14	17	18	19
S (V/dec-A)	4.5	4.4	4.1	4.4

Table 4-1. Parameters for Activation Anneal Optimization at 260°C

4.3.2 Anneal Duration

Activation was compared by sheet resistance, measured by the transmission-line method, described in Chapter 2, illustrated in Figure 2-9. Before annealing, the sheet resistances of the implanted regions were above 1GΩ/□ in all samples. Samples were annealed at 260°C for up to 6 hours in forming gas. The results are shown in Table 4-2.

The silicon-germanium sample achieved minimum sheet resistance before the silicon sample. However, the ultimate resistance of the silicon-germanium sample is higher than the silicon sample. The silicon-germanium sample was not annealed for longer than 1h because the device performance degraded significantly. The silicon sample showed improvements in activation until after 4h. The minimum sheet resistance for the silicon sample was 38 kΩ/□, and for the silicon-germanium sample was 80 kΩ/□, but for the conditions to give optimal device performance was 87 kΩ/□.

	15 min	30 min	60 min	4 h	6 h
a-Si:H	86k	47k	38k	30k	130k
a-$Si_{0.75}Ge_{0.25}$:H	101k	81k	80k	------ poor devices ------	

Table 4-2. Sheet resistances (Ω/□) of Implanted Amorphous Silicon and Silicon-Germanium Material Annealed at 260°C.

4.3.3 Contact Sinter

The contact sinter was based on the I(V) characteristic of the metal contact. The silicon sample required 1 hour of annealing at 260°C to form an ohmic contact. Using the four-terminal resistor structure described in Chapter 2, the Al/n^+ a-Si:H contact resistivity was determined to be 2.4×10^{-3} Ω-cm^2. The silicon-germanium samples required 30 minutes to form an ohmic contact. The measured contact resistivities were determined to be 0.63 and 0.8 Ω-cm^2 for the 15 at%Ge and 25 at%Ge devices. The contacts were not annealed longer, since 30 min was determined to be the maximum anneal time permissible for the SiGe devices before degradation.

4.4 Device Measurement

Device measurement was used to compare annealing conditions to consider the contrasting effects of implant activation and hydrogen loss. The threshold voltage and mobility were measured in saturation, from the $\sqrt{I_D(V_{GS})}$ characteristics where $V_{DS} = V_{GS}$, as shown in Figure 4-2. The mobility was calculated from the maximum slope:

$$\mu_{sat} = \frac{\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2}{C_{ox}}\left(\frac{2L}{W}\right) \qquad (4.1)$$

The threshold voltage was determined by the voltage-intercept of the line extended from the tangent used to determine the mobility.

The subthreshold swing was measured from the $\log(I_D(V_{GS}))$ characteristic, with V_{DS} = 10V, as shown in Figure 4-3.

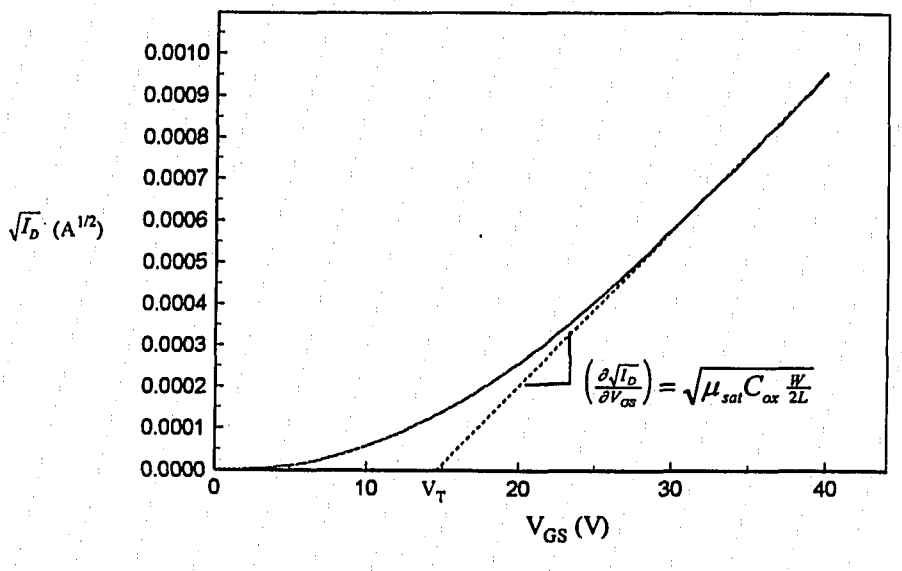


Figure 4-2. Saturation Characteristic to Measure Mobility and Threshold Voltage.

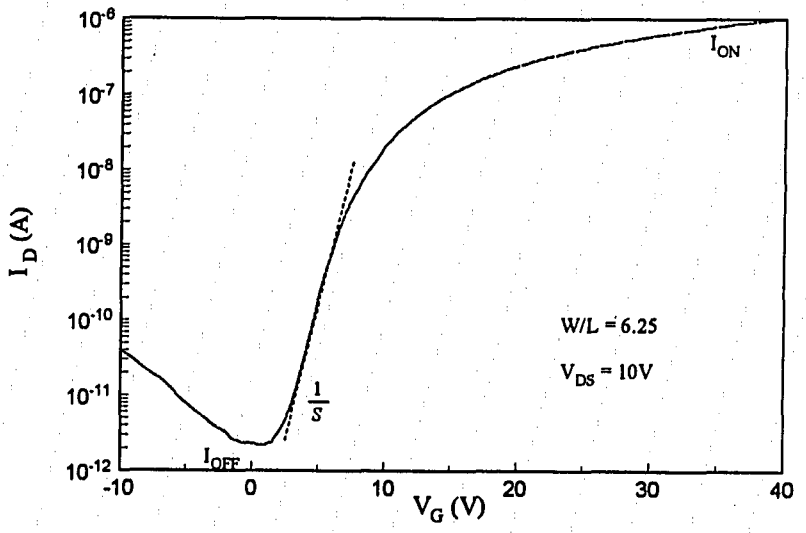


Figure 4-3. Subthreshold Swing Measurement from On-Off Curve.

The parameters of mobility, threshold voltage, and subthreshold swing were determined for each concentration of germanium, and either device structure, over a range of time at 260°C.

4.4.1 Source-Drain Implant Structure

The silicon sample required annealing of 4h to achieve maximum mobility of 0.012 cm^2/V-sec. The threshold voltage began to rise at 4 h. From short annealings, where the value was around 5V, it rose to 10V at 2h, then to 12V for 4h and longer. The subthreshold swing dropped to a minimum of 1.5 V/dec-A at 4h. The curves for the parameters as a function of annealing time are shown in Table 4-3.

The 15 at%Ge sample reached peak mobility of $9.4x10^{-4}$ cm^2/V-sec in only 30 min. The threshold voltage remained high, around 18 - 20V throughout the anneals. The subthreshold swing remained nominally unchanged, around 4.5 V/dec-A. The results are shown in Table 4-4.

The 25 at%Ge sample mobility remained nominally constant for anneals up to 1h, but the threshold voltage rose dramatically after 30 min. The data are shown in Table 4-5. Since this trend of time-dependence was common to both SiGe samples, the optimal annealings for the alloy samples was thus determined to be 30 min.

The effect of the anneal can be seen from the ON-OFF device characteristics as a function of time. Figures 4-4 and 4-5 show the dependence on device performance as a function of annealing time and concentration of germanium.

anneal time (min)	μ_{sat} (cm^2/V-sec)	V_T (V)	S (V/dec-A)
15	$4.7x10^{-4}$	5.3	2.0
30	$8.6x10^{-4}$	4.5	2.3
60	$1.9x10^{-3}$	5.4	2.2
120	$3.5x10^{-3}$	9.8	2.0
240	$1.2x10^{-2}$	12.6	1.5
360	$5.8x10^{-3}$	11.6	2.9

Table 4-3. Annealing Dependence of Mobility in a-Si:H TFT, SD Structure.

anneal time (min)	μ_{sat} (cm^2/V-sec)	V_T (V)	S (V/dec-A)
15	$5.7x10^{-4}$		
30	$9.4x10^{-4}$	20.8	4.4
60	$2.3x10^{-3}$	17.5	4.1
120	$1.5x10^{-3}$	18.9	4.6

Table 4-4. Annealing Dependence of Mobility in a-$Si_{0.85}Ge_{0.15}$:H TFT, SD Structure.

anneal time (min)	μ_{sat} (cm^2/V-sec)	V_T (V)	S (V/dec-A)
15	$5.7x10^{-4}$		
30	$9.4x10^{-4}$	20.8	4.4
60	$2.3x10^{-3}$	17.5	4.1
120	$1.5x10^{-3}$	18.9	4.6

Table 4-5. Annealing Dependence of Mobility in a-$Si_{0.75}Ge_{0.25}$:H TFT, SD Structure.

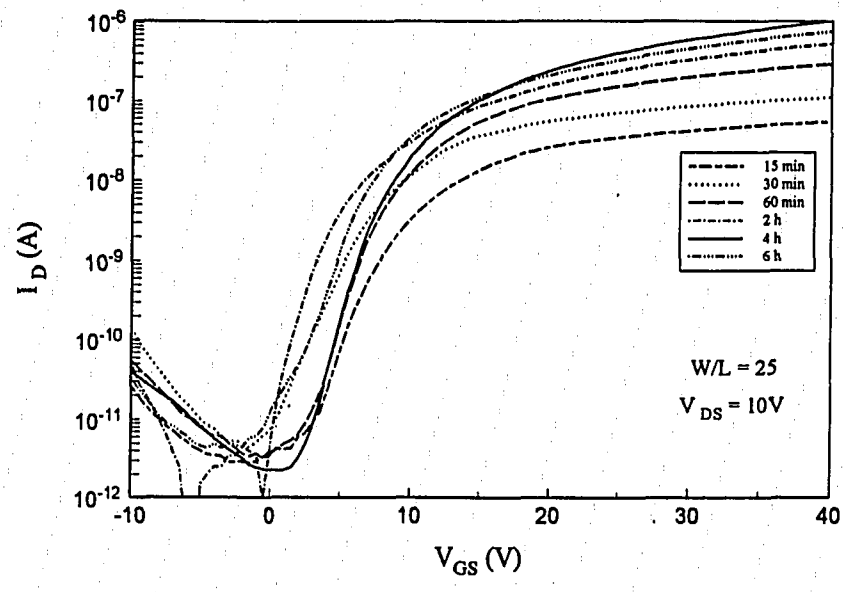


Figure 4-4. Effect of Annealing on a-Si:H (SD) TFT Performance.

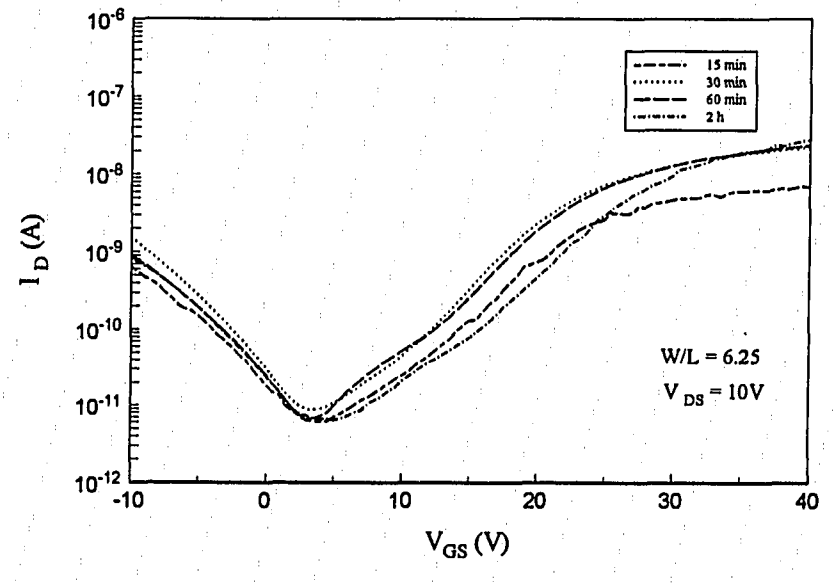


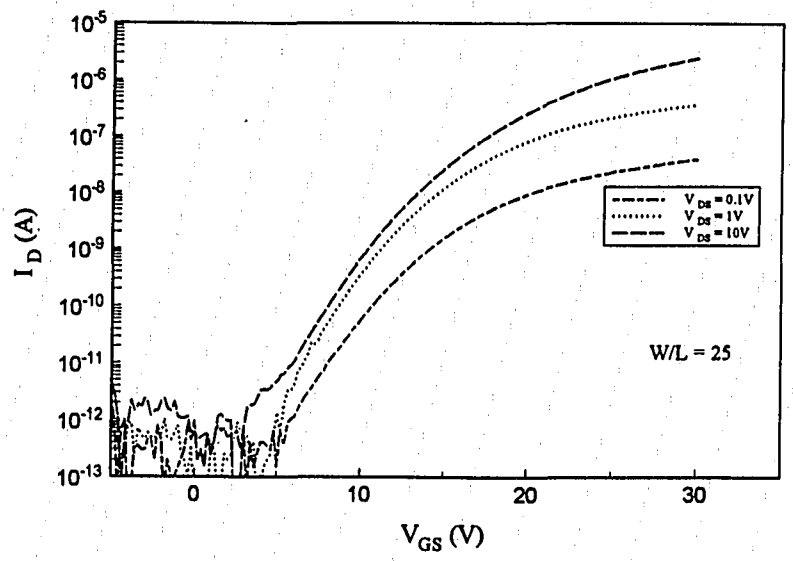
Figure 4-5. Effect of Annealing on a-$Si_{0.75}Ge_{0.25}$:H (SD) TFT Performance.

Because the silicon sample showed optimal performance with 4 h of annealing, it was annealed 3h after implantation, then another hour after metallization. Since the silicon-germanium samples required 30 min to form an ohmic contact, and the device characteristics degrade upon further annealing, metallized silicon-germanium samples were prepared by annealing once, after the aluminum evaporation, for 30 minutes. These "optimized" metallized device characteristics are shown in Figures 4-6 through 4-8 for each of the concentrations of germanium. In Figure 4-9, the device performance is compared directly as a function of germanium content.

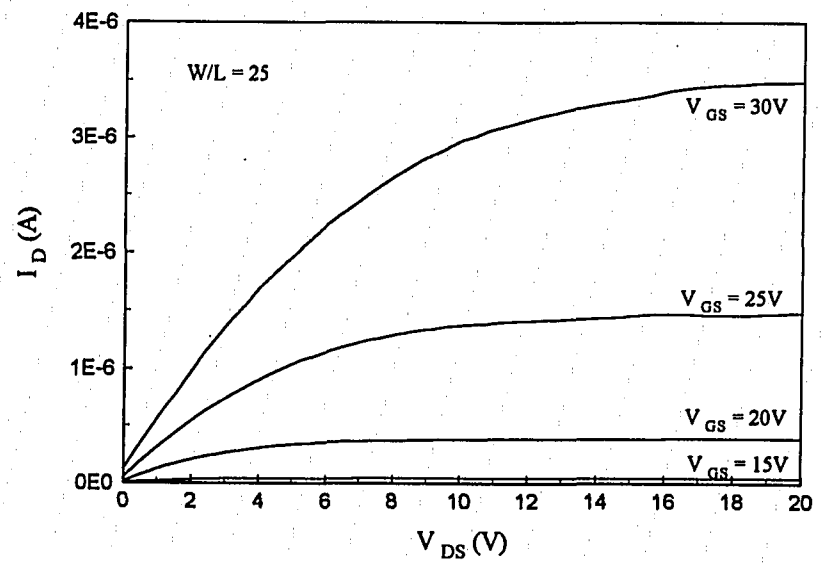
The mobility, threshold voltage, and subthreshold swing of optimized, metallized SD-structure devices for each of the germanium concentrations is given in Table 4-6. Note that the mobilities are much higher than those of the anneal-test devices.

%Ge	μ_{sat} (cm^2/V-sec)	V_T (V)	S (V/dec-A)
0	0.0378	14.1	1.8
15	1.18×10^{-3}	21.3	3.7
25	1.1×10^{-3}	26.5	7.0

Table 4-6. Optimized Metallized (SD) TFT Parameters.

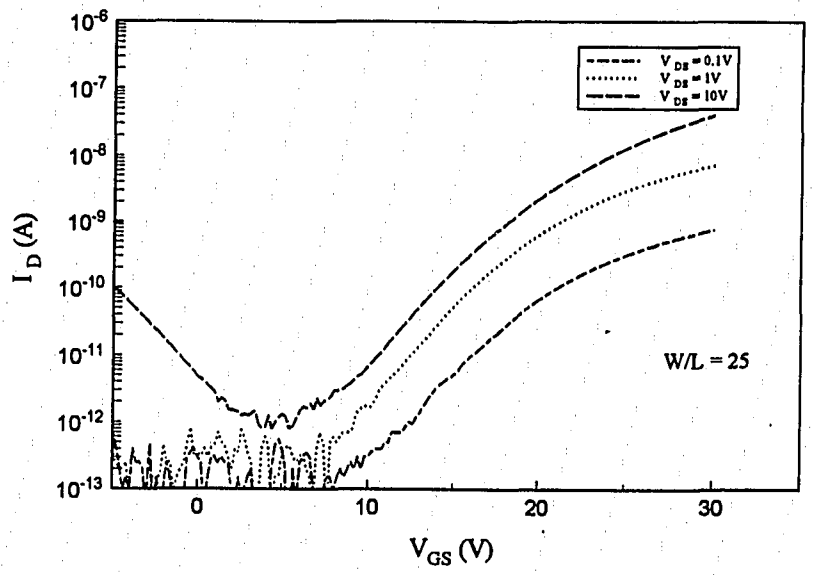


(a) On-Off Characteristic

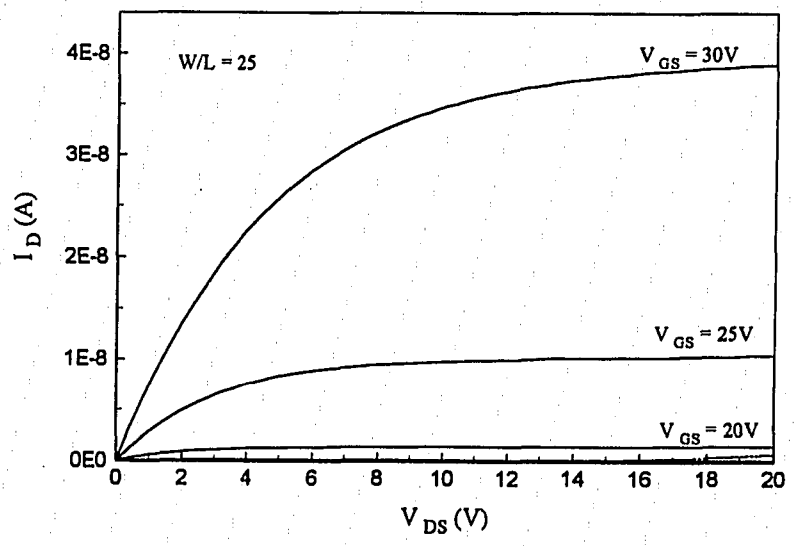


(b) Transfer Characteristic

Figure 4-6. Metallized a-Si:H (SD) TFT Characteristics

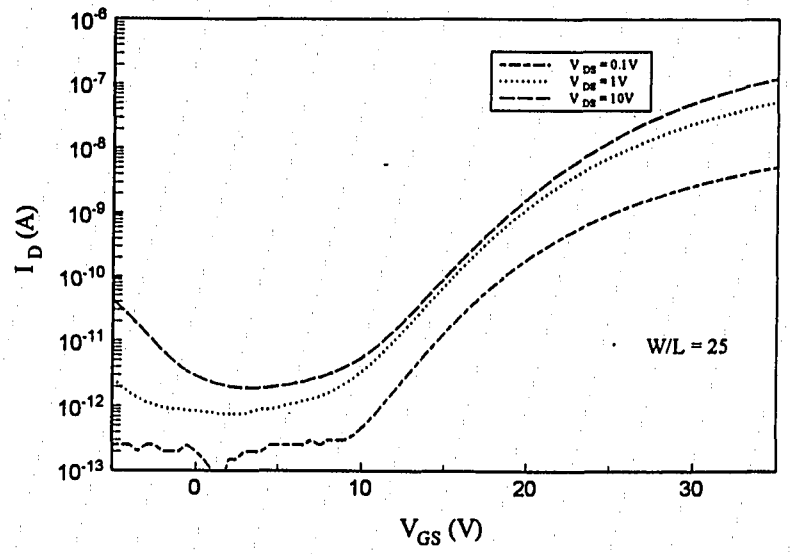


(a) On-Off Characteristic

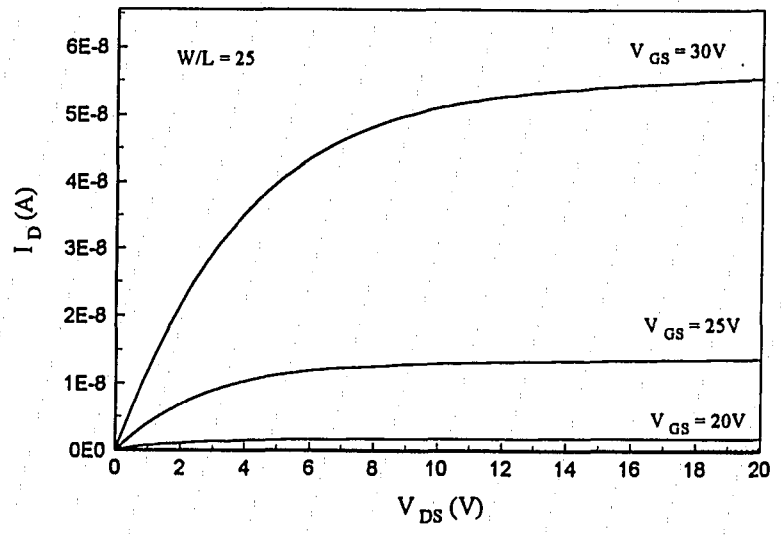


(b) Transfer Characteristic

Figure 4-7. Metallized a-$Si_{0.85}Ge_{0.15}$:H (SD) TFT Characteristics



(a) On-Off Characteristic



(b) Transfer Characteristic

Figure 4-8. Metallized a-$Si_{0.75}Ge_{0.25}$:H (SD) TFT Characteristics

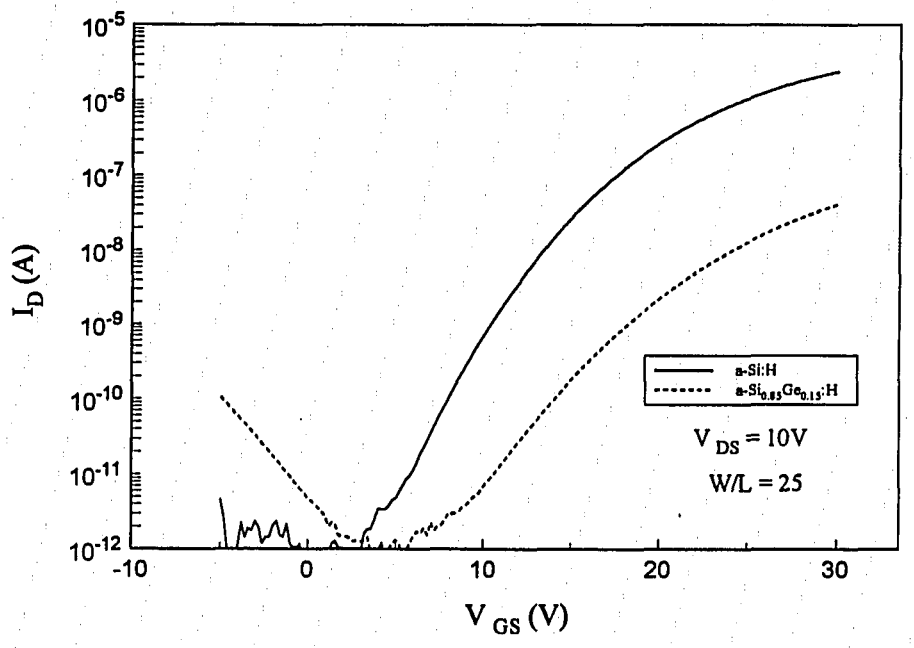


Figure 4-9. Comparison of Device Characteristics for (SD) TFTs with Varying Germanium Content.

4.4.2 Contact-Window Implant Structure

The silicon sample required annealing of 2h to achieve maximum mobility, and did not decline significantly upon further annealing. The peak value was 0.027 cm^2/V-sec, at 2h. The initial threshold voltage was 11 V, which slowly rose throughout the annealings. The subthreshold swing remained low, around 2 V/dec-A, until after 4h. The device parameters as a function of annealing time are shown in Table 4-7.

The 15 at%Ge sample quickly reached peak mobilities of $9x10^{-4}$ cm^2/V-sec in only 15 min., falling only after an hour of annealing. The threshold voltage remained high, around 19 - 20V throughout the anneals. The subthreshold swing remained nominally unchanged, around 4 V/dec-A. The results are shown in Table 4-8.

anneal time (min)	μ_{sat} (cm^2/V-sec)	V_T (V)	S (V/dec-A)
15	$8.3x10^{-5}$	11.6	2.0
30	$9.0x10^{-3}$	13.8	2.3
60	$1.3x10^{-2}$	15.3	2.0
120	$1.8x10^{-2}$	15.8	2.1
240	$2.7x10^{-2}$	17.0	1.9
360	$2.6x10^{-2}$	18.2	2.9

Table 4-7. Annealing Dependence of Mobility in a-Si:H TFT, CW Structure.

anneal time (min)	μ_{sat} (cm^2/V-sec)	V_T (V)	S (V/dec-A)
15	$9.2x10^{-4}$	19.0	4.5
30	$9.4x10^{-4}$	20.8	4.4
60	$9.7x10^{-4}$	19.6	4.0
120	$8.2x10^{-4}$	21.1	4.1

Table 4-8. Annealing Dependence of Mobility in a-$Si_{0.85}Ge_{0.15}$:H TFT, CW Structure.

anneal time (min)	μ_{sat} (cm^2/V-sec)	V_T (V)	S (V/dec-A)
15	$1.1x10^{-3}$	20.6	4.6
30	$1.1x10^{-3}$	20.1	4.1
60	$8.8x10^{-4}$	22.0	4.9
120	$7.2x10^{-4}$	23.3	3.8

Table 4-9. Annealing Dependence of Mobility in a-$Si_{0.75}Ge_{0.25}$:H TFT CW Structure.

The 25 at%Ge mobility peaked for anneals from 15 to 30 min., but the threshold voltage rose dramatically after 30 min. The threshold voltage remained constant, around 20V, and the subthreshold swing remained around 4 V/dec-A. The data are shown in Table 4-9. Since this trend of time-dependence was common to both SiGe samples, the optimal annealings for the alloy samples was thus determined to be 30 min.

The effect of the anneal can be seen from the ON-OFF device characteristics as a function of time. Figures 4-10 through 4-12 show the dependence on device performance as a function of annealing time and concentration of germanium.

Because the silicon sample showed optimal performance with 4 h of annealing, it was annealed 3h after implantation, then another hour after metallization. Since the silicon-germanium samples required 30 min to form an ohmic contact, and the device characteristics degrade upon further annealing, metallized silicon-germanium samples were prepared by annealing once, after the aluminum evaporation, for 30 minutes. These "optimized" metallized device characteristics are shown in Figures 4-13 through 4-15 for each of the concentrations of germanium. In Figure 4-16, the device performance is compared directly as a function of germanium content.

The mobility, threshold voltage, and subthreshold swing of optimized, metallized CW-structure devices for each of the germanium concentrations is given in Table 4-10. Note that the mobilities are much higher than those of the anneal-test devices, and of the SD-devices. The difference in mobility due to the SD *vs.* CW structure will be discussed in the following sections.

%Ge	μ_{sat} (cm^2/V-sec)	V_T (V)	S (V/dec-A)
0	0.828	20.0	2.1
15	8.08×10^{-3}	27.5	5.2
25	8.90×10^{-3}	23.3	4.1

Table 4-10. Optimized Metallized (CW) TFT Parameters.

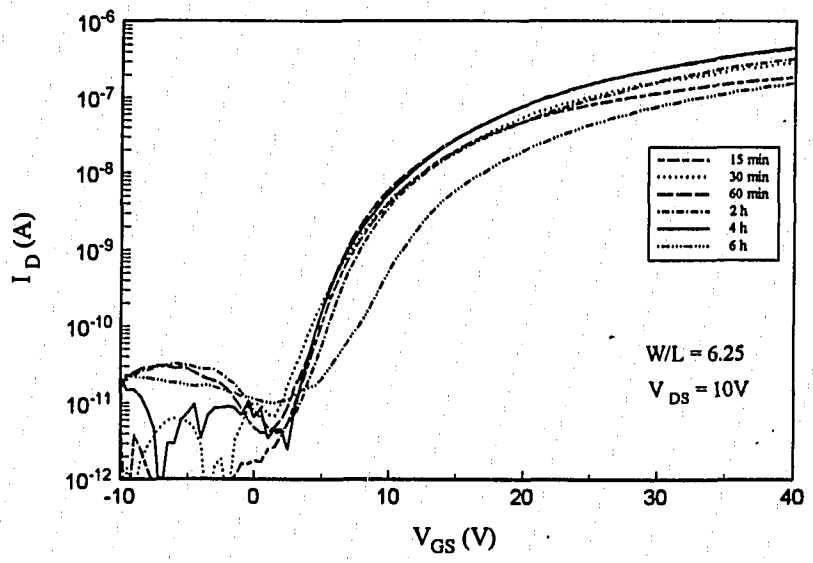


Figure 4-10. Effect of Annealing on a-Si:H (CW) TFT Performance.

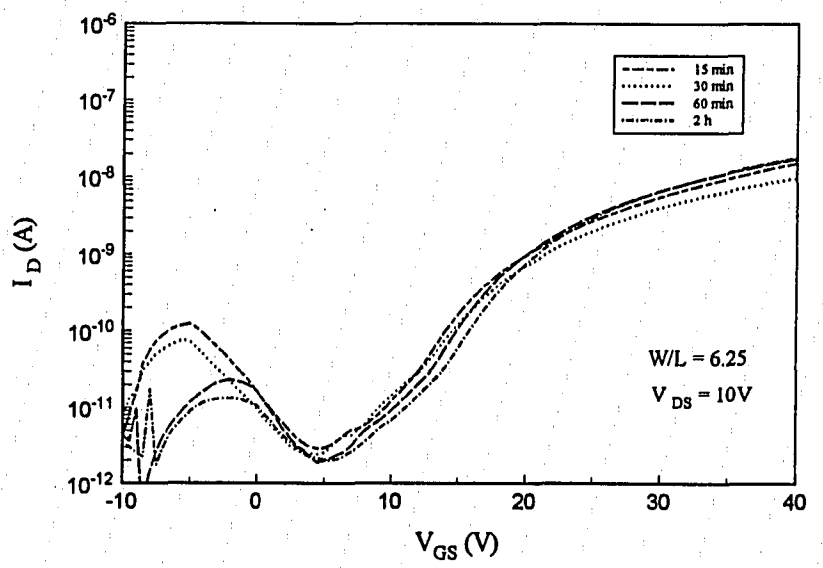


Figure 4-11. Effect of Annealing on a-$Si_{0.85}Ge_{0.15}$:H (CW) TFT Performance.

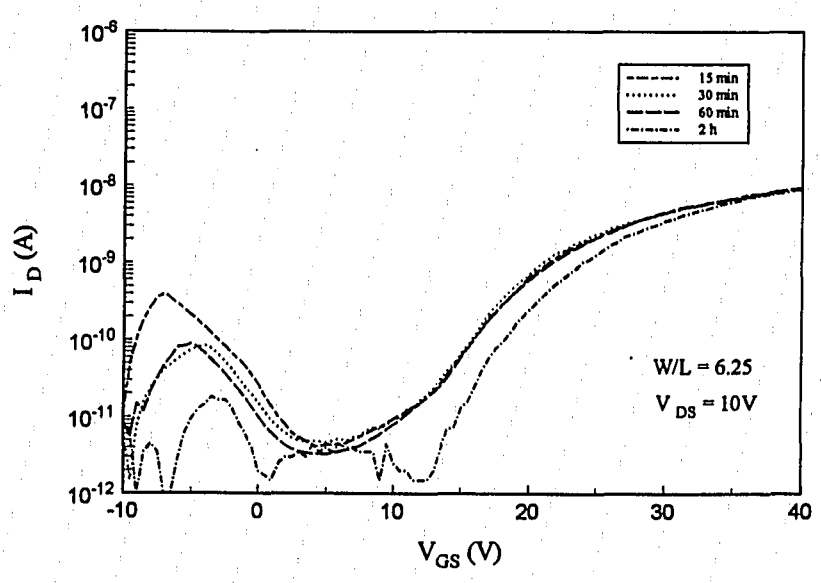
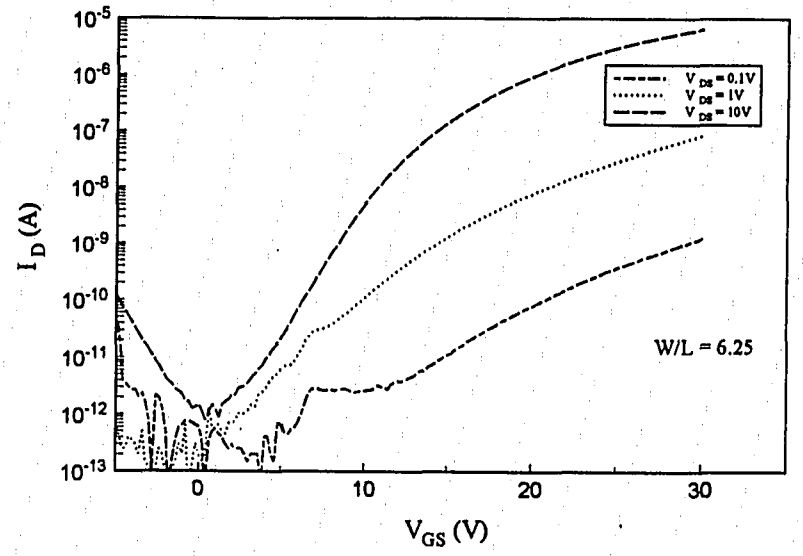
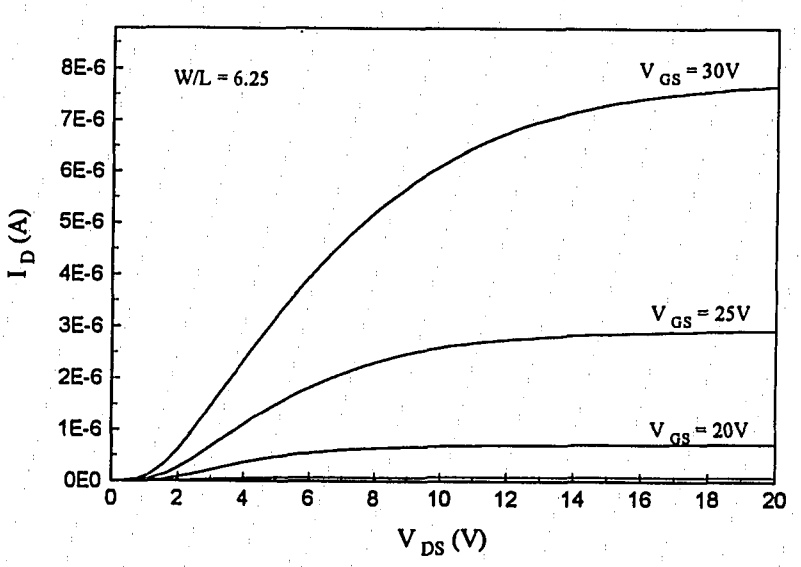


Figure 4-12. Effect of Annealing on a-$Si_{0.75}Ge_{0.25}$:H (CW) TFT Performance.

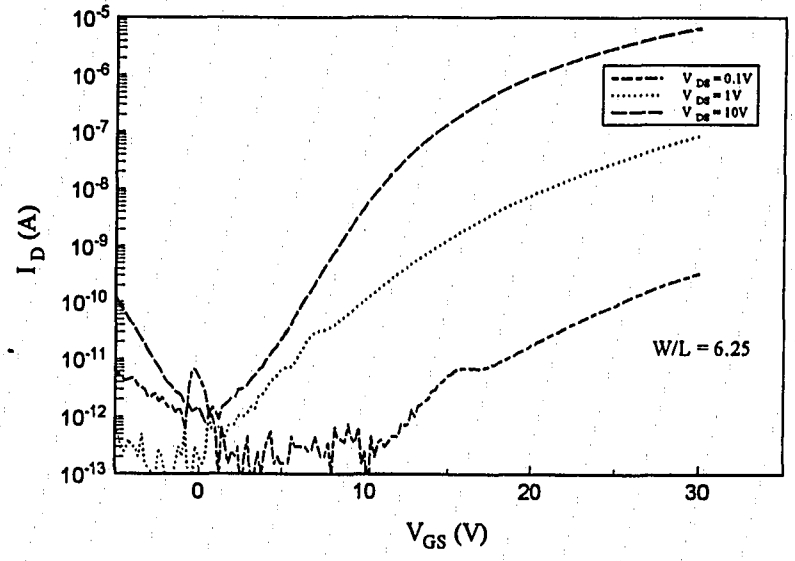


(a) On-Off Characteristic

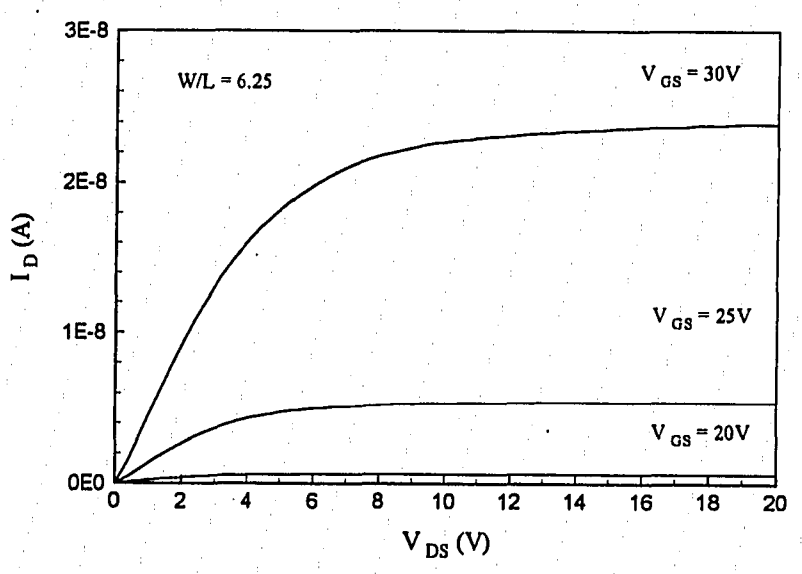


(b) Transfer Characteristic

Figure 4-13. Metallized a-Si:H (CW) TFT Characteristics

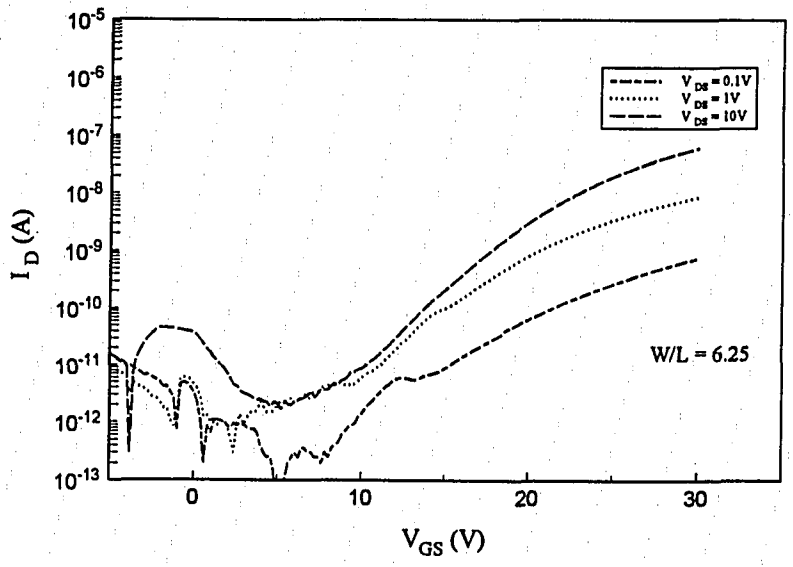


(a) On-Off Characteristic

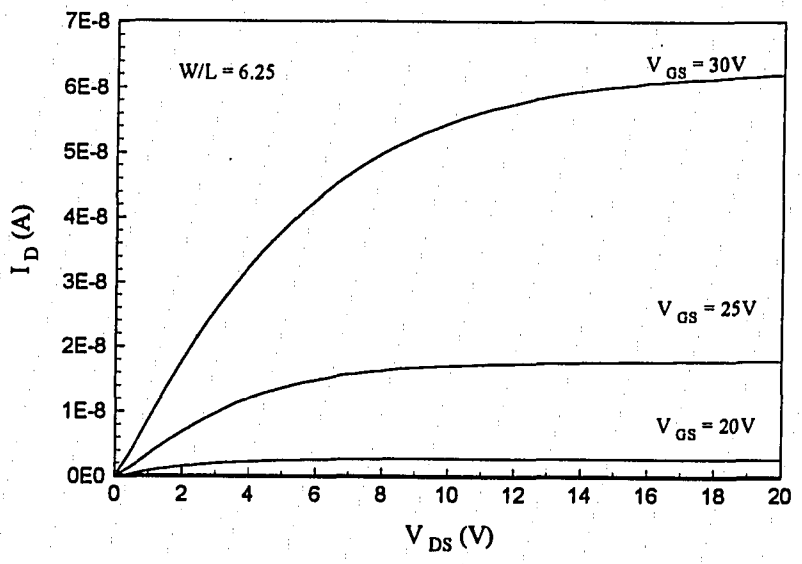


(b) Transfer Characteristic

Figure 4-14. Metallized a-$Si_{0.85}Ge_{0.15}$:H (CW) TFT Characteristics



(a) On-Off Characteristic



(b) Transfer Characteristic

Figure 4-15. Metallized a-$Si_{0.75}Ge_{0.25}$:H (CW) TFT Characteristics

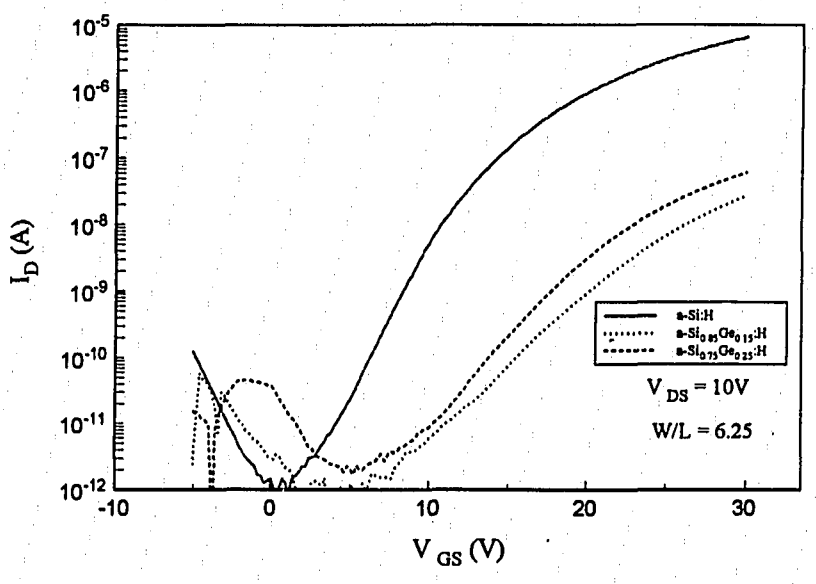


Figure 4-16. Comparison of Device Characteristics for (CW) TFTs with Varying Germanium Content.

4.5 Mobility Correction

The mobilities calculated above were dependent on the device length. In Table 4-11, the mobilities as a function of length, device structure, and concentration of germanium are listed. Note that the values are about a factor of ten higher in the CW structures than in the SD structures, indicating a strong dependence of device characteristics on the structure. Also, the germanium samples show inferior mobilities.

The length dependence of mobility is common in amorphous TFTs. The high external resistance is one reason; it may be comparable to the channel resistance. The effective channel length is also affected by the structure of the device. Three methods were used to correct the mobilities for their length dependence [67-69].

%Ge	L (μm)	structure	μ_{sat} (cm^2/V-sec)
0	5	SD	0.0307
	10	SD	0.0457
	40	CW	0.828
	56	CW	0.723
15	5	SD	7.23×10^{-4}
	10	SD	1.86×10^{-3}
	40	CW	8.46×10^{-3}
	56	CW	1.08×10^{-2}
25	5	SD	6.00×10^{-4}
	10	SD	8.34×10^{-4}
	40	CW	7.21×10^{-3}
	56	CW	8.48×10^{-3}

Table 4-11. Length and Structural Dependence of Mobility

4.5.1 Chern Method

In the Chern analysis, illustrated in Figure 4-17, the resistance of the device in linear mode is plotted against the mask-length for a series of gate voltages [67]. The resistance is given by:

$$R_{meas} = \frac{V_{DS}}{I_D} \tag{4.2}$$

The intersection point of the lines gives the coordinate for the external resistance and the parasitic channel effect 2ΔL. This value indicates structural effects and processing effects. Often, the effective channel length of an amorphous TFT is longer than the mask length, as is opposite the case in single-crystal MOSFETs. The effective channel length L_{eff} is related to the mask length (L) by:

$$L_{eff} = L - \Delta L \tag{4.3}$$

The mobility is corrected by the expression:

$$\mu_{corrected} = \mu_{measured}\left(\frac{L - \Delta L}{L}\right) \tag{4.4}$$

The resulting factors ΔL and R_{ext}, and their corrections to the mobility, are shown in Tables 4-12 and 4-13. Note how the mobility converges within device structures, and that the relative magnitude of the mobilities is still about 10.

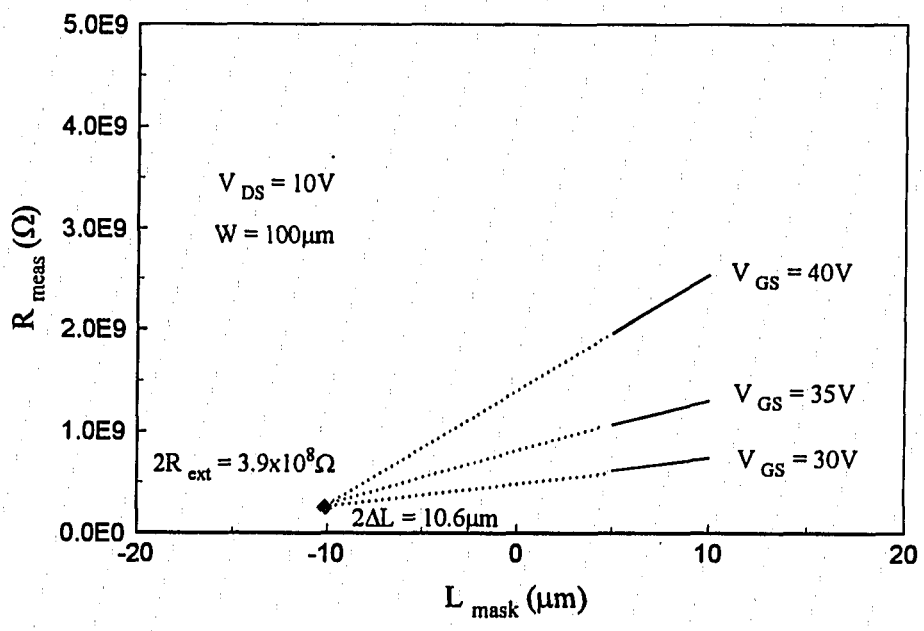


Figure 4-17. Chern Method for Mobility Correction

4.5.2 Whitfield Method

The Whitfield method [68], is used for devices with high external resistance. Devices are compared on their relative resistance. Devices of two lengths are measured, and their resistances, R_1 and R_2, are computed as per equation 4.2. The difference in their resistances (δR) is plotted against the resistance of the shorter-length device (R_1). The resistance intercept of the fitted line, as shown in Figure 4-18, gives the external resistance, R_{ext}. The slope of the line, M, is used to determine the parasitic channel length factor ΔL, according to:

$$\Delta L = L_1 - \frac{L_2 - L_1}{M} \tag{4.5}$$

The parameters for external resistance and channel length correction are listed in Table 4-12, and their corrections to the device mobilities are shown in Table 4-13.

4.5.3 Kaneko Method

The Kaneko method [69] is used to determine the structural effect of the device on the extracted mobility, concentrating on the contact resistance and electron path. These effects are incorporated into an effective length. In this method, the gain of the device, β, is determined and its inverse is plotted against the mask length.

$$\beta = \frac{\mu C_{ox} W}{L} \tag{4.6}$$

The length intercept of the fitted line gives the parasitic channel length correction factor, ΔL, as illustrated in Figure 4-19.

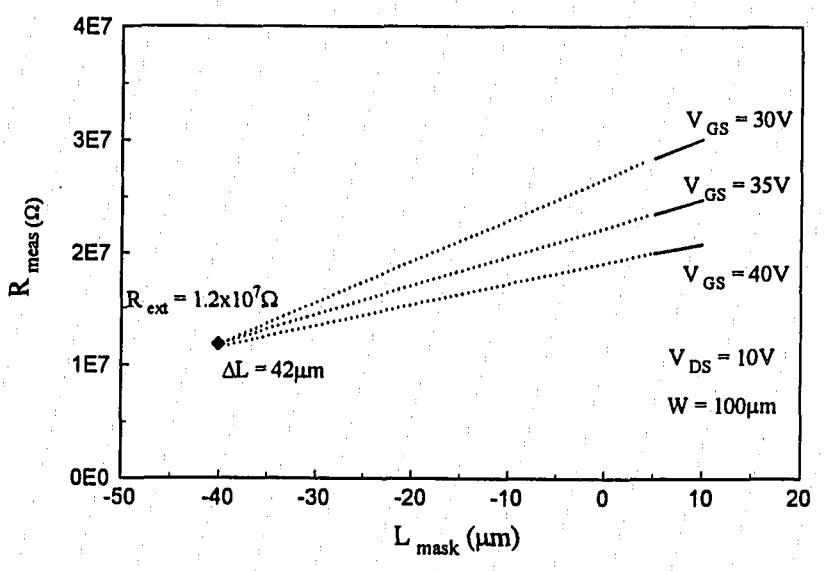


Figure 4-18. Whitfield Method for Mobility Correction

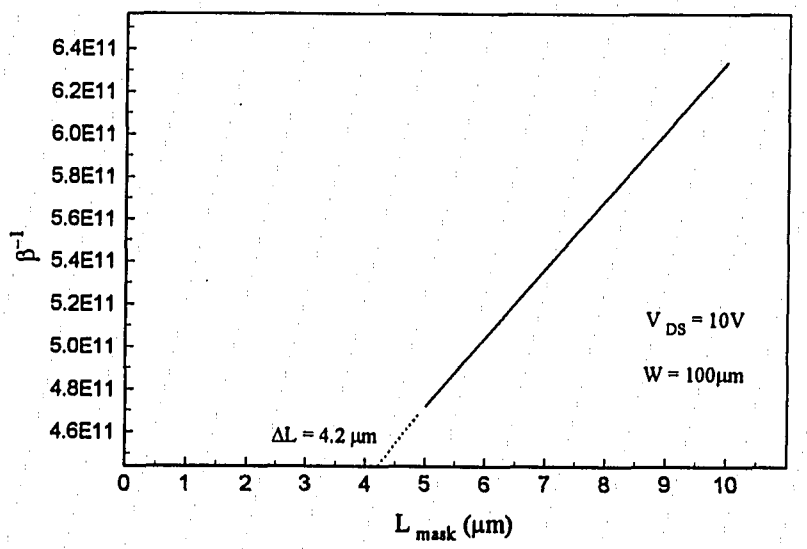


Figure 4-19. Kaneko Method for Mobility Correction

4.5.3 Discussion of Correction Methods

The parasitic channel lengths and the external resistances (Table 4-12) do not agree well because they incorporate different factors. The Chern method considers processing effects. The Whitfield method considers source and drain sheet and contact resistance. The Kaneko method considers conduction path and contact resistance. The methods do, however, converge the mobilities within device structures and germanium content (Table 4-13). The correction factors may give unrealistic values, but that is due to the method of accommodation for parasitics; *e.g.*, for a method which determines only an effective channel length, there may need to be a large correction to compensate for a large contact or series resistance.

The trend of values shows a longer parasitic length in the CW devices than in the SD devices. This may be due to the three-dimensional nature of the electron flow through these devices [69]. The other noticeable trend is a larger resistance in the SD devices than in the CW devices, suggesting increased disorder in the SD devices. The factor of ten difference of the external resistance describes well the difference in the measured mobilities between the two device structures. However, for the germanium devices, the extracted parasitic resistance difference decreases, suggesting a common resistive mechanism: alloy scattering.

		Chern		Whitfield		Kaneko
%Ge	structure	ΔL (μm)	R_{ext} (Ω)	ΔL (μm)	R_{ext} (Ω)	ΔL (μm)
0	SD	10	5.8×10^6	42	1.2×10^7	4.8
	CW	12	3.9×10^5	23	7.7×10^5	13
15	SD	5.3	2.0×10^8	8.6	4.9×10^8	14
	CW	9.2	1.5×10^7	25	3.3×10^8	58
25	SD	1.5	1.0×10^8	2.1	1.1×10^8	3.2
	CW	5.2	5.0×10^7	9.4	1.2×10^8	22

Table 4-12. Mobility Correction Factors

%Ge	L (μm)	structure	μmeasured	μChern	μWhitfield	μKaneko
0	5	SD	0.0307	0.154	0.291	0.089
	10	SD	0.0457	0.137	0.239	0.089
	40	CW	0.828	1.08	1.02	1.05
	56	CW	0.723	1.02	1.02	1.05
15	5	SD	7.2×10^{-4}	2.2×10^{-3}	2.0×10^{-3}	5.0×10^{-3}
	10	SD	1.9×10^{-3}	3.8×10^{-3}	3.4×10^{-3}	7.0×10^{-3}
	40	CW	8.5×10^{-3}	1.2×10^{-2}	1.4×10^{-2}	3.3×10^{-2}
	56	CW	1.1×10^{-2}	1.2×10^{-2}	1.5×10^{-2}	3.3×10^{-2}
25	5	SD	6.0×10^{-4}	9.7×10^{-4}	8.6×10^{-4}	1.4×10^{-3}
	10	SD	8.3×10^{-4}	1.1×10^{-3}	1.0×10^{-3}	1.4×10^{-3}
	40	CW	7.2×10^{-3}	9.1×10^{-3}	8.9×10^{-3}	1.5×10^{-2}
	56	CW	8.5×10^{-3}	1.0×10^{-2}	8.9×10^{-3}	1.5×10^{-2}

Table 4-13. Corrected Mobilities

4.6 Plasma Hydrogenation

Devices were subjected to plasma hydrogenation, which has been observed to increase the mobility of amorphous TFTs [54,70]. Plasma hydrogenation was performed for 90 min at 260°C, at 6 mtorr in hydrogen and nitrogen (2 mtorr H_2, 4 mtorr N_2 partial pressures) at a power intensity of 1 W/cm^2. The pre-and post- hydrogenation non-corrected mobilities for the amorphous silicon devices are 0.828 and 0.420 cm^2/V-sec, *resp.* The silicon-germanium devices did not function after hydrogenation. This suggests that the plasma exposure was damaging to the devices.

4.7 Conclusions

Amorphous silicon TFTs with a mobility above 1 cm^2/V-sec were fabricated using ion-implantation for forming the source and drain regions. After annealing at 260°C, the the implant provided blocking junctions.

The mobility values, even after correction, for the silicon-germanium devices suggest that these devices are inferior to the silicon devices. This may be due to the increased disorder due to the alloy nature of the silicon-germanium, providing additional scattering hence lower mobility. Or, the silicon-germanium may effuse the passivating hydrogen too rapidly, thus preventing anneals long enough to increase the activation of implanted dopants. Judging from these results, silicon-germanium may not be suitable for integrated amorphous TFT driver technology.

The significantly high measured sheet resistances and extracted external resistances of the silicon and silicon-germanium devices supports that conduction through the device may be limited by the parasitic resistance. Low temperature nickel silicidation after the implant may be employed to reduce this resistance. As will be shown in the next chapter, removal of series resistance can greatly improve device performance.

The device structure impacted profoundly the device parameters. This is due to the different conduction nature between the SD and the CW devices. In the SD devices, the electrons must travel laterally, hence longer, through an implanted region. The lower mobility found in the SD devices may be ascribed to their higher external resistance. In the CW devices, the electrons must spread from the bottom of the contact window to the channel edge. This is described by typically longer effective channel length factor than found in the SD devices.

Chapter 5
Polysilicon Thin Film Transistors with Cobalt and Nickel Self-Aligned Silicides

5.1 Introduction

The top-gate structure of polysilicon TFTs, and their superior mobilities in comparison to amorphous silicon and silicon-germanium TFTs, suit them well for active-matrix displays with integrated drivers. Driver circuitry can be designed with CMOS process and circuit architecture. Because low-cost glass cannot withstand the temperatures associated with the crystallization step, the polysilicon process is expensive. Either refractory glasses or quartz must be used as the active plate in a polysilicon TFT display process. However, the better performance of polysilicon TFTs and the savings by the integration of the driver circuitry turn the direction of TFT-LCDs towards polysilicon.

5.2 Motivation for Ultra-Thin Film Transistors

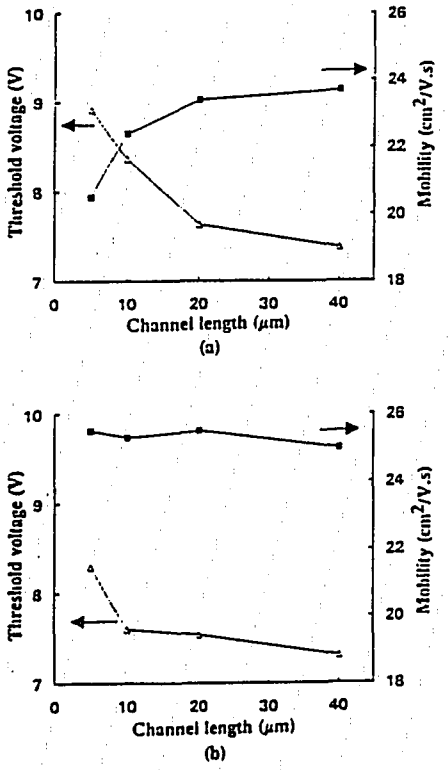
The largest motivation for, and application of LCDs is their portability. For a portable display, one of the primary issues is the power required to operate it. High threshold voltage devices and high-voltage power-supply circuits decrease battery life.

Polysilicon TFTs have been made on films where the polysilicon thickness of or above 1000Å for some time. It has been observed that the threshold voltage, subthreshold swing, leakage current and mobility are related to the grain-boundary defects in the channel [71-74]. The defect states: increase the threshold voltage, increase the subthreshold swing, generate leakage current, and decrease the electron effective mobility. All of these factors increase the power required to drive the device.

The threshold voltage is increased by the defect states because they pin the Fermi level under the gate, preventing the creation of an "inversion" layer for the on state

[72,73]. An increased threshold voltage causes the power supply levels for logic circuits to be higher.

The subthreshold swing, in V/dec-A, indicates how quickly (in terms of the input gate voltage) the TFT switches between the off and on states. A large swing means that the gate voltage must rise more in order to turn the device fully on. For a given input signal, a device with a low swing will turn on and charge up its output load faster than a device with a large swing. In Figure 5-1, the threshold voltage for devices fabricated on 1050Å and 540Å thick islands is compared [72]. The threshold voltage for devices on thin islands is lower.



The variation of measured threshold voltage and measured mobility as a function of the channel length for: 105 nm thick channel layer (a); 54 nm thick channel layer (b).

Figure 5-1. Dependence of Threshold Voltage on Polysilicon Island Thickness [Bonnel, 72]

The leakage current is a field-enhanced generation current generated from defect states [72,74]. Reduction of the number of states decreases the leakage current. The number of states can be decreased by fabricating the device on a thinner island. A comparison of leakage current as a function of island thickness is shown in Figure 5-2 [72]. In that study, films of different thicknesses were crystallized by two methods, furnace and rapid-thermal annealing. Using either method, the leakage current was a function of film thickness.

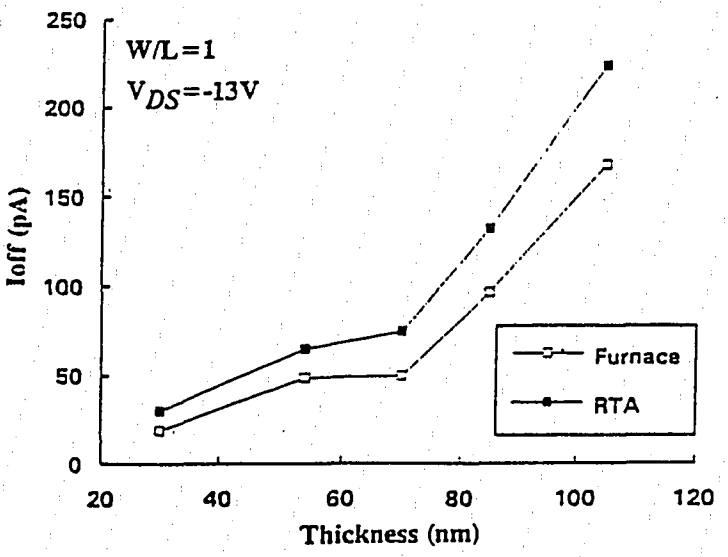


Figure 5-2. Dependence of Leakage Current on Polysilicon Island Thickness [Bonnel, 72]

Reduction in the effect of defect states by forming gas annealing and plasma hydrogen treatments is common [73,75]. Since device characteristics are dependent on the defect state activity, and the number of states in general [71], it seems reasonable that device performance can be improved by reducing the number of states by fabricating the devices on thinner islands. A thinner island offers a lesser volume under the gate for defects. However, thinning the island increases the series resistance of the source and drain. This series resistance limits the current, as shown in Figure 5-4. The drain voltage is 1V, and the source and drain sheet resistance is 100 kΩ/□. The drain current is limited to 1.35μA. The island thickness about 300Å.

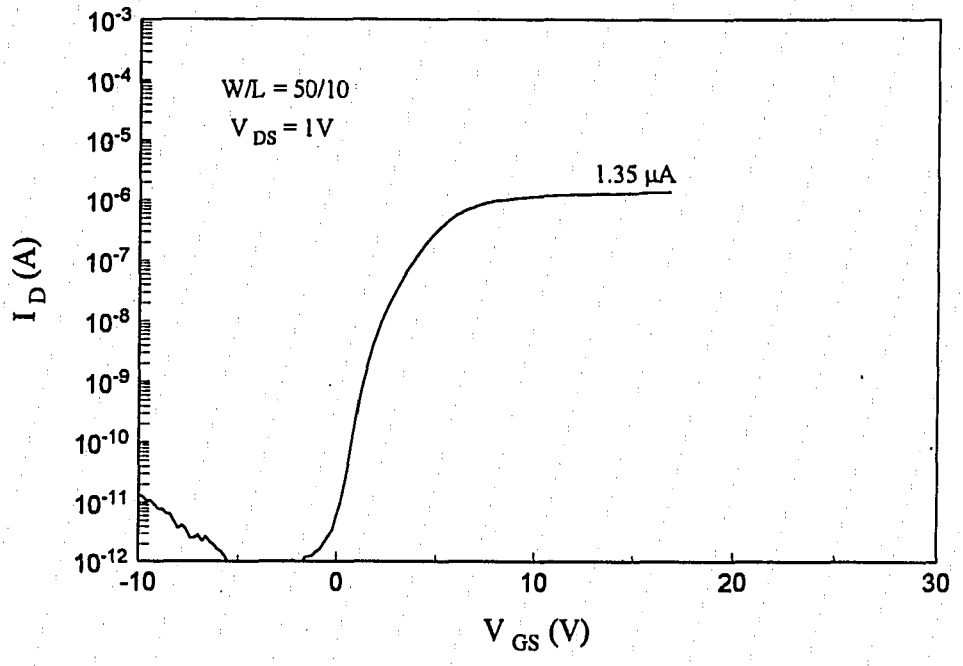


Figure 5-3. Limitation of Ultra-Thin Film Transistor Current Due to Source and Drain Series Resistance.

The self-aligned silicide is expected to remove the limitations imposed by the thin islands. The silicide processes described in Chapter 3 was used on TFTs with island thicknesses of 600Å and less. In this Chapter, device characteristics and parameters on thick and thin islands, with and without silicided sources and drains, are compared.

5.3 Fabrication Process for Self-Aligned Silicided Polysilicon TFTs

Polysilicon thin film transistors were fabricated using the process sequence described in detail in the Appendix. In summary, 1 μm SiO_2 was grown on 3" Si wafers. Silicon was deposited to a thickness of 600Å and 1100Å by LPCVD in 200 mtorr SiH_4, at 580°C. The films were crystallized in N_2 at 600°C for 3h. After island patterning in 1:50:20 $HF:HNO_3:H_2O$, the gate oxide was grown in dry oxygen at 1000°C. The 1100Å islands were oxidized 90 min, to a gate oxide thickness of 900Å. The 600Å islands were oxidized 90 min, to a gate oxide thickness of 720Å. Assuming 45% of the gate oxide is silicon consumptive, the island thicknesses after oxidation were about 695Å and 283Å for "thick" and "thin" TFTs.

Gate silicon was deposited by LPCVD in 200 mtorr SiH_4, at 580°C, to a thickness of 1200Å. After patterning the silicon gate stripes, and source/drain oxide etch, the gate silicon was crystallized and doped, and the source and drain regions formed, by $POCl_3$ diffusion at 900°C. The sheet resistance of the as-diffused gate stripes was 30 - 40 Ω/□. The source and drain region sheet resistance for the thick polysilicon islands, and gate stripes on all devices, was 40 - 90 Ω/□. The source and drain sheet resistance of thin polysilicon devices was greater than 30 kΩ/□. During the $POCl_3$ diffusion, about 200 - 250Å oxide was grown on the doped regions, thinning the source and drain regions by an additional 100Å.

Self-aligned silicides were grown on the gate, source, and drain using the silicidation method described in Chapter 3. Wafers were RCA cleaned, then prior to loading were HF-dipped, DI water rinsed, IPA immersed, and nitrogen blow-dried. Cobalt and nickel were RF-sputtered in Ar at 9 mtorr, followed by in-situ lamp anneal for 10 min. The silicidation anneal temperatures for cobalt wafers was 700°C; for nickel, the anneal temperature was 400°C. The wafers were half-covered by a silicon wafer similarly cleaned and prepared; this permitted the fabrication of "with silicide" and "without silicide" devices on the same substrate for direct comparison. After cooling and removal, wafers were metal-etched for 30 sec. The cobalt samples were etched in 3:1 H_2O_2:HCl. Nickel samples were etched in 3:1 H_2O_2:H_2SO_4. A summary of wafer processing, including island thickness, silicidation, and sheet resistances, is shown in Table 5-1. The device structure is shown in Figure 5-4.

wafer	island thickness (Å)	metal type (Å)	$R_{S,SD}$ (Ω/□) silicided	$R_{S,SD}$ (Ω/□) non-silicided
M3	595	Co (60)	40	> 30k
M11	183	Co (60)	1k	> 100k
M5	595	Ni (86)	10	> 30k
M4	595	Ni (43)	20	> 100k
M10	183	Ni (43)	2k	> 100k

Table 5-1. Summary of Device Parameters with and without Silicidation

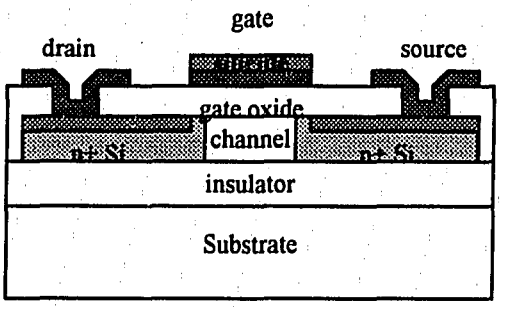


Figure 5-4. Salicide TFT Device Structure

5.4 Electrical Measurement Techniques

Devices were measured using a HP-4145 Semiconductor Parameter Analyzer. From $I_D(V_{GS})$ characteristics, the threshold voltage and effective effective mobility were measured, as shown in Figure 5-5. The mobility was calculated from the transconductance in the linear mode ($V_{DS} < V_{GS} - V_T$):

$$I_D = \mu_{eff} \frac{W}{L} C_{ox} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \tag{5.1}$$

$$\mu_{eff} = \frac{\frac{\partial I_D}{\partial V_{GS}}}{\frac{W}{L} C_{ox} V_{DS}} \tag{5.2}$$

The effective mobility incorporates the extrinsic device resistance. Decreases in the extrinsic resistance by incorporating a silicide to the source and drain would increase the effective mobility. The increase in current due to the silicide can be related to the decrease in the series resistance, R, from the non-silicided device, by equation 2.14.

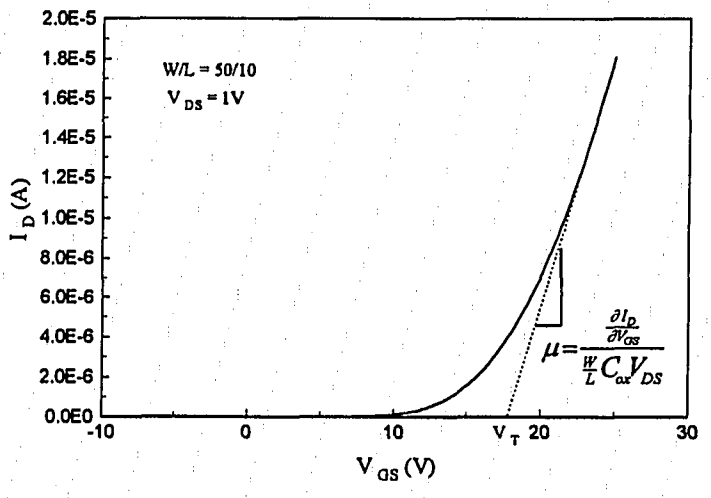


Figure 5-5. Extraction of Threshold Voltage and Effective Mobility

The subthreshold swing, S (V/dec-A) is measured from the inverse of the maximum slope of the $\log I_D(V_{GS})$ characteristic, as shown in Figure 5-6. The FET transfer characteristics of the TFT are shown in Figure 5-7.

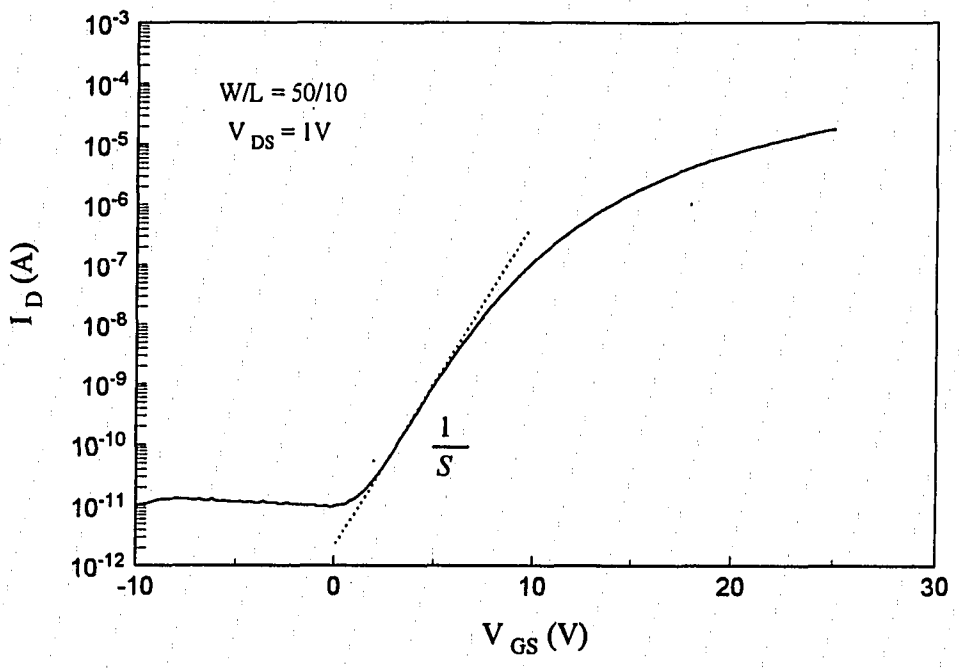


Figure 5-6. Extraction of Subthreshold Swing

These measurements were taken on devices with and without silicide, on the same wafer. The device characteristics of non-silicided, nickel- and cobalt silicided devices, on thin and thick polysilicon, are discussed in the following section.

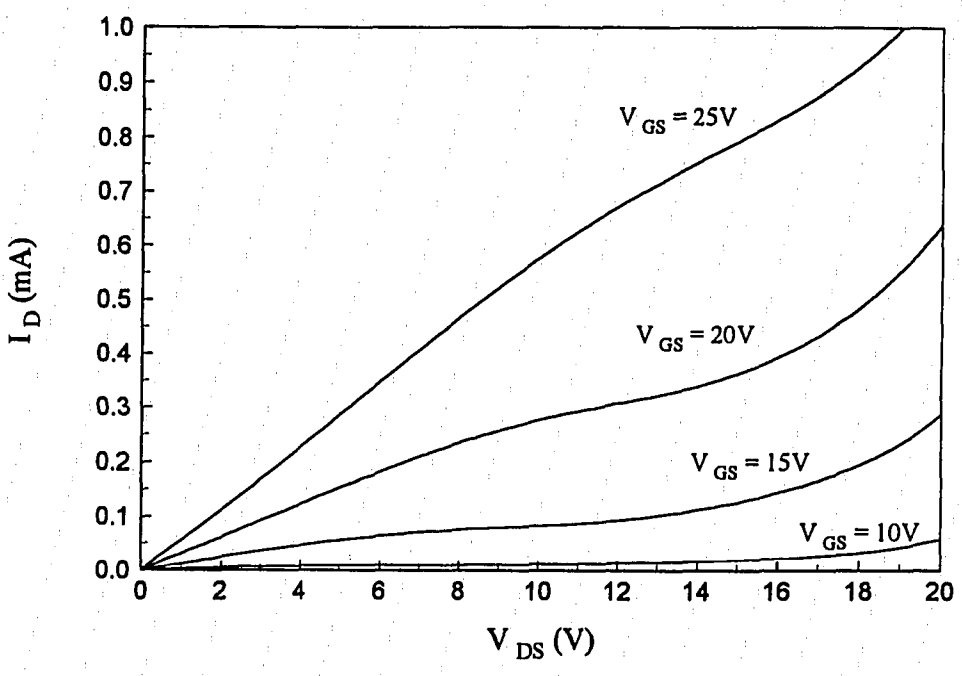


Figure 5-7. FET Transfer Characteristics of TFT

5.5 Results and Discussion

The device results will be discussed by comparing device characteristics for each of the effects of polysilicon island thickness, silicidation, hydrogen anneal (if applicable), and silicide type (nickel or cobalt). A comparative log $I_D(V_{GS})$ plot will typically be used in order to show the difference in the subthreshold swing and saturation current, and because the difference between the silicided devices and non-silicided devices was often too great to be clearly shown with a transfer plot. Tables will summarize device parameters. Device measurement and parameter extraction were taken on devices with geometry 50/10, with V_{DS} = 1V for standardization.

5.5.1 Cobalt Silicided Devices

The parameters for cobalt silicided devices are listed in Table 5-2. Listed are: thick polysilicon devices before silicidation; thick polysilicon devices immediately after silicidation; and thick and thin polysilicon devices after 2h PMA in forming gas.

island thickness (Å)	μ (cm^2/V-sec)	V_T (V)	S (V/dec-A)
		before silicidation	
600	13	18	1.9
		silicided, after silicidation (no PMA)	
600	1.1	21	4.5
295	1.3	22	4.1
		non-silicided, after PMA	
600	22	15	1.3
295	(1)	(3.79)	0.614
		silicided, after PMA	
600	22	16	1.3
295	27	9	0.53

Table 5-2. Device Parameters from Cobalt -Silicided TFT Study

The cobalt silicided devices required the PMA treatment due to the increase of the threshold voltage, subthreshold swing, and high gate current. The parameters for the thin island after silicidation before PMA were severely limited by series resistance; the parameter extraction methods gave accordingly misleading results, particularly for the threshold voltage.

The characteristics in Figure 5-8 show thick polysilicon devices without silicide as a function of annealing treatments. Shown are the initial device, the device after the silicidation treatment (though the devices were masked to prevent cobalt exposure), and the same devices after the post-silicidation forming gas anneal.

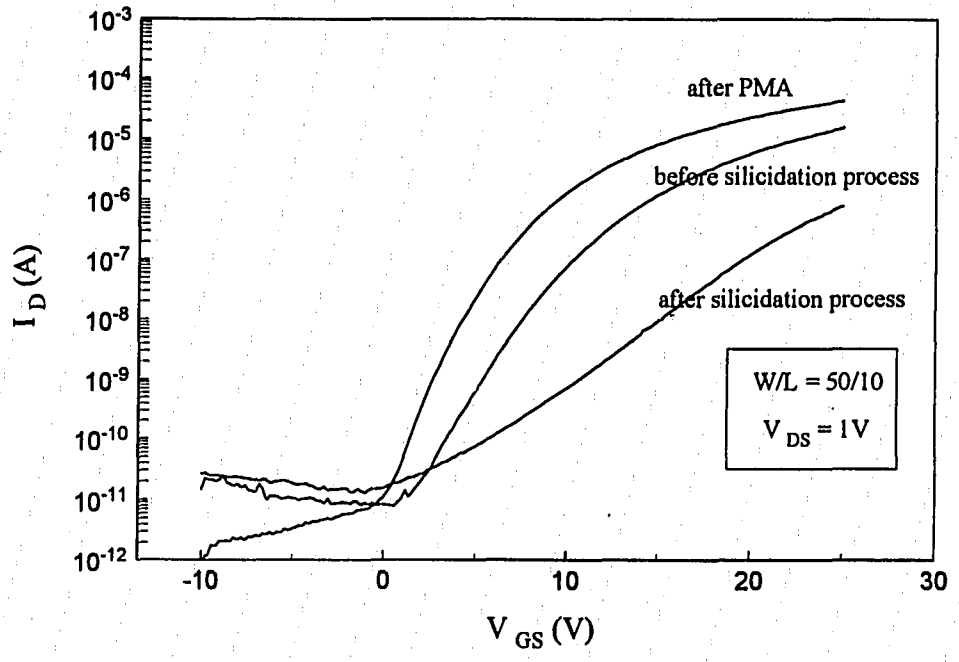


Figure 5-8. Effect of Annealing on Thick Polysilicon Devices without Cobalt Silicide

Note that the devices after silicidation were in need of hydrogen passivation anneal. The hydrogen annealed devices are similar to, or better than the initial devices. The hydrogen anneal improved the swing dramatically, indicating removal of damage which also increased the mobility and decreased the threshold voltage. Because the hydrogen annealed device performed better than the initial device, the initial device must have had defects in the polysilicon film and gate dielectric interface, both of which had negative effects on the mobility, threshold voltage, and swing.

Figure 5-9 shows the same comparison, for thin polysilicon TFTs. Again, the silicidation process was damaging to the devices. What is different here is the performance of the "before silicidation" device in comparison to the hydrogen annealed

device after the silicidation process. The initial device has a much lower threshold voltage, and higher subthreshold swing than the hydrogen annealed device. This indicates that the hydrogen anneal does not remove all of the damage. Also note that the initial device has a lower swing than the initial, thick poly device (0.614 *vs.* 1.9 V/dec-A). This suggests that the reduction of island thickness may improve device performance by reduction of the number of defects. However, due to the series resistance limitation of the initial device, the threshold voltage could not be accurately extracted.

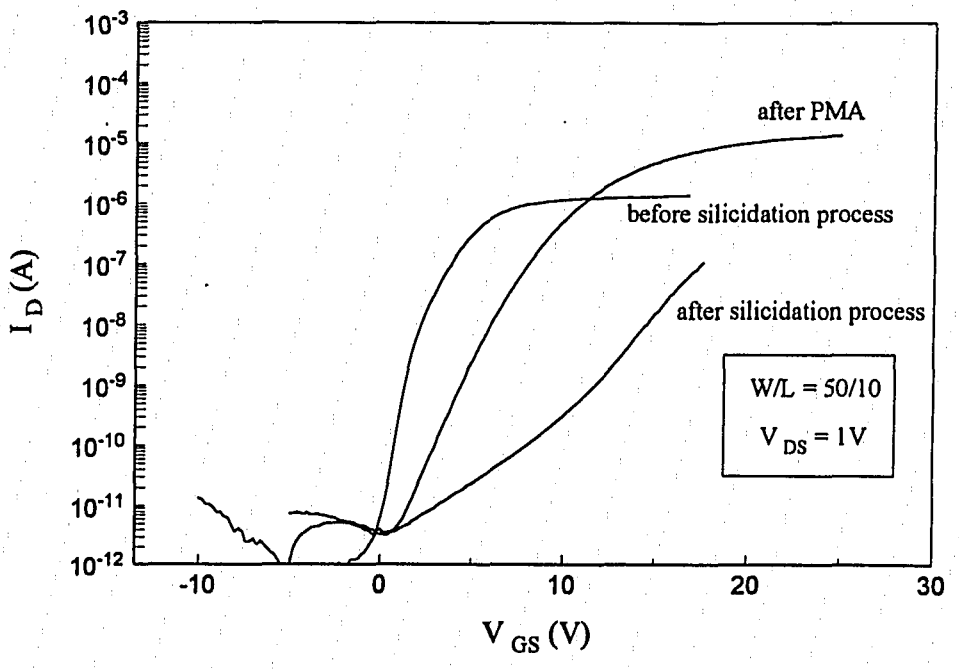


Figure 5-9. Effect of Annealing on Thin Polysilicon Devices without Cobalt Silicide

In Figure 5-10, the effect of the annealings on thick devices with silicide are compared to the initial device. Note the necessity of hydrogen annealing for the silicided device.

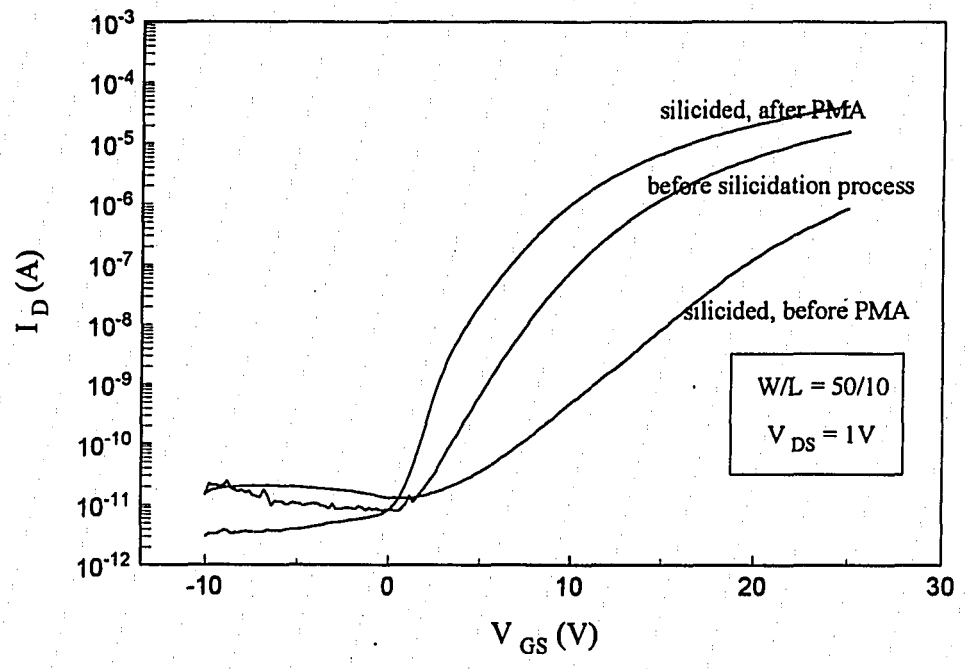


Figure 5-10. Effect of Annealing on Thick Polysilicon Devices with Cobalt Silicide

The subthreshold swing and threshold voltage have decreased, and the mobility increased due to the silicide and/ or the hydrogen anneal. Figure 5-12 will re-address this issue.

The corresponding comparison on thin devices with silicide is shown in Figure 5-11. Again, the device is improved greatly by silicidation. The initial device here performed better than in Figure 5-9 because the island was slightly thicker, thus imposing less series resistance limitations. The mobility for the thin, silicided device, 27 cm^2/V-sec, was the highest of all of the cobalt devices.

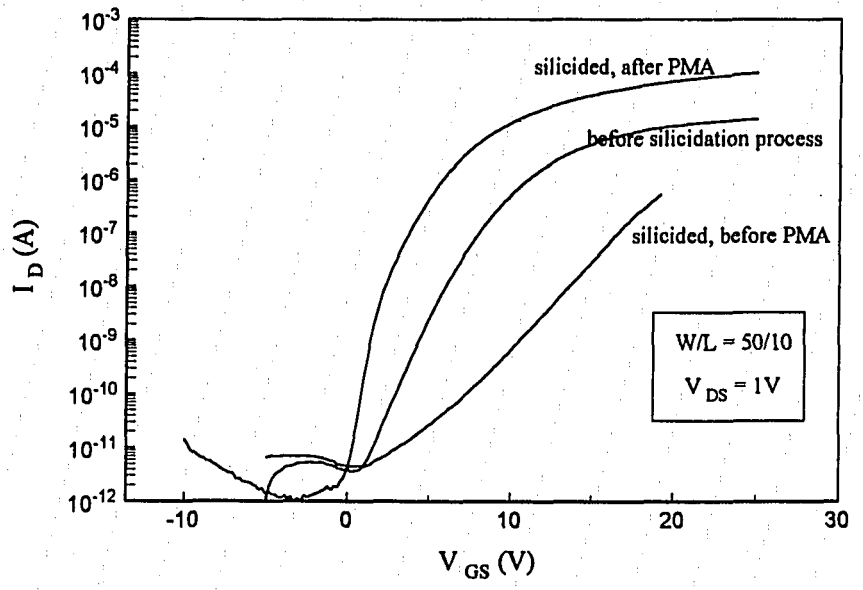


Figure 5-11. Effect of Annealing on Thin Polysilicon Devices with Cobalt Silicide

The characteristics shown are for hydrogen-annealed devices. For the thick poly TFTs shown in Figure 5-12, there appears to be little improvement in the device characteristics. Since both are so similar, improvement from the initial device is not due to the silicide. The sheet resistance of the source and drain of the non-silicided devices may be low enough, such that the device conductance is channel-limited. In some instances, the silicided devices appear to be worse than the non-silicided devices! This implies that there may be some residual radiation damage to the silicided devices. The damage is evinced as a slight increase in the threshold voltage. This is supported by the data in Table 5-2, and the appearance of the curves of Figure 5-12 to be a "shift", instead of a distinct difference in magnitude. However, the difference is minor compared to those shown in Figures 5-8 and 5-10, where the anneal damage is quite severe. Thus thermal

exposure may be more damaging than the short radiation exposure. It should also be noted that the leakage current is not increased by the silicide.

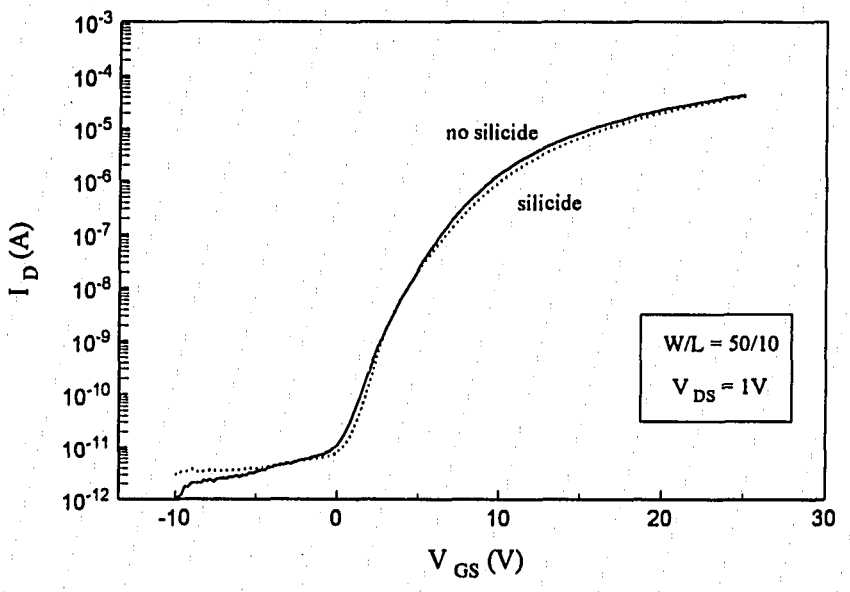
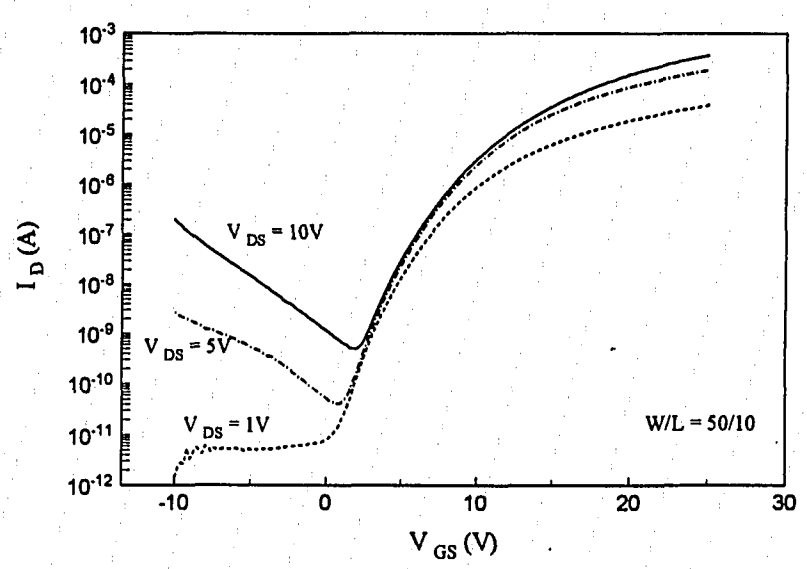
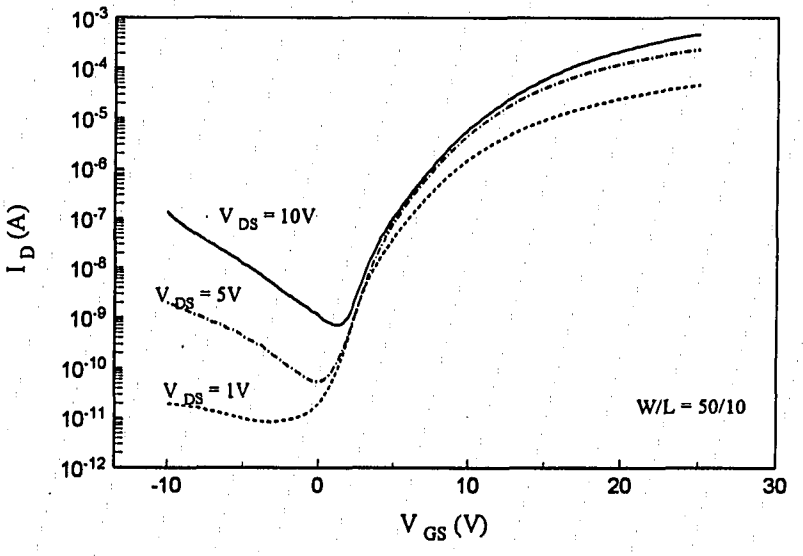


Figure 5-12. Effect of Cobalt Silicide on Thick Polysilicon Device Characteristic

In Figure 5-13, device characteristics for drain voltages of 1, 5, and 10V are shown for (a) cobalt silicided and (b) non-silicided thick island TFTs. There is little improvement in the on current by the silicide. The off current is not increased by the silicidation. For a difference between the silicided and non-silicided devices, either the silicided device needs a thicker silicide, or the non-silicided device must have a higher source sheet resistance. Because these devices were fabricated using diffusion, the source and drain regions are doped to the solid solubility of phosphorous. For ion-implanted fabrication, with lower temperature activation, the sheet resistance would be higher, and the device performance should not be as good as those shown here; the silicided device would then provide a larger on current.



(a) Cobalt Silicided Source and Drain



(b) without Silicide

Figure 5-13. Thick Island TFTs with and without Cobalt Silicide

In Figure 5-14, transfer characteristics of thick polysilicon devices with and without silicide are compared. The concavity of the non-silicided devices at low drain voltage indicates a contact resistance limitation; the silicided device exhibits no such behavior. The Kink effect is not promoted by silicidation.

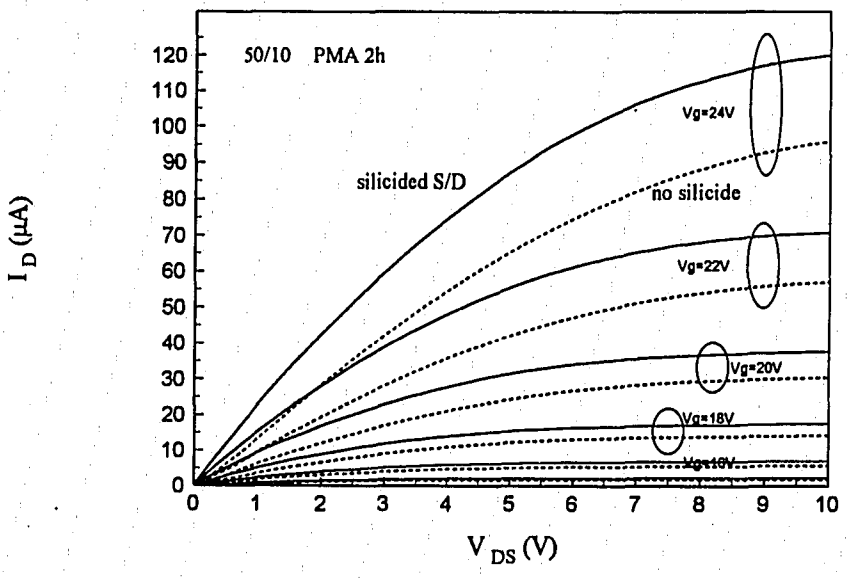


Figure 5-14. Transfer Characteristic of Thick Island Devices with and without Cobalt Silicide

Figure 5-15 shows thin island TFTs with and without cobalt silicide. In the non-silicided device, the on current is limited to about 1.3 μA. The silicided device shows on current similar to the thick island devices, illustrating the removal of the series resistance limitation of the thin island.

Figure 5-16 shows silicided and non-silicided thin island devices at drain bias of 1,5, and 10V. The series resistance limitation of the thin island device remains for high V_{DS},

indicating that the severe current limitation is not primarily due to a high contact resistance resulting from poor processing.

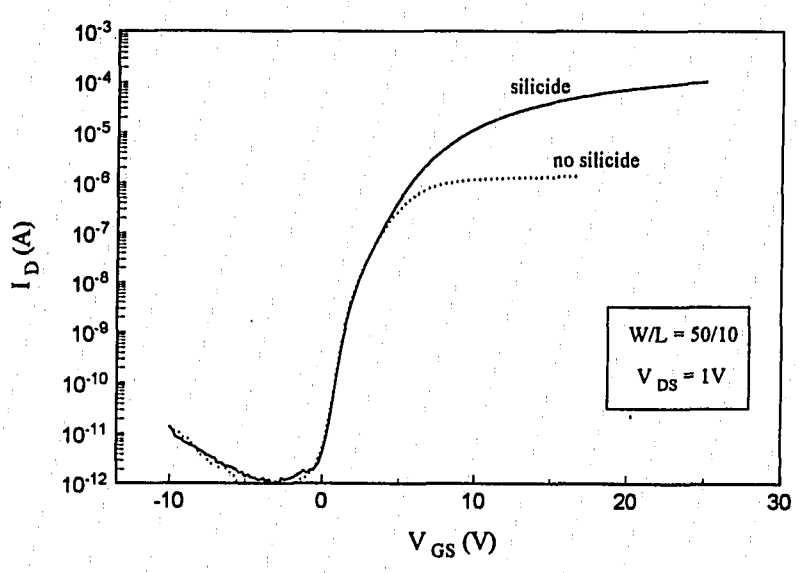
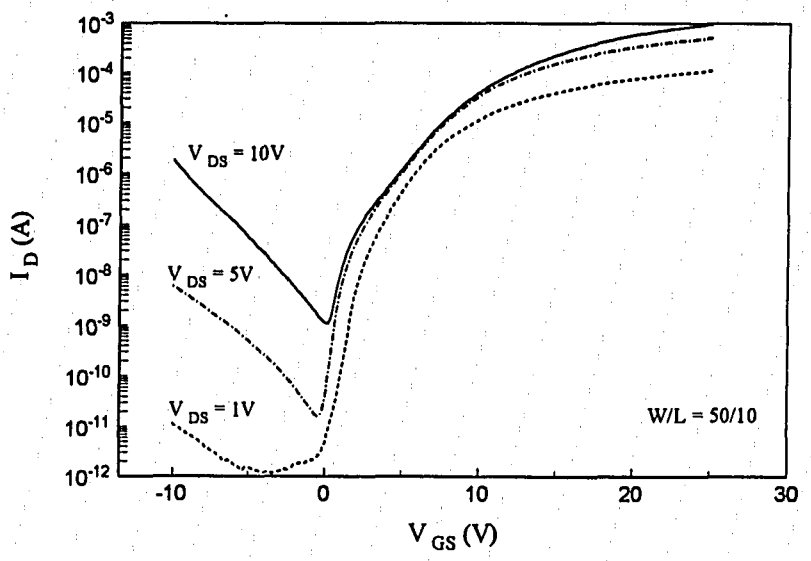
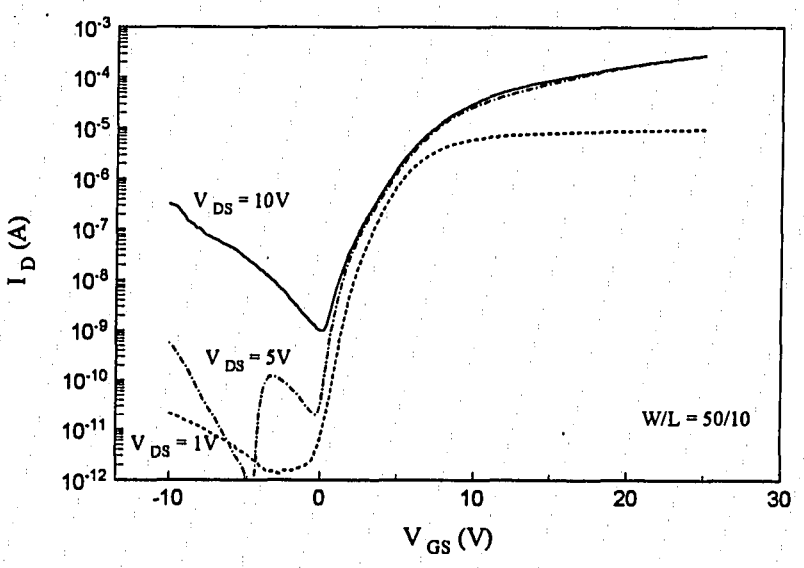


Figure 5-15. Effect of Cobalt Silicide on Thin Polysilicon Device Characteristic



(a) with Cobalt Silicide



(b) without Silicide

Figure 5-16. Thin Island TFTs with and without Cobalt Silicide

Figure 5-17 shows the FET transfer characteristics of thin island devices with and without cobalt silicide. Note that the scale for the drain current of the non-silicided device is on the right, and shows that the difference in current between the silicided and non-silicided device is more than a factor of 10.

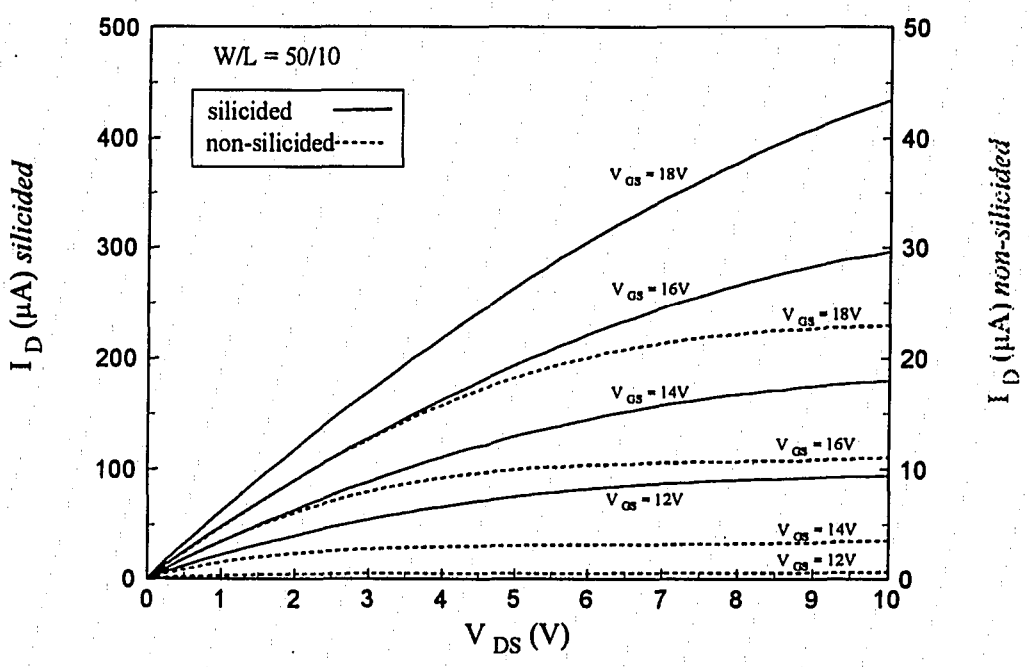


Figure 5-17. Transfer Characteristics of Cobalt Silicided and Non-Silicided Thin Island TFTs

Again, using the analysis of sections 2.6.2, the difference in the extrinsic resistance between silicided and non-silicided devices can be determined from the characteristics in Figure 5-14. Assuming V_{DS0} = 10V, using V_{GS} = 18V, and assuming the silicided device to have current I_{DS0}, then I_{DS0} = 430μA, and I_{DS} = 23μA. Thus, R = 411 kΩ. If the extrinsic resistance R were evenly divided between the source and drain, and

assuming that the majority of the resistance were series resistance (and not contact resistance), the series resistance of the non-silicided device is about 205 kΩ, which agrees well with the value for R_{SD} for the non-silicided device in Table 5-1.

A comparison of non-silicided and cobalt silicided TFTs as a function of island thickness is shown in Figures 5-18 and 5-19.

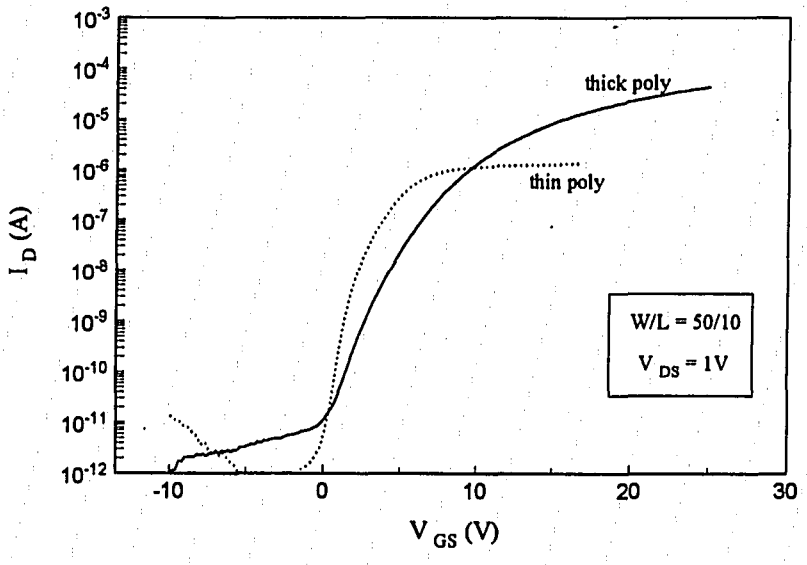


Figure 5-18. Effect of Island Thickness on Non-Silicided TFTs

In both of the non-silicided and cobalt silicided cases, the threshold voltage and subthreshold swing of the thin island device are lower. This supports the theory that a thinner island contains fewer defects to be depleted. The lower number of defects also explains the reduced off-current in the thin island devices. The on-current limitation imposed by the high series resistance of the thin island's source and drain is eliminated by incorporation of a silicide. Because the thin island has fewer defects, its threshold voltage

and subthreshold swing are lower, hence the better characteristic for the thin-island silicided device in comparison to the thick island silicided device.

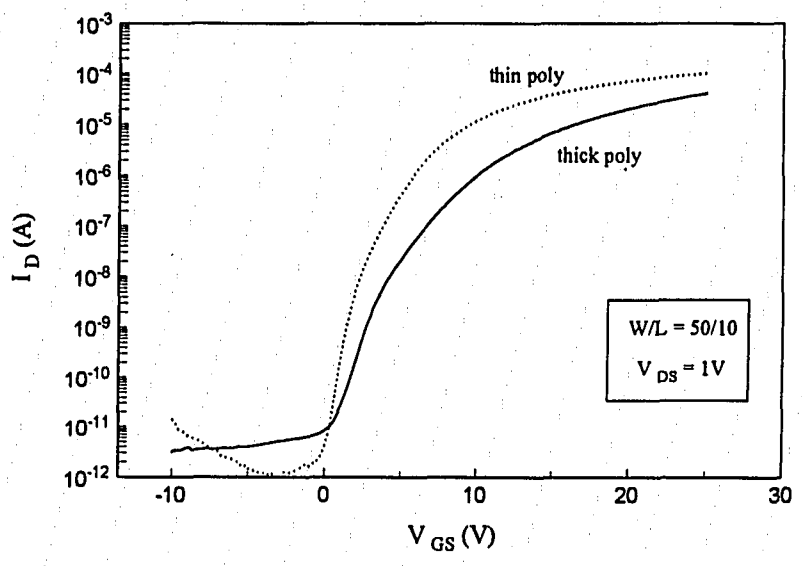


Figure 5-19. Effect of Island Thickness on Cobalt Silicided TFTs

In both of the non-silicided and cobalt silicided cases, the threshold voltage and subthreshold swing of the thin island device are lower. This supports the theory that a thinner island contains fewer defects to be depleted. The lower number of defects also explains the reduced off-current in the thin island devices. The on-current limitation imposed by the high series resistance of the thin island's source and drain is eliminated by incorporation of a silicide. Because the thin island has fewer defects, its threshold voltage and subthreshold swing are lower, hence the better characteristic for the thin-island silicided device in comparison to the thick island silicided device.

5.5.2 Nickel Silicided Devices

The parameters for the nickel silicided devices are listed in Table 5-3. Two thick polysilicon island wafers were silicidized: one with 43Å nickel, the other with 86Å nickel. The subthreshold swings of the devices after the silicidation process were comparable to those of the cobalt process after silicidation; hence forming gas annealing was not performed, also avoiding the possibility that the nickel silicidation reaction would continue and produce the higher-resistance nickel disilicide phase.

island thickness (Å)		μ (cm^2/V-sec)	V_T (V)	S (V/dec-A)
			before silicidation	
600		13	18	1.9
			non-silicided	
600		17	16	1.7
295		$5.8x10^{-4}$?	20	--
	nickel thickness (Å)		silicided	
600	43	19	17	1.5
600	86	31	14	1.3
295	43	31	13	1.2

Table 5-3. Device Parameters from Nickel -Silicided TFT Study

The effect of the nickel silicidation process on thick polysilicon island devices is shown in Figure 5-20. During the 400°C, 10 min silicidation anneal, the threshold voltage and subthreshold swing decrease. These devices were protected from the Ar-plasma, hence the effect is not due to radiation. Since the device characteristics were not degraded in the silicidation anneal, especially in comparison to the cobalt devices, forming gas annealing was not performed on the nickel samples.

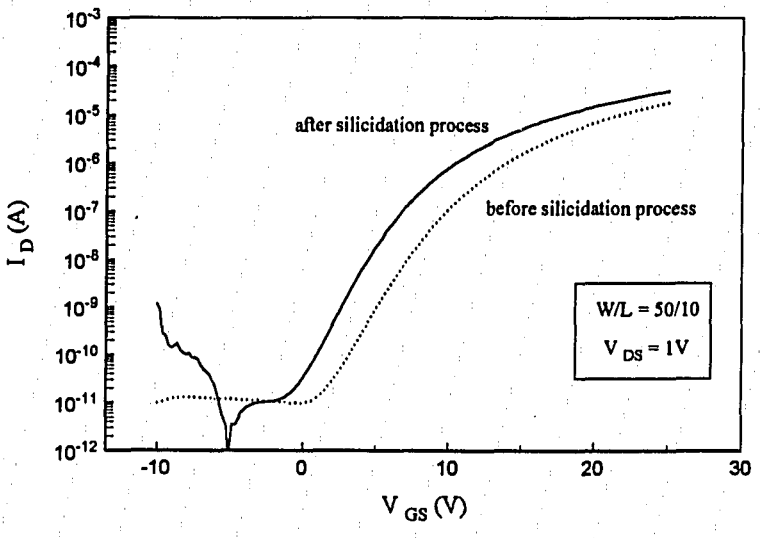


Figure 5-20. Effect of Nickel Silicidation Process on Non-Silicided Thick Polysilicon Devices

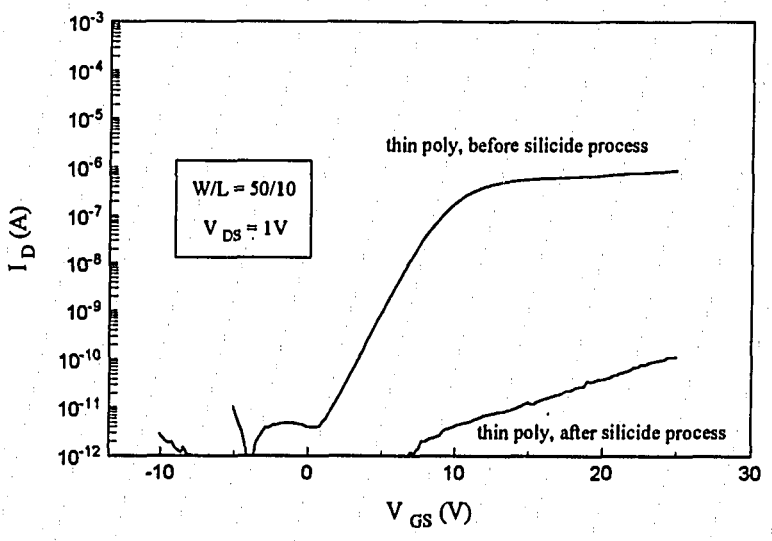


Figure 5-21. Effect of Nickel Silicidation Process on Non-Silicided Thin Polysilicon Devices

The effect of the nickel silicidation process on thin island non-silicided devices is shown in Figure 5-21. The thin, non-silicided islands were damaged to near extinction by the anneal. The drain current was not identical to the gate current; the extremely low conduction is due to serious resistance limitations. The thin polysilicon for the nickel sample was much thinner than the thin island cobalt sample. This effect was also observed in one of the thin-island cobalt silicide runs. However, after forming gas annealing, the conduction disappeared altogether. The thin islands may be susceptible to dissolution in the cleaning and metal-etching procedures.

The effect of the silicidation process on thick island devices with silicide grown from 86Å Ni is shown in Figure 5-22. The mobility is significantly higher, 31 cm^2/V-sec, compared to 13 cm^2/V-sec before silicidation. The threshold voltage is not affected, and the subthreshold swing is reduced.

In Figure 5-23, the FET transfer characteristics for thick island TFTs with nickel silicide grown from 86Å nickel and without nickel silicide are compared. The non-silicided drain current scale is to the right, indicating that the current is half that of the silicided device. Close examination shows that the non-silicided devices suffer a slight limitation from contact resistance, illustrated by a concavity in current at low drain bias.

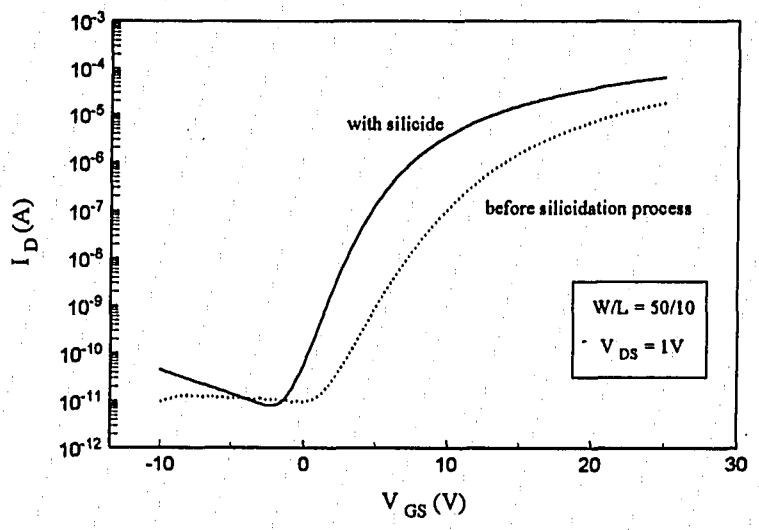


Figure 5-22. Effect of Nickel Silicidation Process on Silicided Thick Polysilicon Devices

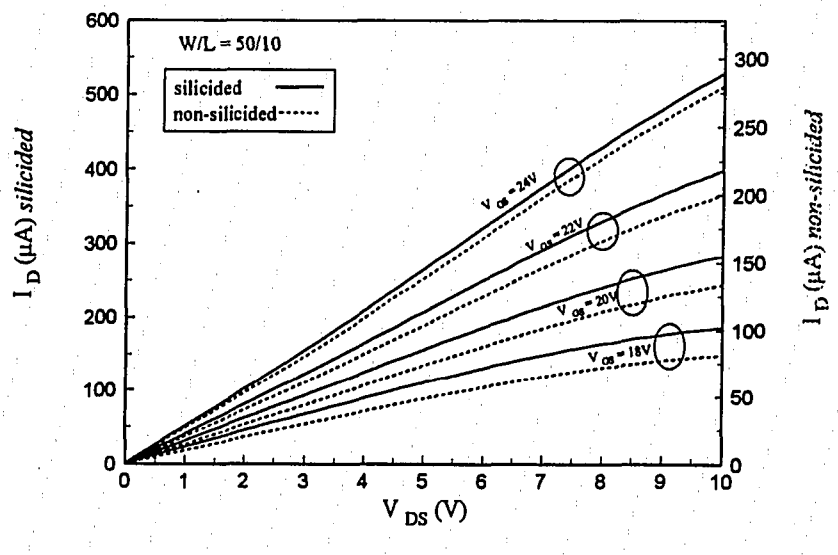


Figure 5-23. Transfer Characteristics of Thick Island TFTs with and without Nickel Silicide

Again, using the analysis of sections 2.6.2, the difference in the extrinsic resistance between silicided and non-silicided devices can be determined from the characteristics in Figure 5-14. Assuming V_{DS0} = 10V, using V_{GS} = 18V, and assuming the silicided device to have current I_{DS0}, then I_{DS0} = 200μA, and I_{DS} = 70μA. Thus, R = 93 kΩ. If the extrinsic resistance R were evenly divided between the source and drain, and assuming that the majority of the resistance were series resistance (and not contact resistance), the series resistance of the non-silicided device is about 47 kΩ, which agrees well with the value for R_{SD} for the non-silicided device in Table 5-1.

Thick island devices with nickel silicide are compared to devices without silicide in Figure 5-24. The subthreshold swing and threshold voltage are lower, and the mobility is higher, for the device with silicide. The silicide does not increase the off current.

Figure 5-25 shows the on-off characteristics for thick island TFTs (a) with and (b) without nickel silicide grown from 46Å nickel with drain bias of 1,5, and 10V. The leakage current is higher in the silicided device because there is less voltage drop in the source and drain regions; hence, there is a higher field at the channel ends for field-emission induced leakage current.

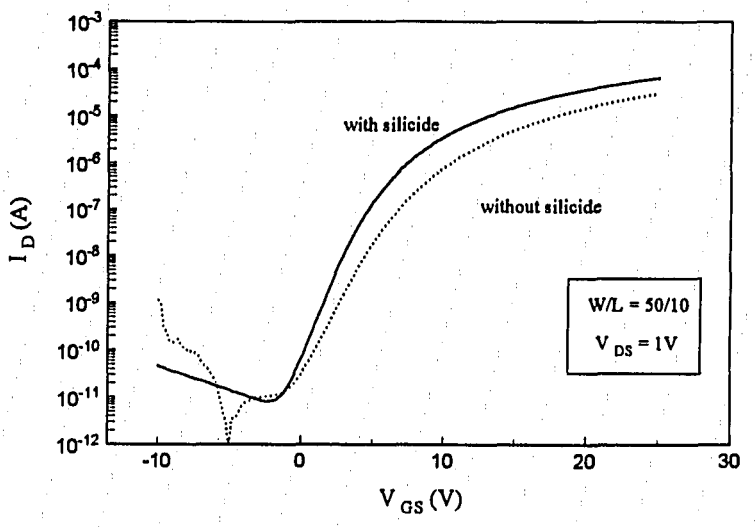
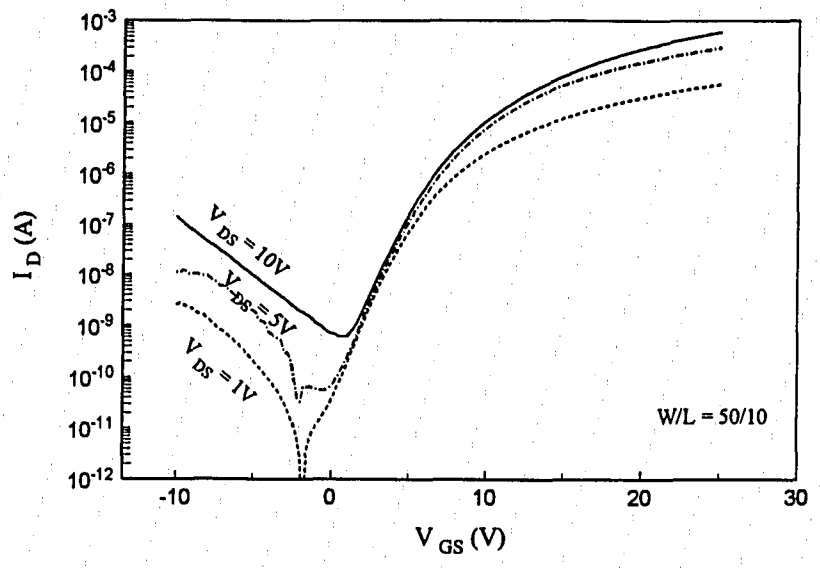
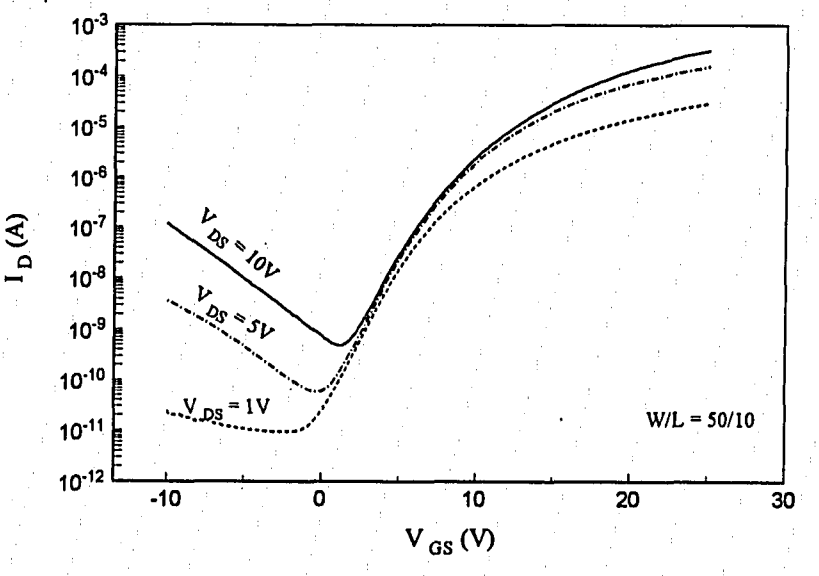


Figure 5-24. Effect of Nickel Silicidation Process on Silicided Thick Polysilicon Devices



(a) Nickel Silicided



(b) non-Silicided

Figure 5-25. Thick Island TFTs with and without Nickel Silicide

The effect of the silicidation process on thin island devices is shown in Figure 5-26. Note that the on-current is limited due to series resistance. The mobility is increased, and the threshold voltage and subthreshold swing are decreased, as in the thick island case. Since no hydrogen annealing was performed, the decrease in the subthreshold swing is due to the decreased series resistance, which causes a voltage drop between the source and drain contacts and the channel ends. As the resistance decreases, the voltage drop in the source and drain is less, hence more of the terminal voltage is applied across the channel, inducing more current.

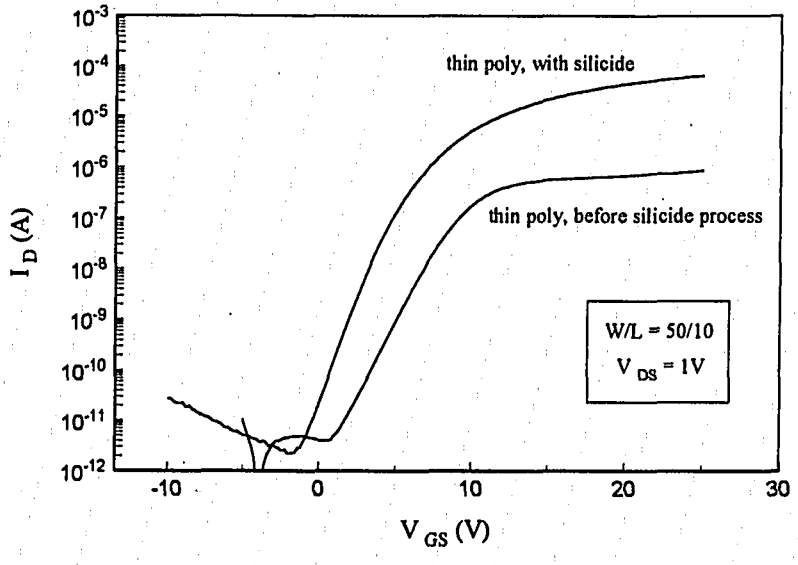


Figure 5-26. Effect of Nickel Silicidation Process on Silicided Thin Polysilicon Devices

Thin island devices with nickel silicide are compared to devices without silicide in Figure 5-27. The silicided device shows strong characteristics, while the non-silicided device does not. The presence of nickel silicide prevents the destruction of the thin island devices. The thin islands are either oxidizing during sputtering, or are dissolved in the nickel etch. If the islands were oxidizing in the sputtering system, then silicide should not form due to the creation of an oxide over any silicon. Obviously, this is not the case, as the sheet resistance of the nickel silicide source and drains is low. Thus, the nickel etch (3:1 H_2O_2:H_2SO_4) must be dissolving the thin polysilicon films.

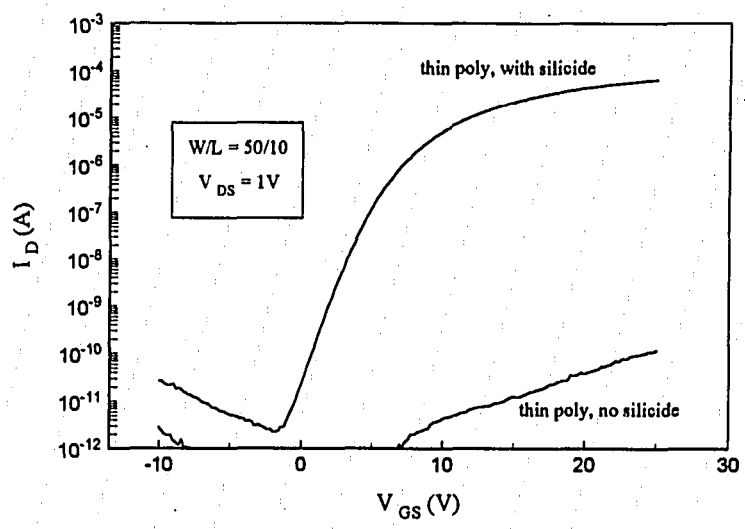


Figure 5-27. Effect of Nickel Silicidation Process on Silicided Thin Polysilicon Devices

The effect of the nickel thickness on device performance is shown in Figure 5-28. On the thin polysilicon island device, only 43Å of nickel were deposited. On thick polysilicon devices, 43 and 86Å of nickel were deposited. Clearly, from the data in Table 5-3, and the characteristics below, the device improves as the nickel silicide consumes the island.

For the thick island case, the thin nickel silicide does not perform much better than the non-silicided device; the mobilities are 17 and 16 cm^2/V-sec, and the threshold voltages are 16 and 17 V. With the thicker nickel film, producing a thicker nickel silicide, the mobility increases to 31 cm^2/V-sec, and the subthreshold swing decreases to 1.3. This effect is due only to the thicker silicide; the silicidation anneal times were the same. The additional minute of plasma exposure to the 86Å sample did not cause any observable damage. Hence, the plasma does not cause significant damage. The thin island device was prepared with only a 43Å nickel film to avoid silicon dissolution. This device performs better than the thick island devices, as there are fewer defects, hence the threshold voltage and subthreshold swing are lower. The device, for a given terminal bias, will perform better as there is less voltage loss between the contacts and channel. The channel is more sensitive to the input gate signal.

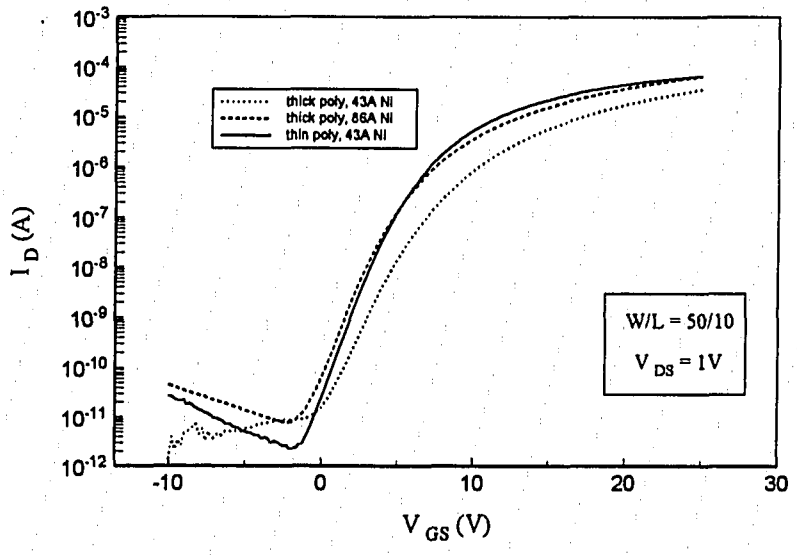


Figure 5-28. Effect of Nickel Thickness on Nickel Silicided TFTs

Figure 5-29 shows device characteristics for thin island TFTs with nickel silicide. Figure 5-30 shows the transfer characteristics of a thin island TFT with nickel silicide. There is no contact resistance limitation, shown by the high currents acheivable at low drain bias. As described earlier, the thin island devices without nickel silicide were damaged, providing no useful characteristics.

Figure 5-31 shows the effect of polysilicon island thickness on nickel silicided TFTs. The off current for the thin island device is less, as is the subthreshold swing. The on-current is higher for the thin island device, probably due to its lower threshold voltage.

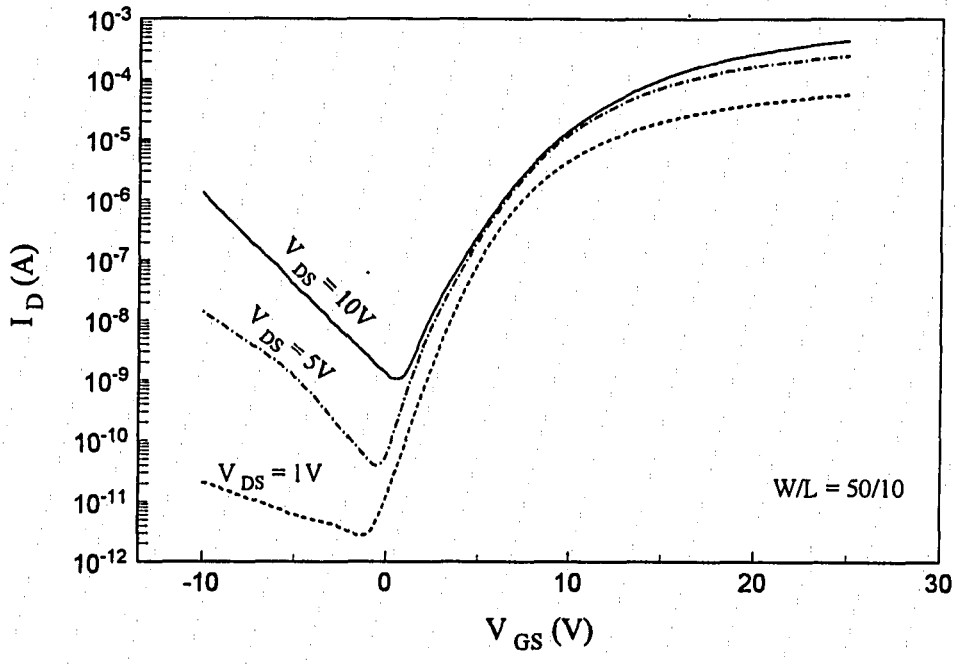


Figure 5-29. Thin Island TFTs with Nickel Silicide

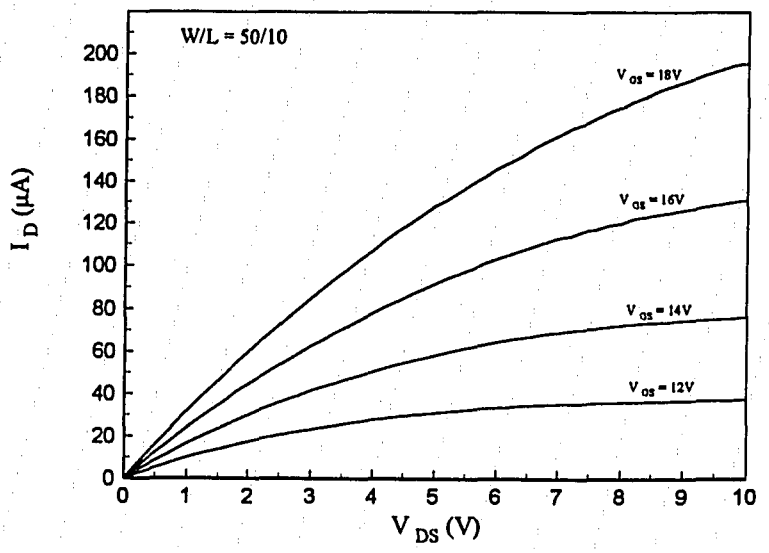


Figure 5-30. Transfer Characteristic of Thin Island Devices with Nickel Silicide

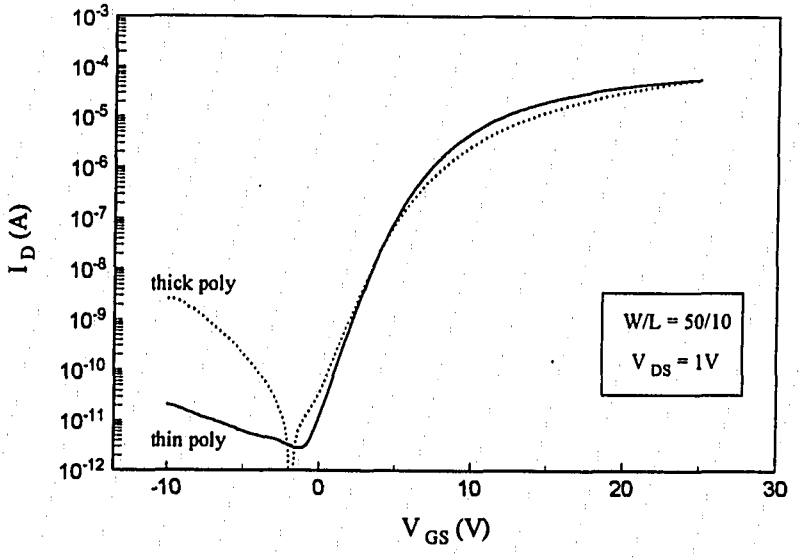


Figure 5-31. Effect of Island Thickness on Nickel Silicided TFTs

5.5.3 Comparison of Cobalt and Nickel Silicided Devices

Thick polysilicon island devices with cobalt and nickel silicided source and drain are shown in Figure 5-32. The nickel device has a significantly higher mobility (31, compared to 22 cm^2/V-sec), and the subthreshold swings are the same at 1.3 V/dec-A. The threshold voltage is lower for the nickel device (14V *vs.* 16V). The threshold voltage for the cobalt device is higher possible due to vestigial damage from the high temperature anneal, not removed by the forming gas treatment. The mobility of the nickel device may be higher due to a lower silicide sheet resistance (10 *vs.* 40 Ω/□, from Table 5-1).

Silicided thin island devices are shown in Figure 5-33. Here, the cobalt device is superior. The very low subthreshold swing suggests that this is due to thorough defect passivation by the forming gas anneal, and not strictly the presence of the silicide, as the non-silicided device also had a low swing. The threshold voltage for the thin island cobalt device was also remarkably low, 9V. Unfortunately, due to series resistance limitations, the threshold voltage for the non-silicided cobalt device could not be extracted. Thus, the superior performance of the thin island cobalt device is due to the forming gas anneal.

Although the nickel devices did not require forming gas annealing to produce reasonable device characteristics, they may improve in forming gas anneals, however, the sheet resistance of the silicides may increase. The longer plasma exposure of the nickel devices did not evince any additional damage. Hence, the plasma does not create as much damage as does the heat of the cobalt silicidation anneal. The lack of thermal damage may explain the good performance of the nickel silicides.

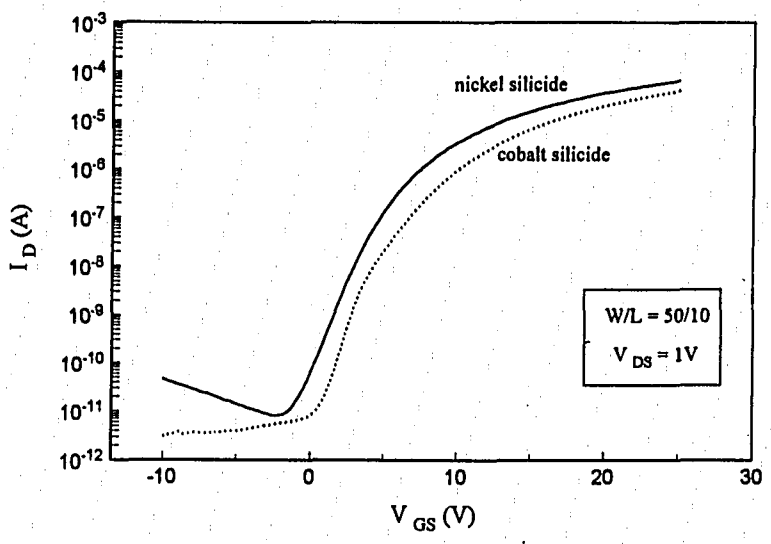


Figure 5-32. Comparison of Cobalt and Nickel Silicided TFTs on Thick Polysilicon Island

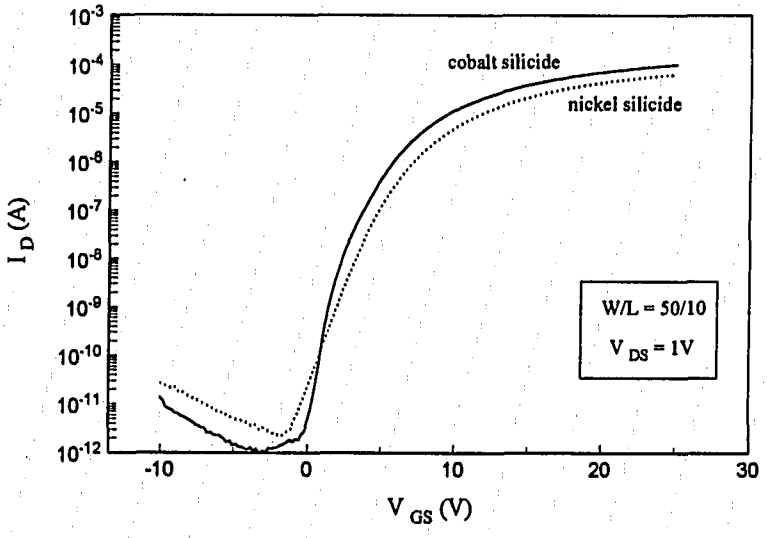


Figure 5-33. Comparison of Cobalt and Nickel Silicided TFTs on Thin Polysilicon Island

Using the subthreshold current expression of Sze [57], the effect of the island thickness, silicidation treatments, and forming gas anneal can be compared by determining the number of electrically active traps. Assuming that the traps in the polysilicon island dominate the subthreshold regime, the subthreshold swing, S, as shown in Figure 5-6, can be described as:

$$S = 2.3\frac{kT}{q}\left(1+\frac{x_{ox}}{\varepsilon_{ox}}\left(qD_t+\frac{\varepsilon_s}{x_{poly}}\right)\right) \tag{5.3}$$

where x_{ox} and x_{poly} are the thicknesses of the gate oxide and island layer.

Using equation 5.3, the density of traps can be compared to determine the effects of the island thickness, silicidation treatments, and forming gas anneal to describe the changes in the performance of the devices. The results are shown in Table 5-4. Using the data for the nickel silicided devices, the island thickness shows no impact on the density of traps. However, because the thinner island has a lesser *volume* of traps, $x_{poly}D_t$, the thinner islands are easier to deplete, hence have a lower subthreshold swing. The presence of a silicide does not significantly affect the trap denisty, when comparing silicided to non-silicided devices of the same island thickness and forming gas anneal (in the case of cobalt).

The cobalt devices show that the anneal at 700°C damages the device, significantly increasing the number of electrically active traps. The forming gas anneal reduces the traps to near the level, in the nickel silicided devices which received no PMA. The cobalt data also show that thinner islands are more efficiently passivated by the hydrogen anneal than the thicker islands. Regardless of the presence of a silicide, the thin island devices exposed to the 700°C anneal show one-tenth the trap density of the thick island devices.

metal	treatment	x_{poly} (Å)	x_{ox} (Å)	S (V/dec-A)	D_t (1/cm^2-eV) x10^{12}
Co	after silicidation	600	900	4.5	16.8
	no PMA	295	700	4.1	18.6
	non-silicided	600	900	1.3	4.96
	after PMA	295	700	0.61	0.668
	$CoSi_2$ S/D	600	900	1.3	4.96
	after PMA	295	700	0.53	0.235
Ni	NiSi	600	900	1.3	4.02
	NiSi	295	700	1.2	3.96

Table 5-4. Comparative Trap Densities

5.6 Mobility Correction

The Chern method for mobility correction as described in Section 4.5.1 was used to determine the lateral diffusion of dopant under the gate caused by the wet-etching of the polysilicon gate stripe, the $POCl_3$ diffusion, and the silicidation treatments. Also, the extrinsic resistances of devices with and without silicide can be compared using this method. An example of the determination of the channel length factor ΔL and extrinsic resistance R_{ext} is shown in Figure 5-34, which shows the Chern measurements for a non-silicided thick island TFT without PMA. Because it was observed that the threshold voltages were dependent on the device process, and it was noted during the Chern measurements that the threshold voltage was a minor function of gate length, the gate-to-source voltages were taken for all devices to be $V_T + V_{DS} + 5V$, $V_T + V_{DS} + 7V$, and $V_T + V_{DS} + 9V$, with $V_{DS} = 1V$, as shown in Figure 5-34.

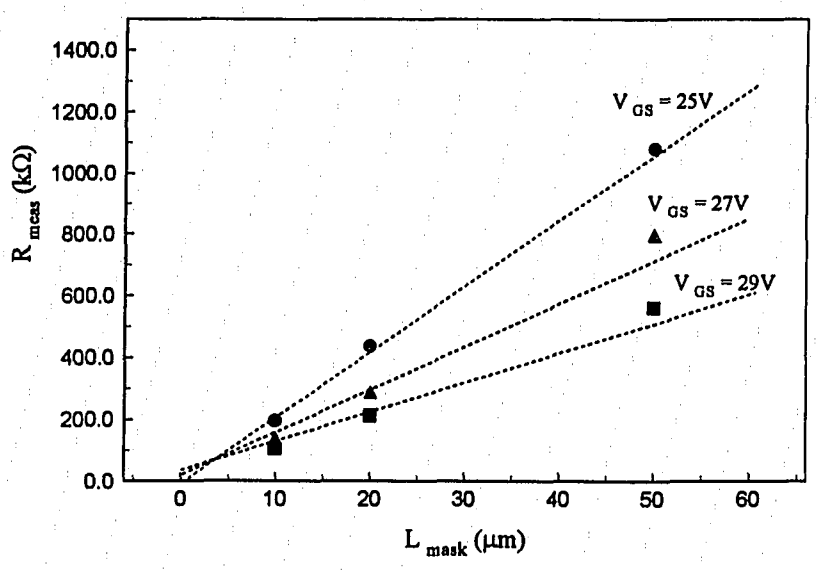


Figure 5-34. Chern Method for Channel Correction Factor and Extrinsic Resistance Determination for Non-Silicided Device.

The channel length and extrinsic resistance factors determined by the Chern method are summarized in Table 5-4. The devices measured had widths of 20 μm. The channel lengths were 10, 20, and 50 μm.

The silicided and non-silicided devices show a high extrinsic resistance. This may be due to the low-doped region of lateral dopant diffusion under the gate, which adds a series resistance to the devices regardless of silicidation. The resistance intersection was highly non-reproducible from one series of devices to another; the results listed in Table 5-4 show the typical trend. The as-measured" mobility, μ_{meas}, are from Tables 5-2 and 5-3. Devices listed as "w/o silicide" are those measured on the silicided wafer on the covered (non-silicided) portion. These devices undergo the same annealing and passivation (in the case of cobalt) as the silicided devices. The "after $POCl_3$" listing is

used to determine the effects of the silicidation anneals. Reliable devices on the thin island non-nickel-silicided sample were not found.

	μ_{meas} (cm^2/V-sec)	R_{ext} (kΩ)	ΔL (μm)	μ_{corr} (cm^2/V-sec)
thick (600Å) island				
after $POCl_3$	14	24	0.137	13
w/o $CoSi_2$	22	26	2.26	17
$CoSi_2$	22	25	3.05	15
w/o NiSi (43Å Ni)	13	38	1.11	12
NiSi (43Å Ni)	19	24	1.07	17
w/o NiSi (86Å Ni)	13	80	1.27	11
NiSi (86Å Ni)	31	18	1.66	26
thin (200Å) island				
w/o NiSi	n/a			
NiSi (43Å Ni)	31	8	1.44	27
w/o $CoSi_2$	(1)	917	2.45	--
$CoSi_2$	27	18	2.46	20

Table 5-5. Chern Measurement Parameters for Silicided and Non-Silicided TFTs

The wafer-to-wafer variation in non-silicided extrinsic resistance is due to the non-reproducibility of the measurement, and minor variation in deposited silicon thickness during island LPCVD. The extrinsic resistance for silicided devices is lower than those of the non-silicided devices. The most notable is in the thin island case of cobalt. The non-silicided mobility measurement was meaningless due to the severe series resistance limitation-- the extrinsic series resistance of nearly 1MΩ limited the current to about 1μA. The silicided thin island devices had extrinsic resistances similar to the silicided thick island devices. Thus, the series resistance limitation of thin island devices is again shown to be removed by silicidation.

It is not conclusive whether the metal affects lateral junction rediffusion during the silicidation anneal. Thus it is the temperature, and not the presence of silicidation-induced stress or silicon vacancies, which drives the rediffusion. The nickel devices show a

smaller channel length factor than the cobalt devices, probably due to the lower anneal temperature. The island thickness did not appear to affect the channel length factor.

5.7 Conclusions

Cobalt and nickel silicides were fabricated on thin (< 600Å) polysilicon films with sheet resistances as low as 20 Ω/□. For ultra-thin (< 200Å) polysilicon films, the sheet resistance of the silicide is exceptionally high, though it is significantly less (< 1%) than the sheet resistance of doped polysilicon. Ultra-thin polysilicon films exhibit dissolution during cleaning and etching of metal films, and during processing. Silicides, as in the case of the thin-island nickel sample, may protect the island from dissolution.

Self-aligned thin and ultra-thin film transistors in polysilicon were fabricated for the first time using cobalt and nickel silicides. A low-temperature process sequence would require a spacer etch, similar to the LDD-spacer in salicide CMOS processes in order to prevent silicide-channel shorting. Otherwise, the fabrication sequence used herein is compatible with TFT-LCD processing.

Cobalt silicided TFTs require annealing in hydrogen to remove damage from the silicidation step. The majority of the damage is from the heat of silicidation, not the sputtering plasma. Nickel silicided TFTs did not require hydrogen anneals. Silicided TFT characteristics are dependent on the thickness of the silicide, and its relation to the sheet resistances of the source and drain, and the channel. For highly-doped, thick sources and drains, silicides may not provide improvement. For ultra-thin TFTs, silicides are required to eliminate the series-resistance limitation of the on current.

Using a subthreshold conduction model, the trap denities of the islands were computed to compare island thickness and silicidation treatments for their impact on the defects in the island. It was confirmed that the cobalt silicidation anneal damages the film, increasing the defect density. Forming gas annealing reduced the trap density.

Thinner islands were shown to be more efficiently passivated by forming gas annealing. The silicides by themselves did not increase the number of traps; the trap density for similarly prepared devices except for the presence of a silicide were reasonably the same.

Ultra-thin TFTs were shown to have a lower subthreshold swing, threshold voltage, and off current, supporting the theory that these parameters are dominated by the volume of defects in the channel. The mobility was not seen to be a function of film thickness. Ultra-thin TFTs were shown to have device characteristics similar to thicker island TFTs, but have lower threshold voltages, which make them a better choice for integrated driver circuitry, which will be discussed in the following Chapter.

Chapter 6
Silicides in Active Matrix Liquid Crystal Display Design

In this chapter, the design of driving circuits for AMLCDs will be discussed. The electrical load and response of the display will be determined and used in the mathematical analysis for the design of display driver circuits. Circuits which are incorporated in state-of-the-art data driving circuits-- digital-to-analog converters and amplifiers-- will be presented. It will be shown that the most important factor of the drive circuits is the temporal response. This motivates the circuit design and the device process towards maximizing the TFT drive current, and places constraints on the materials viable for signal lines in the display.

The anticipated effects of the incorporation of silicides in the TFT circuit fabrication process will be simulated. Expected improvements are an increase the drive current and reduction in the duration of the display signal transients.

6.1 General Operation

The display is similar to a capacitor-based dynamic RAM. The pixel electrode is the capacitive element, composed of the capacitance of the liquid crystal between the transparent metal electrodes and a "storage" capacitance (described below). The pixels are addressed by their row (or *scan*) line and column (or *data*) line. In an active-matrix liquid crystal display, the pixels are isolated by a TFT pass transistor between the data line and the pixel electrode. Figure 6-1 shows the physical layout of a TFT-switched pixel and its equivalent circuit.

When a row is turned on, or is scanned, the voltage on the scan line turns all of the TFTs of that row on. The data line voltage can then be passed through the pixel TFT onto the pixel electrode. The voltage difference between that of the pixel electrode and

the common voltage on the opposing glass plate creates an electric field across the liquid crystal within the area of the pixel. The transmission of light through the pixel area is modulated by the applied data voltage (Figure 1-5) [6].

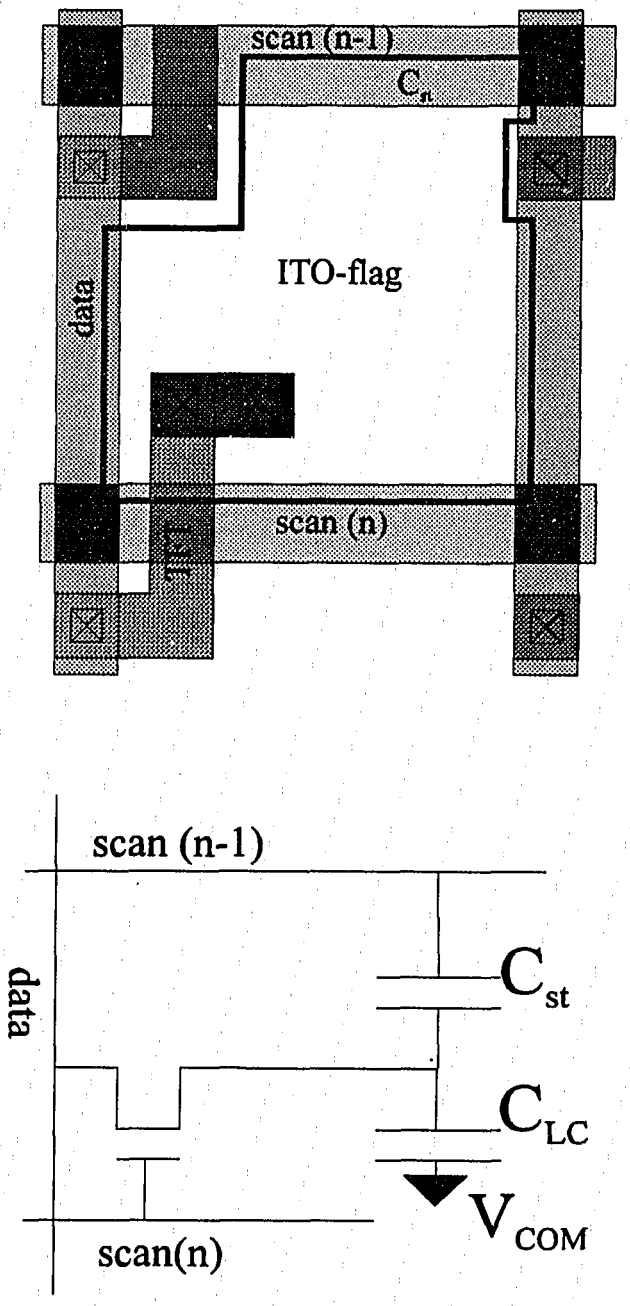


Figure 6-1. Layout and equivalent circuit of pixel in TFT-LCD.

6.1.1 Scan Theory in Active Matrix Displays

In active-matrix LCDs, only one row is driven at a time. Conceptually, the scan driver is essentially a shift register, where the "on" line shifts from one line to the next. When the scanned line is driven into the "on" state, its voltage is driven high enough to turn on the pixel TFTs, allowing the data to be written to the pixels. The selected line scrolls down the display sequentially, once per image frame.

Since the output of the scan driver is the gate voltage of the pixel TFTs, which are pass transistors between the data driver and the target pixel, the output voltage of the scan line in the selected state must be at least a threshold voltage above the highest data voltage. Hence, a high voltage needs to be output. High-voltage shift registers have been made, but the increased voltage swing of the shift register cells requires higher current, hence larger-area devices and capacitive loading. A more efficient method is to have a low voltage shift register, with the output of each stage fed to a level-shifter whose function is to raise the "on" voltage from the logical-on level to the scan-select on-level [11,16,76]. In Figure 6-2, a 5V shift register is connected to level shifters to bring the line select voltage up to 20V.

The capacitance of the scan line is the sum of the data line overlaps, pixel gates, and any overlap of source and drain regions, black matrix, liquid crystal capacitance to the common plane, and other design parasitics. The scan line also has a very high L/W. Since it cannot be made of an arbitrarily thick conductor, it has a non-negligible resistance. The level-shifter may not be able to solely produce enough current to quickly bring the line to the select voltage. Multi-staged buffers, essentially inverters with power supply voltages of the off (ground) and on (select) voltages are placed between the level shifter and the display to charge or discharge the line quickly. Figure 6-3 shows a TFT scan drive circuit for one line, including shift register cell, level shifter, and buffer, using CMOS-based circuit architecture.

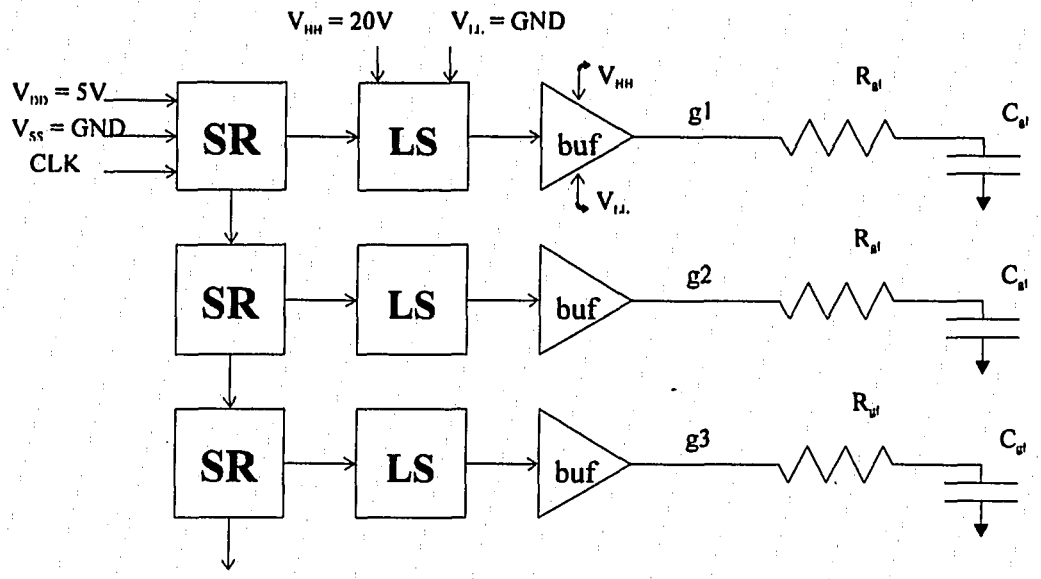


Figure 6-2. Concept of scan driver for AMLCD.

6.1.2 Scan Line Resistivity

The gate line material has serious constraints regarding its thickness and resistance. Because subsequent films are deposited over the gate line, it cannot be arbitrarily thick. Since it is relatively thin, it may be highly resistive. The gate line must also withstand thermal treatments after its deposition. Hence, aluminum, with one of the lowest conductor resistivities, cannot be used in the case of polysilicon TFTs with self-aligned source and drain implants. Instead, refractory metals and silicides are used as the scan lines in displays [18,76,77]. Assuming a lumped-RC model for the scan line resistance and capacitance, a conservative maximum resistivity value can be determined.

For a monochrome VGA display (640 rows, 480 columns), the resistance of the gate line, R_{gl}, and the gate line period, can be written in terms of the gate line sheet resistance $R_{S\,gl}$:

$$R_{gl} = R_{sgl}\frac{L}{W} = R_{sgl}\frac{640 \cdot pitch}{gate\,linewidth} \qquad (6.1)$$

The gate line period, t_{gl}, is given in terms of the image frame rate (*frate*):

$$t_{gl} = \frac{1}{frate}\frac{1}{480} \tag{6.2}$$

The gate line should be nearly fully charged for the majority of the line time. Since data lines are divided into blocks, or *datagroups*, so that there are simultaneous data lines written within each block, the scan line must be on for the majority of the first data block period. The data block period is a fraction ($\frac{1}{datagroups}$) of the line time. The rise time of the gate line is 3RC, where C is the scan line capacitance. Allowing for 90% charging within the first data period, The gate line rise time can be defined as:

$$\tau'_{gl} \equiv 3R_{gl}C_{gl} < \frac{1}{3}t_{gl}\frac{1}{datagroups} \tag{6.3}$$

Using equations 6.2 and 6.3, the maximum sheet resistance of the gate line is then:

$$R_{sgl} < \frac{1}{9}\frac{W}{L}\frac{1}{frate}\frac{1}{480}\frac{1}{datagroups}\frac{1}{C_{gl}} \tag{6.4}$$

With a pitch of 48μm, a gate linewidth of 8μm, a frame rate of 60 Hz, a gate line capacitance of 100pF, and 20 datagroups, the maximum sheet resistance is then 2Ω/□. For a gate line thickness of 2000Å, the maximum resistivity of the gate line is 40μΩ-cm. This value is achievable with sputtered and CVD tungsten silicide [18].

Since the gate line is more accurately a transmission line than a lump RC network, this analysis gives a conservatively low maximum resistivity. Also, pixels of the first data block, which is near the gate driver, will be turned on before those in the later blocks farther down the gate line. The current drive should ensure that by the second data block period, the line has become fully charged.

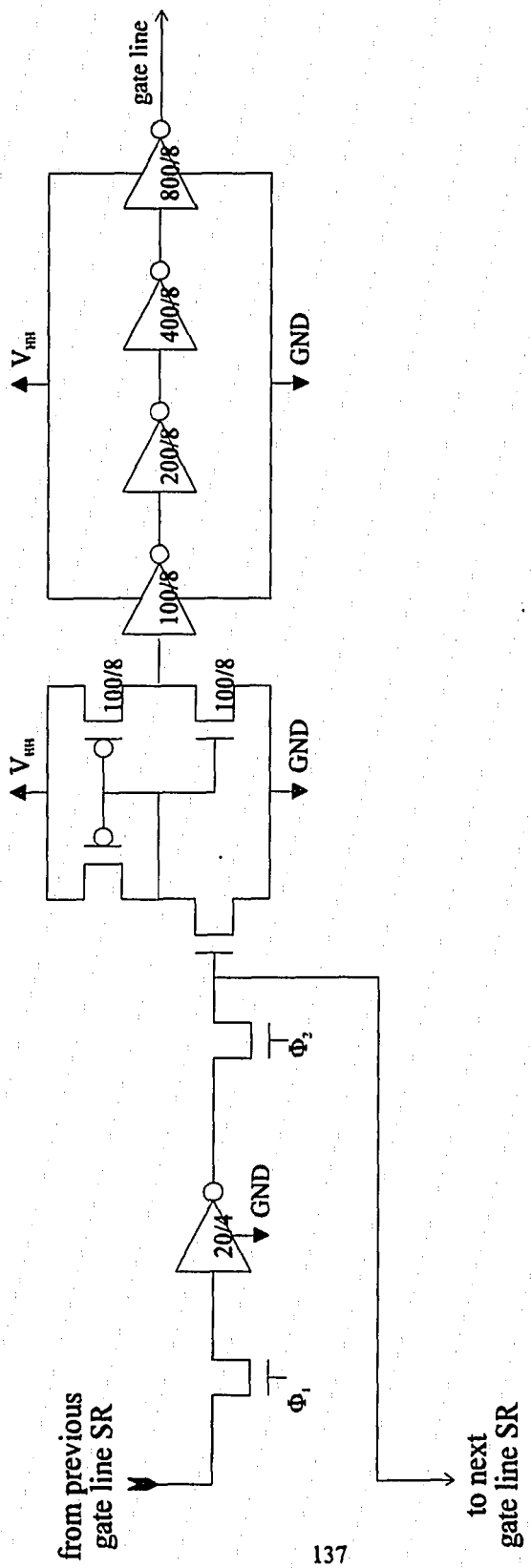


Figure 6-3. Dynamic Scan Driver Circuit for Gate Line

6.1.3 Data Driving Theory in Active Matrix Displays

Producing an image on the display is a matter of applying voltages on the arranged pixel electrodes to produce electric fields to appropriately modulate light transmission through the pixel TN cells. The image is re-written many times per second, according to the *frame rate*. The role of data drivers is to provide current to charge up the data line. All of the pixels on a row must have their data written before the row is turned off, when the next row is written. In a non-interlaced display, the rows are written sequentially each frame. In an interlaced display, the odd lines are written one frame, then the even on the next. Because of their superior image quality, non-interlaced displays are becoming the norm.

The time to write the pixel is a function of the number of rows and columns, and on the driving scheme. Three cases of data transmission on a monochrome VGA (480 rows x 640 columns) display with a frame rate of 60 Hz are described and compared below: serial, line-at-a-time, and blocked data.

6.1.3.1 Serial Data

The classic example of serial data is a cathode ray tube (CRT). The electron beam sweeps across each phosphorescent pixel in raster-scan method. The beam current is analog-controlled for varied pixel phosphor emission intensity. If each pixel were to have a different gray level, the response time of the beam must be:

$$t = \frac{1}{640 \cdot 480 \cdot 60\ \text{Hz}} = 54\ \text{nsec} \qquad (6.5)$$

corresponding to a data-frequency of 18 MHz. In a TFT-LCD, the data would need to be manipulated to go to the proper column, and the data line charged. Since this involves multiple stages of circuit function, each stage would need to operate much faster.

Integrated TFT circuits cannot yet operate that quickly. Thus, connecting "one wire" of data input to a glass panel and seeing its video image is quite unlikely in the near future.

6.1.3.2 Line-at-a-Time Data

An example of line-at-a-time data is an amorphous-silicon TFT laptop LCD. The row and column lines on the display are brought to pads for connection to external circuitry. The data drivers are integrated circuits on single-crystal silicon, with connections made by either Chip On Glass (COG) or Tape Automated Bonding (TAB) technologies [78]. The chips, called column drivers, receive digital-word input, convert the word to an analog voltage by a digital-to-analog converter, then put the voltage into a unity gain amplifier to increase the output current. The response time of the column driver output must only provide current enough to charge the data line in a fraction (*e.g.* $\frac{1}{3}$) of the row time:

$$t = \frac{1}{3}\,\frac{1}{480 \cdot 60\ \text{Hz}} = 11.5\mu\text{sec} \tag{6.6}$$

The advantage of this technology is that low-power, high-speed, high-current single-crystal CMOS circuitry can be used. The drawback is the number of connections required. For a color VGA display, there must be $3 \times 640 = 1920$ data connections. This high number of connections increases production cost. Also, TAB and COG technologies are not readily applicable to small-area, high content displays, such as LCD projection light valves, where the data lines are close due to the small pitch of the pixels. This causes the linear density of data connections to be too small for TAB and COG technologies [4,79].

6.1.3.3 Blocked Data

In this scheme, pixels are written in sequential blocks of parallel data. Figure 6-4 is an example of a display where the 640 data lines are partitioned into 32 blocks, each 20 lines wide. In each *block period*, 20 data lines are written at once. The lines which are written are selected by the *block control signal*. Hence, there must be 52 data inputs: 32 for analog data, 20 for block selection.

The production of high-current analog voltages to drive the data lines can be produced by external ICs or integrated TFT circuits. The block control signals, produced by a simple decoder or shift register, can be produced similarly.

The time that the data voltages must be ready is a function of the number of blocks. The critical block is the first one, which is being written while the gate line is still charging to its ON state. Note that as the number of blocks increases, the serial scheme is approached. And, as the number of blocks goes to one, the line-at-a-time case is approached. With *blocks* = 20, the response time of the data driver output must only provide current enough to charge the data line in a fraction (*e.g.* $\frac{1}{3}$) of the block time is:

$$t = \frac{1}{3} \frac{1}{480 \cdot \left(\frac{640}{blocks}\right) \cdot 60\text{Hz}} = 361 \text{ nsec} \qquad (6.7)$$

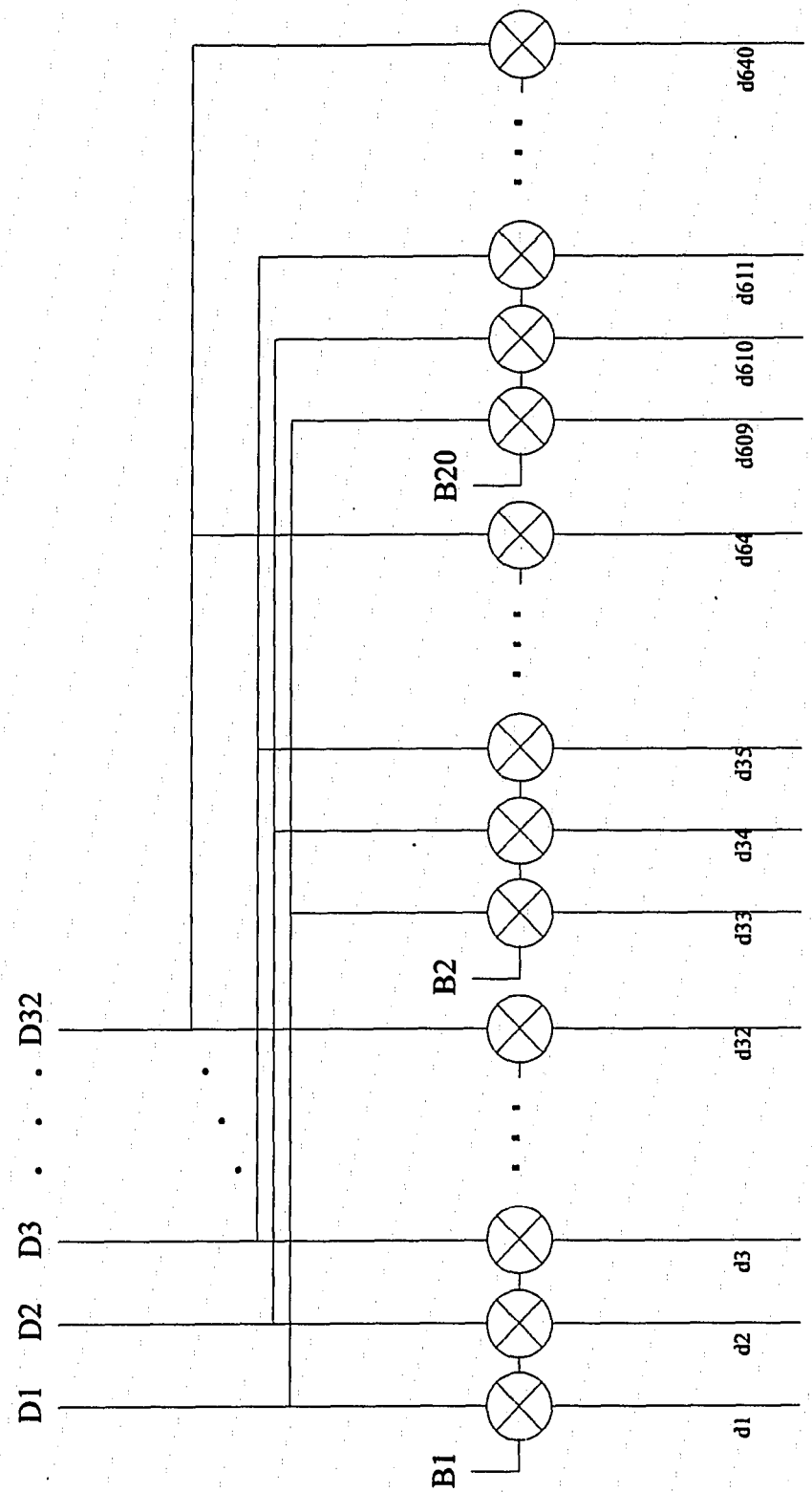


Figure 6-4. Block-Data Driving Scheme

6.1.4 Data Inversion

Since the liquid crystal material contains impurities, the field across the gap must be reversed periodically to prevent migration of the impurities towards the electrodes, which can cause field termination and result in poor image quality [80]. Because the liquid crystal is bi-directional, the transmission-vs.- field characteristic is an even function; the molecule will be tilted equally by a field of +10kV/cm as it would by -10kV/cm (4V across the 4μm cell gap). The simple case of a "fixed common voltage," where the unpatterned transparent electrode is fixed at a given voltage, V_{COM} will be discussed here. In this case, the data voltages are in two ranges, above and below V_{COM}, as illustrated in Figure 6-5. Above V_{COM}, the gray scales increase with increasing voltage, as the field increases, decreasing transmission through the normally-on TN cell. These data voltages are the "+data" voltages, and affect the transmission of the liquid crystal as shown in Figure 1-5.

The "-data" gray scales are reversed, since the field increases with decreasing data voltage. Note that a given gray scale in Figure 6-5 has the same electric field value E_{gs} in +data and -data modes because the electro-optic response of the of the TN cell is even, as shown in figure 6-5 and described in equation 6.8:

$$E_{gs} = \left| \frac{V_{pixel} - V_{COM}}{d_{gap}} \right| \tag{6.8}$$

The polarity of the liquid-crystal electric field is reversed each frame by writing data voltages above and then below the common voltage, V_{COM}. Due to the frame-inversion of the data voltages, the voltage swing can be large, up to 20 V. Since the time for data writing is short, the average current the data drivers must supply is large:

$$I_{avg} = C_{dl}\left(\frac{\Delta V}{\Delta t}\right) \tag{6.9}$$

If the data line capacitance is 100 pF, the voltage swing a maximum of 20 V, and the time needed to energize the data line is 361 nsec as given by eq. 6.7, then the average current is 5.6 mA. Since the current through the data driver is not constant, the device must be designed to be larger to accommodate the initial "peak" current.

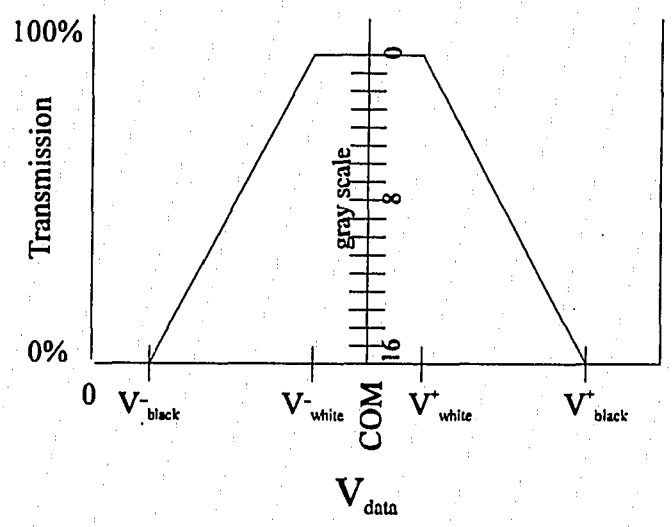


Figure 6-5. Data voltage ranges in "fixed-COM" data-driving scheme.

6.2 Scan Circuitry

This section illustrates the components of the scan driver: shift register, level shifter, and line driver.

6.2.1 Shift Registers

The shift register is simply a clocked, serial memory device. A sample shift register is shown in Figure 6-6, taken from Figure 6-3. This shift register design is the simplest: static register with dual non-overlapping clocks. Other shift register designs have been proposed and examined for their utility in AMLCD design, and are described in another thesis regarding AMLCDs at Lehigh University's Display Research Laboratory [81].

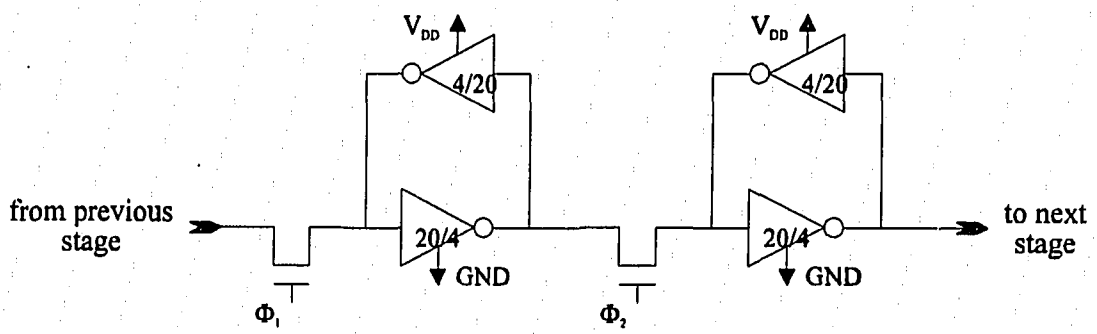


Figure 6-6. Static Shift Register Design

6.2.2 Level Shifters

The necessity of the level-shifter is to ensure that the scan line ON-voltage is high enough to keep the pixel TFT in the linear mode, so that there is no source-follower threshold voltage loss on data voltage transferal to the pixel. CMOS and nMOS designs are considered below.

6.2.2.1 CMOS Designs

Two CMOS non-inverting level shifters are shown in Figures 6-7 and 6-8. They are based on a differentiating input pair. The difference is in the generation of the gate signal to the output pull-down nTFT. In Figure 6-7, the signal is the internally generated inverse of the input signal, which comes from the low-voltage shift register. This signal will have a logic high value near V_{HH}.

Simulations were performed using Aim-Spice, a circuit simulator from University of Virginia, which models the polysilicon TFT with a floating body. The device parameters used to optimize the circuit design for th most robust operation were: μ_n and μ_p of 10 cm^2/V-sec, V_{Tn} = 2V, and V_{Tp} = -2V. The output load was 1kΩ and 350 fF, simulating the source sheet resistance and gate capacitances of a two-transistor load, similar to the input of a CMOS inverter with 50x10 μm^2 gates.

The simulated rise time dependence of the circuit in Figure 6-7 on the aspect ratio of the output devices is summarized in Table 6-1. The input stage aspect ratio was 5/10. The rise time increases for increasing device area because of the load it presents to the inverted input signal.

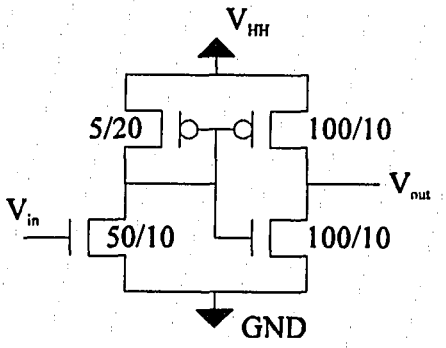


Figure 6-7. CMOS Level Shifter

W/L output TFTs	90% rise time (μsec)
100/10	1
500/10	3
1000/10	6

Table 6-1. CMOS Level Shifter Rise Time Dependence on Output Stage Size

The rise and fall time of the output was found to be a function of the input pTFT pull-up aspect ratio. If this device had a high W/L ratio, the voltage drop across it would be insufficient to cause the source voltage to be well below V_{Tn} so that the output pull-down device cannot be turned off. Hence, there would be a parasitic pull-down at the output node, which would decrease V_{OH}. If the device were too highly resistive (too low aspect ratio), the internal nodal voltage would not rise quickly, and would slow down the fall time of the output. With the output stage sized as 100/10, the simulated rise time of the output as a function of the pTFT pull-up is shown in Table 6-2.

W/L input pull-up	90% rise time (μsec)
5/40	1
5/20	0.9
5/10	1

Table 6-2. CMOS Level Shifter Rise Time Dependence on Input Pull-up Size

The level shifter shown in Figure 6-8 avoids the problems associated with sizing of the pull-up device. However, the gate voltage of the output pull-down nTFT will be less than in the circuit of Figure 6-7, because the logic high value of the shift register output is only V_{DD}. This may reduce the ability of the device to discharge the driven node at

V_{out}. It may also present a capacitive load to the shift register, especially if the inverse of the shift register output is to be obtained from the weaker "feedback" inverter. Depending on the architecture of the shift register, the signal to that device may arrive quicker than if it were to be generated by the circuit in Figure 6-7.

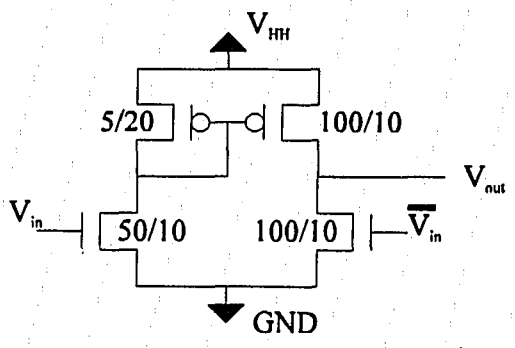


Figure 6-8. Modified CMOS Level Shifter

6.2.2.2 nMOS Design

An nMOS up-shifter is essentially an inverter pair with the drain voltage, V_{DD}, increased to the up-shifted level, V_{HH}. A non-inverting nMOS up-shifter is shown in Figure 6-9. Note that the output pole can serve as the first stage of a multi-stage nMOS buffer.

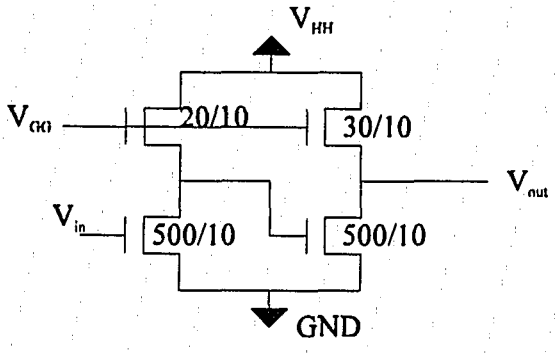


Figure 6-9. nMOS Level Shifter

The performance of the nMOS level shifter was much poorer than the CMOS shifters due to the larger device areas which provided increased capacitances. The pull-down transistors need to be wide because the pull-up transistors are always on; the output voltage of the pole will be a fraction of V_{HH} respective to the ratio of the pull-up and pull-down devices. Increasing the ratio of the pull-up to the pull-down device will decrease the rise time, but increase the output low voltage. Similarly, decreasing the size of the pull-up device will reduce the output low voltage, but will increase the rise time. This problem is common to the nMOS level shifter and buffer, since they are essentially the same devices. The response time and the output high levels of the nMOS circuit are more susceptible to threshold voltage variations.

Using the same parameters as in the CMOS circuit, the rise time was longer than 10μsec, whereas the fall time was less than 1μsec. Attempting to tailor the pull-up and pull-down on a pole-by-pole basis to optimize the final output to have a rapid rise or fall time can be done. However, the opposing edge (fall or rise, *resp.*) would be excessively slow. Due to the slow response, and the static current, the nMOS shifters are inferior to the CMOS circuits. Their only advantage is the reduction in processing complexity by elimination of the n- and p- implant masking process steps.

6.2.3 Line Drivers

The output pole of the level shifters is essentially an inverter. This can serve as the first stage in a multi-stage buffer. Multi-stage buffers of CMOS and nMOS types are discussed below. Because the scan line is driven to either of two voltages, the on and off levels, which can be set to the voltage supplies of the level shifter, the scan driver is a series of logic inverters which output either the scan select on or off levels

6.2.3.1 CMOS Design

CMOS inverters output the power supply voltage for the output high voltage, V_{OH} and the source voltage (V_{SS}, or ground) when outputting the low level, V_{OL}. Also, the output load of a series of inverters is driven by the current of only the last stage; the preceding stages serve only to efficiently switch the last stage. With device parameters of V_{Tn} = 8V, V_{Tp} = -8V, $\mu_n = \mu_p$ = 20 cm^2/V-sec, descriptive of devices fabricated in our lab, the aspect ratio required to drive a 2kΩ, 100pF load, similar to the scan line, within 1μsec is W/L = 800/8.

If the driver were done in a single stage, it would be inverting; hence at least two stages, or any even number of stages, are needed for a positive line driver. A comparison of a 2-stage and a 4-stage buffer, with the output devices sized to 800/8 was performed. The input stage of the 2-stage driver was 40/8, similar to the typical logic devices used in the logic circuits. The device parameters were those mentioned above. The rise and fall times were 1.3 μsec and 1.1 μsec *resp.* In the 4-stage driver, the lengths were all 8 μm, and the widths scaled up by factors of two. Beginning with (roughly) twice the typical logic gate width, the widths of each device in each stage of the driver were scaled up to the 800μm driver: 100, 200, 400, 800 μm. The rise and fall times were 0.8 μsec. However, there is an optimal number of inverters for a multi-stage buffer. A six stage inverter with a drive stage of 800/8, and input stage of 100/8 would have widths of: 100, 150, 230, 350, 530, 800 μm. The rise and fall times were 0.9 μsec; the increasing number of gate delays is counteracting the effect of reducing the capacitive loading of each of the stages. Thus, a 4-stage CMOS inverter design was chosen.

The effects of series resistance is shown in Figure 6-10, which compares the rising output of a 4-stage CMOS shift register with and without silicided sources and drains. The sheet resistance of the silicided sources and drains is about 20 Ω/□, with the aspect ratio of the area between the contact and the channel about 0.5 □. The sheet resistance

of non-silicided source and drain regions was about 1k Ω/□, with again an area of about 0.5□. Hence, the total series resitance is 1000Ω. The series resistance can be added to the Aim-Spice Model 12 Polysilicon TFTs by putting in the .MODEL card for the TFT the resistance, since the area for the source and drain regions is assumed to be 1. Hence, for a non-silicided device, the .MODEL card for the TFT would be:

.model NGREGTFR NMOS Level=12 VTO=8 U0=20 RSH=500

This transistor, an n-type MOSFET of level 12, would be an n-TFT. The threshold voltage is 8V, and mobility of 20 cm^2/V-sec. Setting the sheet resistance RSH to 500 provides the total series resistance to be 1000Ω, because the assumed source and drain areas are 1 □. If the series resistance were not accurately known, the effective mobility as measured from devices can be used for U0.

Figure 6-10 compares the rise time of C-TFT 4-stage line driver with and without silicides. Two non-silicided drivers were simulated: one which uses refractory metal or deposited silicide scan lines, the other using n^+ polysilicon scan lines. The line resistance of the refractory scan lines was also 1kΩ. The polysilicon scan line resistance was 40kΩ. The wiring resistance of the non-silicided circuits was 10kΩ, considering a polysilicon sheet resistance of 500 Ω/□, and an aspect ratio of 20. The resistance of the gate stripes over the TFTs were simulated by placing a series resistance of half the total resistance of the gate stripe, giving the gate stripe transmission line load of $\frac{1}{2}RC_G$ [78]. The rise time of the silicided buffer was 0.8 μsec; the rise time of the non-silicided buffer with refractory scan line was 1.2μsec. The non-silicided driver rise time was over 10μsec.

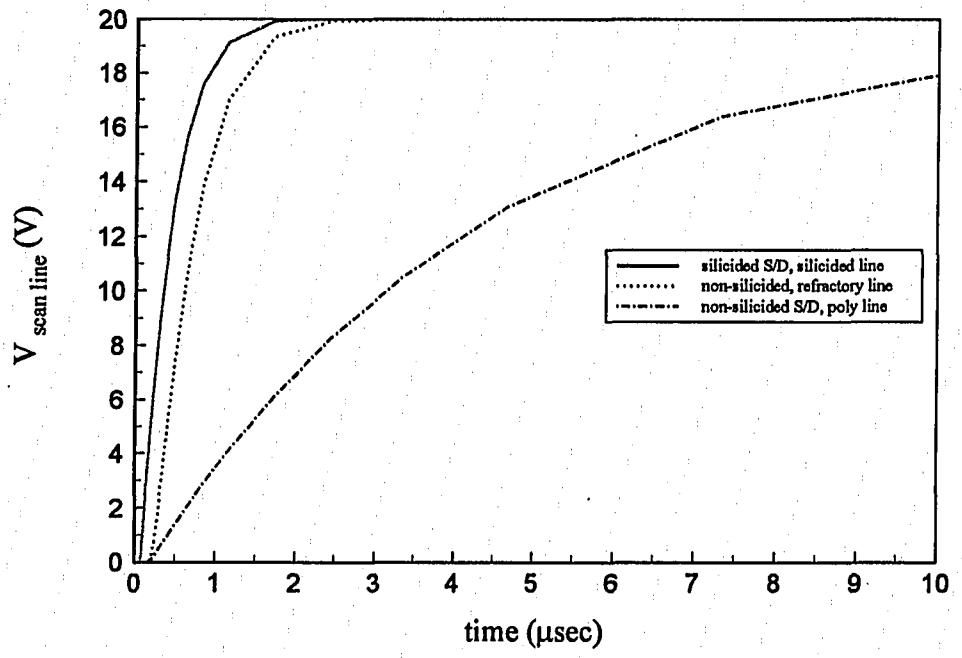


Figure 6-10. Rise Characteristics of Four-Stage CMOS Buffer with and without Silicided Source and Drain Regions

6.2.3.2 nMOS Design

As described above, the nMOS inverter suffers from a continuous pull-up. The rise time is long because the pull-up device must be small in order to be able to output $V_{OL} < V_{Tn}$, so that a valid 0 can be sent to the following stage.

A solution to the nMOS buffer problem is the nMOS superbuffer, which is a two-stage inverter, drawn in Figure 6-11. The first stage generates the inverse of the input signal as in the regular nMOS inverter. But, in the output stage, the pull-up is driven by the inverse of the input signal, *not* V_{GG}. This permits the pull-up to be sized larger, so

that the rise time can be reduced. Since the gate signal to this device will fall to GND when the input is high, should be low, the device will be off and provide no parasitic pull-up, forcing V_{OL}= GND.

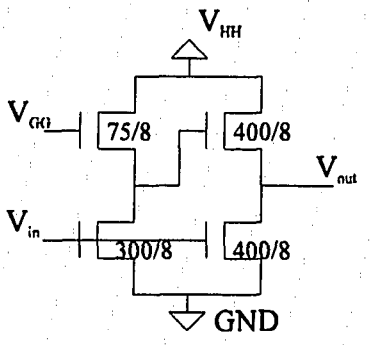


Figure 6-11. nMOS Superbuffer

Because the nMOS level-shifter resembles a 2-stage non-superbuffer, the 4-stage line driver was composed of two regular inverter stages followed by two superbuffer stages. The rise time of the silicided 4-stage mixed nMOS buffer is 0.75μsec. The rise time of the non-silicided buffer is 1.6 μsec. The comparison of the rise characteristics of the 4-stage nMOS mixed buffer with and without silicides is shown in Figure 6-12.

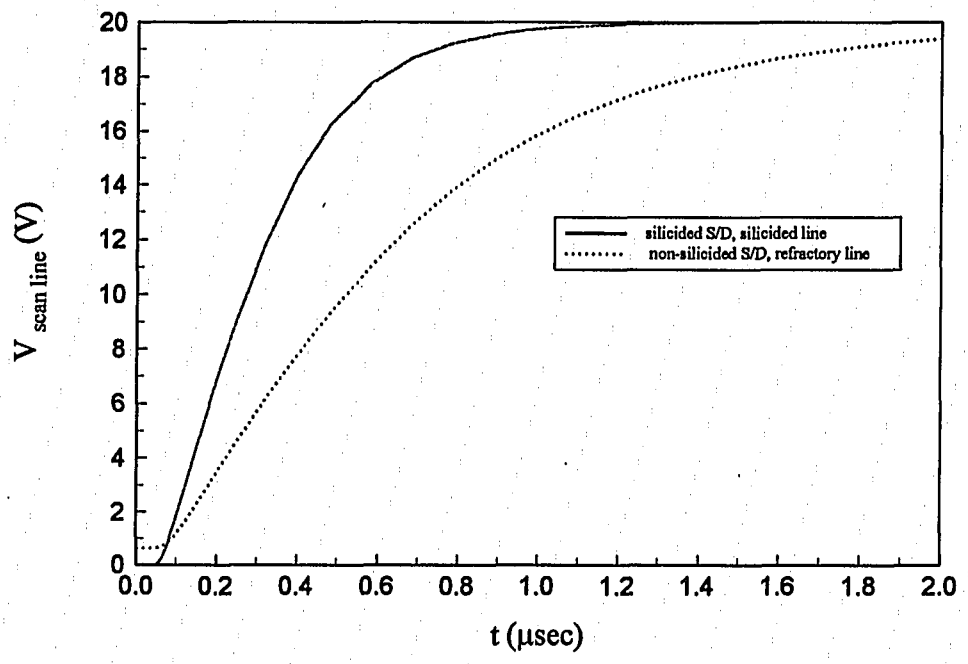


Figure 6-12. Rise Characteristics of Four-Stage Mixed nMOS Buffer with and without Silicided Source and Drain Regions

6.2.4 Scan Line

The scan line was assumed in the mathematical derivations and simulations to be a lump-RC load. However, it is more accurately described as a distributed transmission line. The voltage of the line near the driver will rise or fall more rapidly than farther down the line. (see Figure 6-13.) This is fortunate, since the most time-critical section of the scan line is its pixels which are in the first data block. The first $\frac{640}{blocks}$ pixels down the scan line are the only ones which must have the high voltage immediately in order to write the data. By the second data block period, the scan line would be fully charged.

If the scan driver were unable to meet these charging criteria, then it should execute "precharging," where two scan lines are turned on, as shown in Figure 6-14. The leading scan line is charging up while the lagging scan line has its data written. Note that this will write false data onto the leading line. However, this false data will be on the display for only 1 scan-line time (35 μsec on a 60 Hz display with 480 vertical lines), which is too rapid for the eye to see.

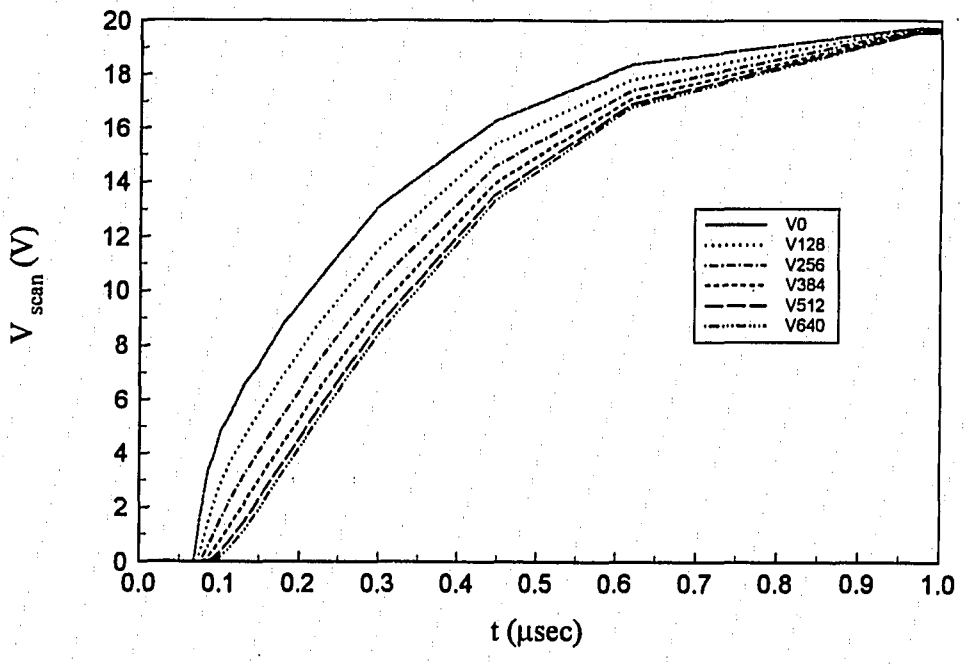


Figure 6-13. Voltage Transient Along the Scan Line

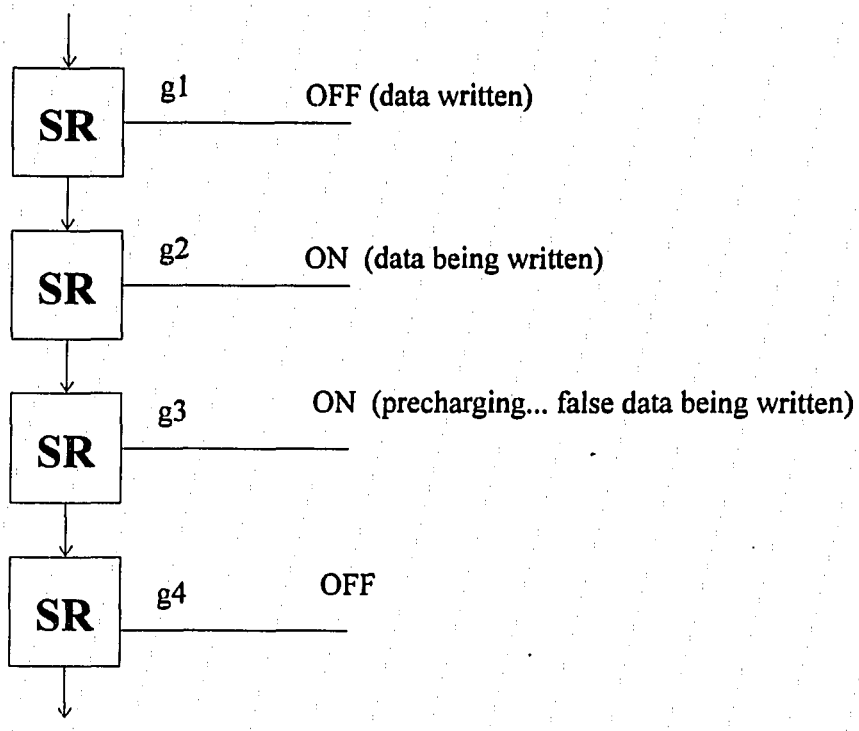


Figure 6-14. Scan-Line Precharging Method

6.3 Data Circuitry

The components of the data drivers are the digital-to-analog converter, amplifiers, and block-switching (data multiplexing) elements. Circuits for each of these are described below.

6.3.1 Digital-to-Analog Converters

The digital-to-analog converters (DACs) receive a binary string which represents a relative fraction of the voltage between the maximum and minimum data voltages, V_{MAX} and V_{min}. Between V_{MAX} and V_{min} are the gray scales. Four different methods of gray scale generation are described for DACs with 16 gray levels.

6.3.1.1 Switch-Capacitor

A basic DAC is the switch capacitor type, which uses relative charge storage to define the relative voltages. A switch-capacitor DAC is shown in Figure 6-15. The network operates between any two voltages, V_{MAX} and V_{min}. The control sequence for this DAC is as follows.

1. Precharge the capacitors by setting PRECHARGE on and OUTPUT off. All capacitors will store charge needed to store $V_{MAX} - V_{min}$.

2. Turn PRECHARGE off.

3. Present the binary inverse of the gray-level word to the discharge switches. This step discharges the unwanted charge. For example, if the input word were <1100> (gray scale 12, near V_{MAX}), the inverted word is <0011>. The charge is dumped from the two low-order capacitors to the power rail V_{min}.

4. Set the input word to <0000> to lock the remaining charge.

5. Set OUTPUT on, which will make the charge accessible to V_{out}^+. Since V_{out}^- is the power rail V_{min}, the accessed charge is the fraction of the charge stored on the capacitors to store V_{MAX}.

Because the charge on the storage capacitors will be shared across the input capacitance of the circuit following the DAC, the base capacitance value, C, should be at least 10 times the input capacitance of the load.

To fabricate this circuit in polysilicon TFT technology, the capacitors cannot be arbitrarily designed. The lower plate should not be island polysilicon for two reasons. If the upper plate were gate material, then the storage poly would be masked during implantation. The undoped poly would be highly resistive, thus difficult to charge and discharge quickly. Secondly, the capacitance would primarily be depletion capacitance, which would decrease the value of the capacitance per area. A larger capacitor area would be required. The solution is to use polycide as the lower plate. Then, the

capacitors are MIM capacitors whose capacitance is solely defined by the dielectric thickness.

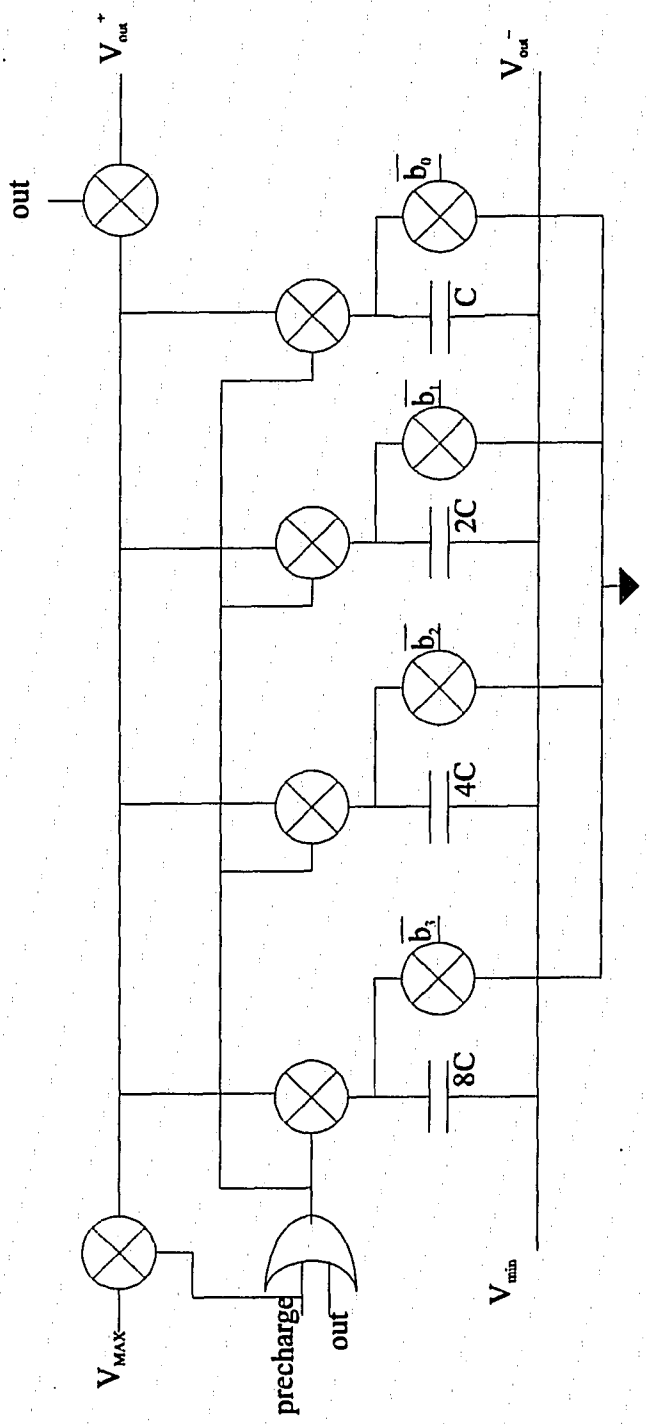


Figure 6-15. Switch-Capacitor DAC

6.3.1.2 Time-Modulated Gray Scaling

By oscillating the output voltage between two values faster than the response of the load, the DC-bias of the output node will settle on the intermediate voltage defined by the relative duration at each driven voltage [82]. The output voltage for a 16 gray scale DAC whose output switches between V_{hi} and V_{lo}, spending n/16 of the period at V_{lo} is:

$$V_{out} = \frac{n}{16}(V_{hi} - V_{lo}) \tag{6.10}$$

A DAC based on a time-modulation was designed by Okada *et. al.* [82]. The originally published version of this circuit contained errors which caused "missing" gray scales and a non-linear gray scale number to output voltage transfer characteristic. To solve the errors, the circuit was prototyped here at Lehigh with off-the-shelf TTL and CMOS ICs. After solving the error (improper decoder-to-NAND plane transcription), the revised circuit for 16-gray levels is shown in Figure 6-16. The gray scale voltage is generated in two planes. In the second plane, the data voltages V_{MAX} and V_{min} are divided across V_{16} (=V_{MAX}) and V_0 (=V_{min}). The voltage must be divided into the number of ranges which is $2^{\#choice\_bits}$. In this example, the *choice_bits* are D_3 and D_4. The output voltage will switch between the divided voltages chosen by the decoder-driven voltage selector.

The relative amount of time the output is selected to the lower-chosen voltage is determined by the first plane. Using the lower data word bits (D_0 and D_1), the multiplexer chooses among a 100%, 75%, 50%, and 25% low duty-cycle wave to send to the voltage switches in the second plane.

Note that the output is a single-pole. The reference node for this voltage is V_0. The voltage selection inputs (V_{16}, V_{12}, V_8, V_4, V_0) are generated either by setting V_{MAX} to V_{16}, and V_{min} to V_0, and placing resistors between to appropriately generate V_{12},

V_8, and V_4. Due to the non-linear nature of some liquid crystal transmission characteristics, the resistor values may not be equal. Alternatively, all of the inputs can be externally provided to optimize the gray scaling performance.

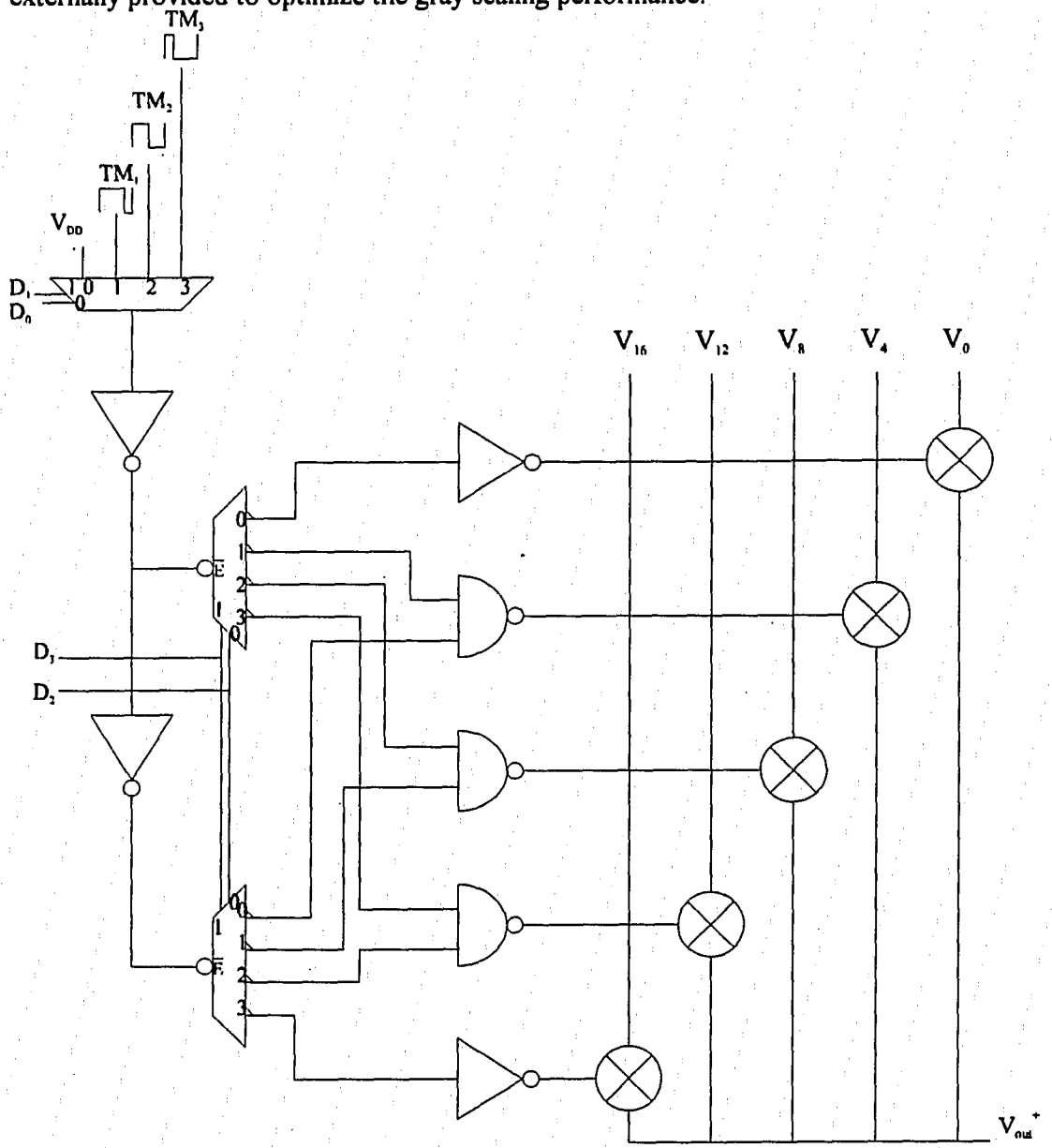


Figure 6-16. Time-Modulated Digital-to-Analog Converter

6.3.1.3 Voltage-Divided Gray Scaling

Because the decoders and multiplexers are composed of many gates, and the voltage selection plane is switched, the Time-Modulated DAC may produce serious switching transients. To eliminate them, gray scales can be statically produced by voltage-division. In the simplest case, V_{MAX} and V_{min} can be mediated by 15 resistors to produce 16 gray levels. However, resistors are undesirable in VLSI technology due to their area, and in thin polysilicon technology due to the non-uniformity of their values. In Figure 6-17, a 16 gray scale Voltage-Division DAC based on a design by Furuhashi *et. al.* [83] is shown. In this scheme, the data voltage range V_{MAX} through V_{min} is partitioned as above, and two adjacent values are chosen by the high-order bits of the data word (D_3 and D_2). This voltage pair is presented to a resistive voltage divider. The portion between these two values is chosen by the low-order bits (D_1 and D_0).

Because of the highly resistive nature of the output phase of this converter, an "overshoot" path is provided. By having OVERSHOOT on, the output node can quickly ramp up to the higher of the chosen voltage pair. Within the data output cycle, the OVERSHOOT signal is turned off, so that the output voltage can settle on the desired gray level. The timing of the OVERSHOOT signal is dependent on the resistances of the analog switches and the second-stage voltage divider, and on the gray level "within" the chosen voltage pair.

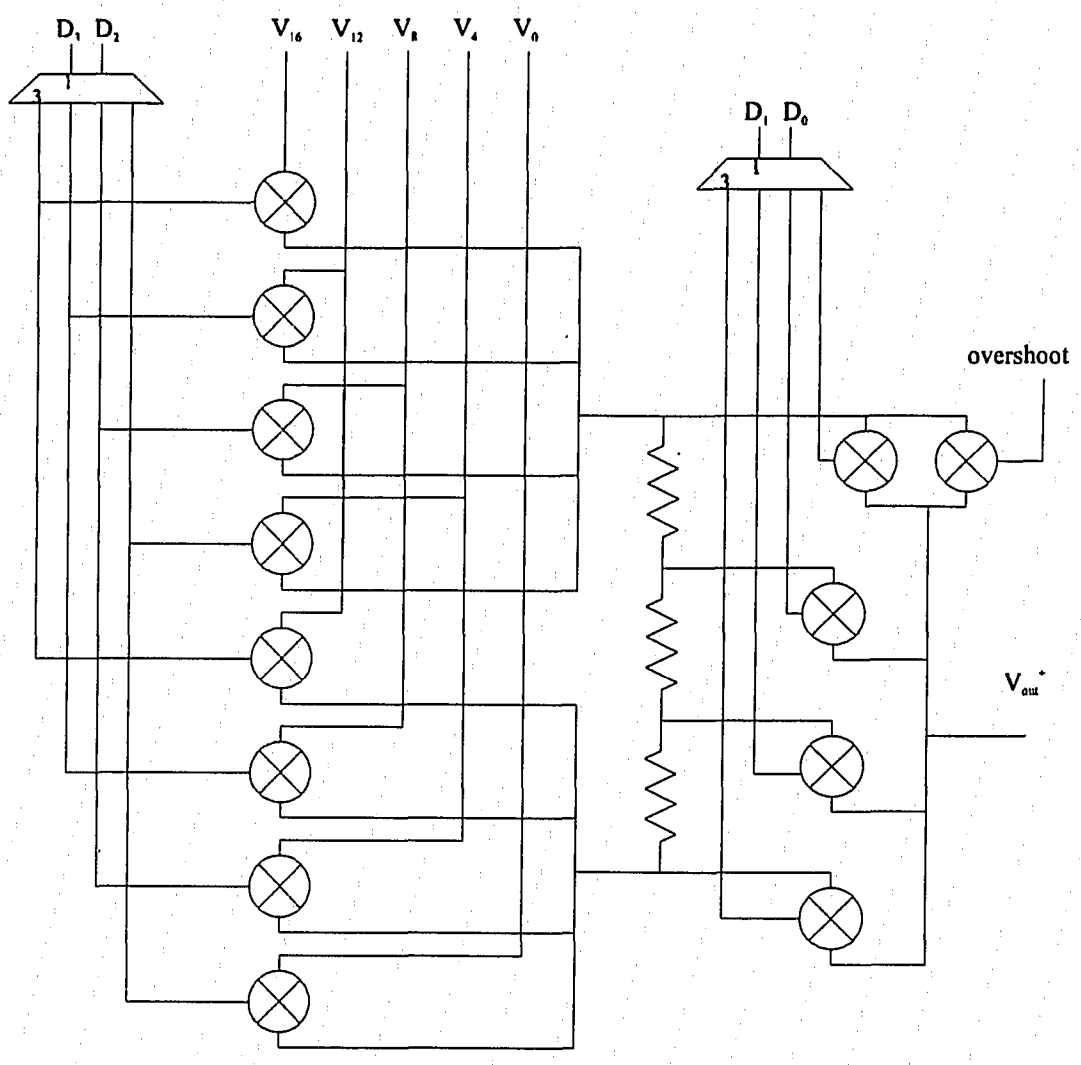


Figure 6-17. Voltage-Division Digital-to-Analog Converter

6.3.1.4 Current-Based DAC

The preceding two DACs require a very large device count. And the switch-capacitor network is highly susceptible to the leakage currents in the pass switches and storage dielectrics. In this dissertation, a new DAC is proposed, which sends discrete levels of current through a resistor to produce a differentiating voltage. This voltage is

amplified using a linear differential amplifier to produce the gray scale voltage levels for the data line. The circuit which produces the differential voltage is shown in Figure 6-18. In this circuit, 16 values of current are permitted to pass through the intermediary resistor which produces a differential voltage. The power rails can be designed to offset variations in threshold voltage and mobility when generating the output voltage difference.

The linearity of the output voltage requires that V_{DS} and V_{GS} of the conducting devices be unaffected by the current level; if the current is too large, the differentiating resistor may provide a large IR voltage drop, which would cause a reduction of V_{GS} and V_{DS} of the pMOS and nMOS devices. Since the current level is dependent on the input word, the reduction in V_{GS} and V_{DS} would be dependent on the input word. The IR drop would be larger for the high graycales (*e.g.* <1111>) where the current levels are higher. Because of the IR loss which reduces V_{GS} and V_{DS}, less current than required would flow through the resistor, thus reducing the differential voltage, and hence the output voltage.

To ensure linearity, the resistor should be small. Also, the pTFTs require that the gate voltage be the inverse of their respective bits in the input data word; this ensures V_{GSp} is unaffected by the voltage drop across the resistor and the nTFTs.

Simpler pull-up and pull-down networks of saturated and linear nTFT and pTFT loads were unable to produce a linear output response for the reasons stated above of the current level dependence of V_{GS} and V_{DS}. Only with nMOS pull-down, and pMOS pull-up (using inverted grayscale word to the pMOS gates) can the voltages at the terminals of the resistor be decoupled from the V_{GS} of the transistors. Still, the differential IR-drop must be kept reasonably small to avoid excessive V_{DS} reduction.

For the circuit shown in Figure 6-18, the total effective width of the nMOS and pMOS transistors is 20μm × *grayscale#*. Thus, for grayscale 3= <0011>, the total width

is 60μm, since transistors C and D will conduct. For grayscale 13=<1101>, transistors A,B, and D will conduct, giving the total eeffective width of 260μm. Note that the pMOS and nMOS transistors of a given bit (A,B,C,D) are either conducting or non-conducting together.

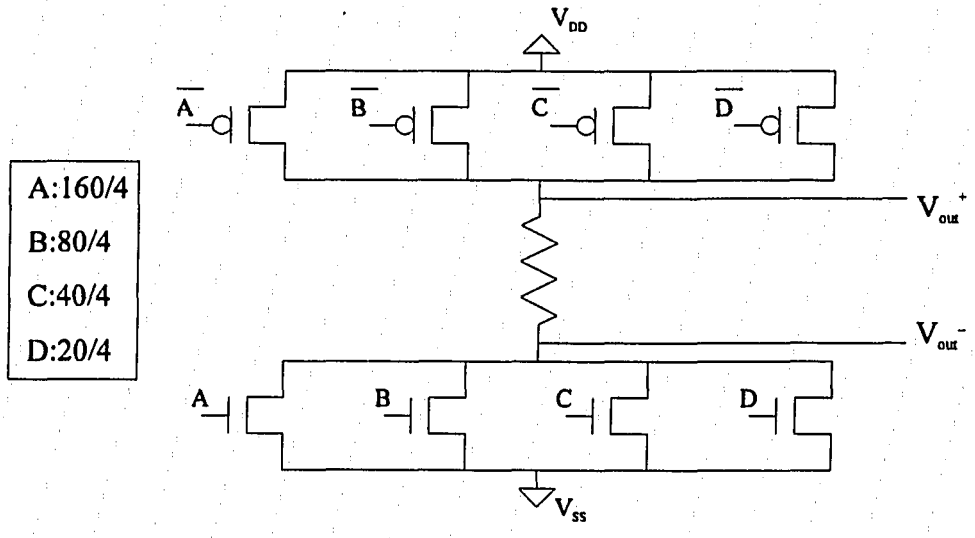


Figure 6-18. Current-Based Digital-to-Analog Converter

Because the output voltage difference must be small, it needs to be amplified. A differential amplifier is shown in Figure 6-19 [84]. The input stage of the amplifier is the differentiating current mirror of the CMOS level shifters. However, unlike the level shifter, the inputs are not at the power rails, so that the output is not necessarily switched to the rails. Threshold voltage and mobility variations can be accommodated by changing V_{GG}, which affects the gain. The rails of the amplifier are set by V_{HH} and V_{LL} of this circuit. They are related to the linear response of the output of the amplifier, and the voltages required to modulate the liquid crystal from the light to dark states.

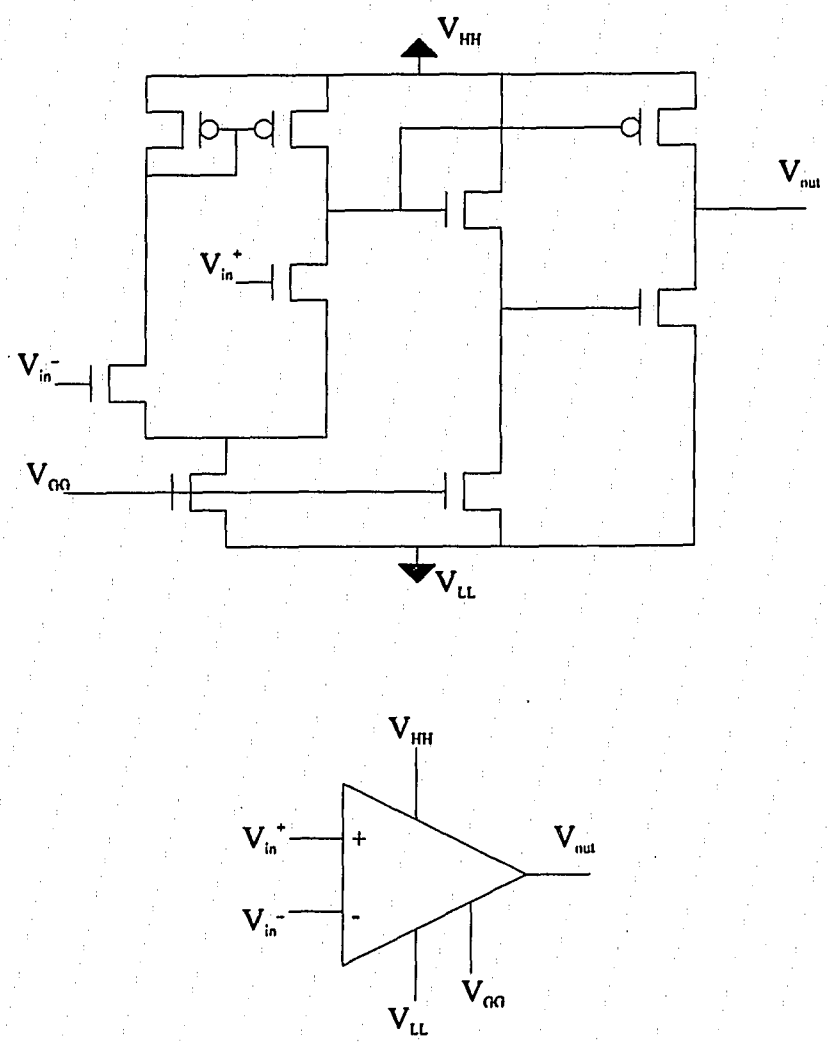


Figure 6-19. Differential Amplifier [Gregorian, 84]

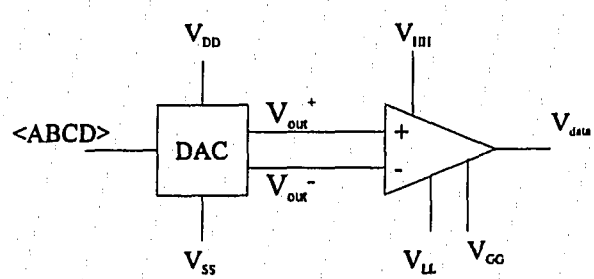


Figure 6-20. Positive-Data Current-Based Digital-to-Analog Converter

The new current based data driver is the combination of the current-based voltage generator and the amplifier. To generate the positive-data gray scales, the components can be connected as shown in Figure 6-20. With square-wave inputs to sequence through the 16 gray levels, the voltage differences produced by the circuit of Figure 6-18 were input to the differential amplifier. The response is shown in Figure 6-21. The down-bounces are due to the zeroing of the input pulses used to generate the gray levels <ABCD> = <1111> through <0000>.

To generate the positive and negative-data gray scales, the circuit can be expanded as shown in Figure 6-22. The current-based voltage difference is input to two amplifiers. Each amplifier is to generate one of the data phases (positive or negative). An analog switch chooses which amplifier to send to the data lines by multiplexing based on the control signal POLARITY. In this circuit, when POLARITY = 0, the positive gray-scale data range is passed; the negative gray-scale range is passed when POLARITY = 1.

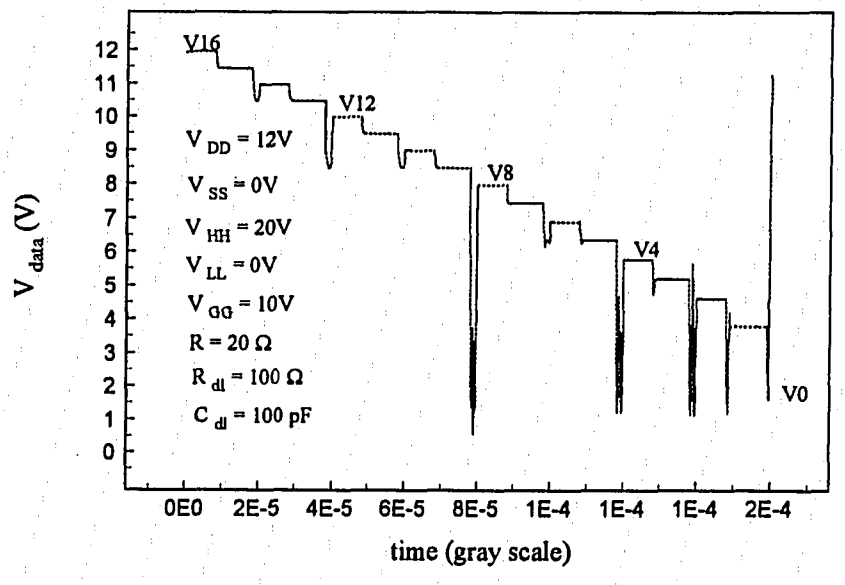


Figure 6-21. Response of Current-Based Digital-to-Analog Converter

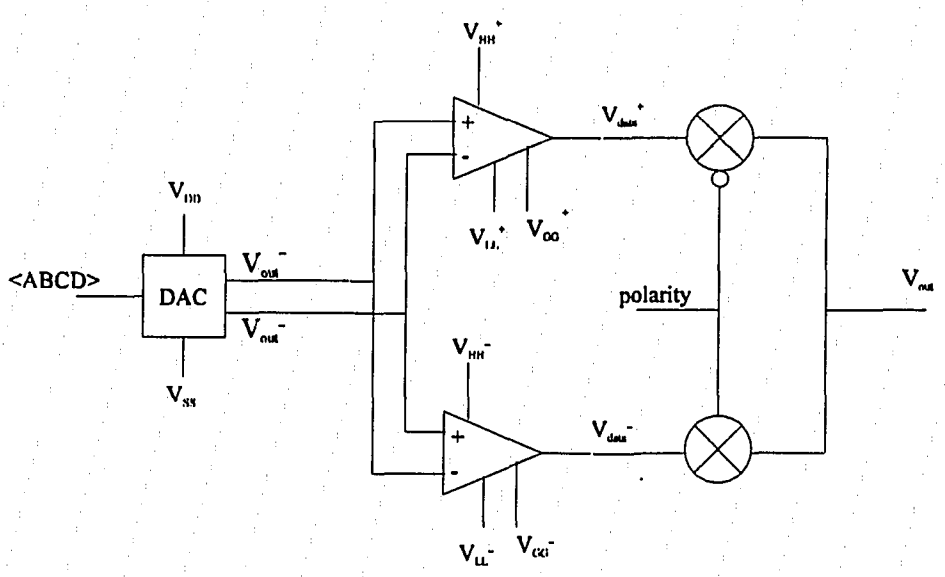
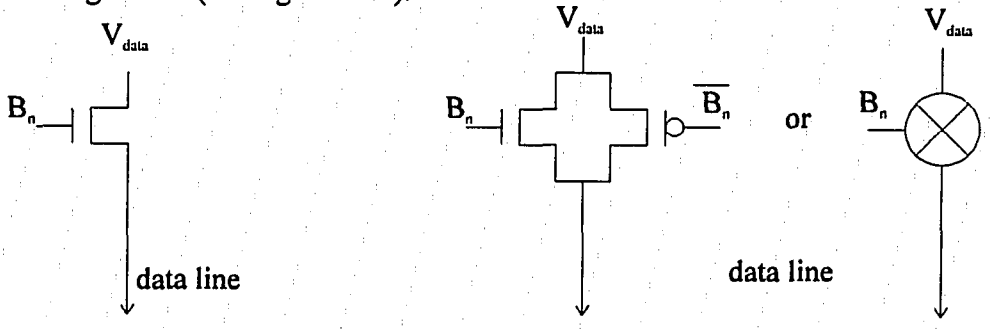


Figure 6-22. Current-Based Data Driver for Positive and Negative Gray Scales

6.3.2 Block Switching/ Data Multiplexing

The data voltages are applied or isolated from the data lines by the block-switching transistors. These devices must be wide enough such that in the on state, the data line can be charged within the time determined by equation 6.7. In the case of the display described, the time is 361 nsec. Because the data is frame-inverted, the maximum data voltage swing can be at least 10V, or twice the black-to-white voltage swing of the liquid crystal. Two cases of block-switches will be compared: the nMOS pass transistor and the CMOS analog switch (see Figure 6-23).



(a) nMOS Pass Transistor (b) CMOS Analog Switch

Figure 6-23. Block-Switches for Data Lines

6.3.2.1 nMOS Pass Transistor

The nMOS pass transistor is the simplest block-switch. To ensure proper passage of the data voltage, the block control signal which is applied to the gate must be at least V_{Tn} above the highest data voltage. Aim-Spice simulations were run for a 20V data swing. To achieve 18V (90%) within 361 nsec, the nTFT geometry needs to be 1600/8 for $V_{Tn} = 2V$ and $\mu_n = 20\ cm^2/V\text{-sec}$. The rise characteristic is shown in Figure 6-24.

When the data period ends, and the transistor is turned off, the channel charge will dissipate. Assuming half of the channel charge will go to the source node, and half to the drain, then half of the channel charge will be put onto the data line. The amount of this "feed through" charge is:

$$\Delta Q \equiv \tfrac{1}{2} Q_{channel} = \tfrac{1}{2} C_G (V_G - V_T) \tag{6.11}$$

where

$$C_G = WL \frac{\varepsilon_{ox}}{x_{ox}}. \tag{6.12}$$

The feedthrough voltage drop on the data line, ΔV_{dl}, is expressed as:

$$\Delta V_{dl} = \frac{\Delta Q}{C_{dl}} = \frac{C_G (V_G - V_T)}{2 C_{dl}} \tag{6.13}$$

This feedthrough voltage shift will cause the data line voltage to drop by 0.52V. Since the scan line is on for the pixels this data line had written data into, this voltage loss will be transferred onto the pixels in the data block on that scan line. To avoid this problem, a charge-sink capacitor can be added to the data line. The arrangement of the

capacitor is shown in Figure 6-25. When the block is active, the sink capacitor appears as a capacitance to ground, increasing the capacitance of the data line. When the block is turned off, the gate of the sink capacitor will turn on, and attract the electrons coming from the nTFT pass transistor channel, preventing them from distributing along the data line and affecting the line voltage, and the scanned pixel voltages. The area of the capacitor is assumed to be half of the area of the block switch transistor.

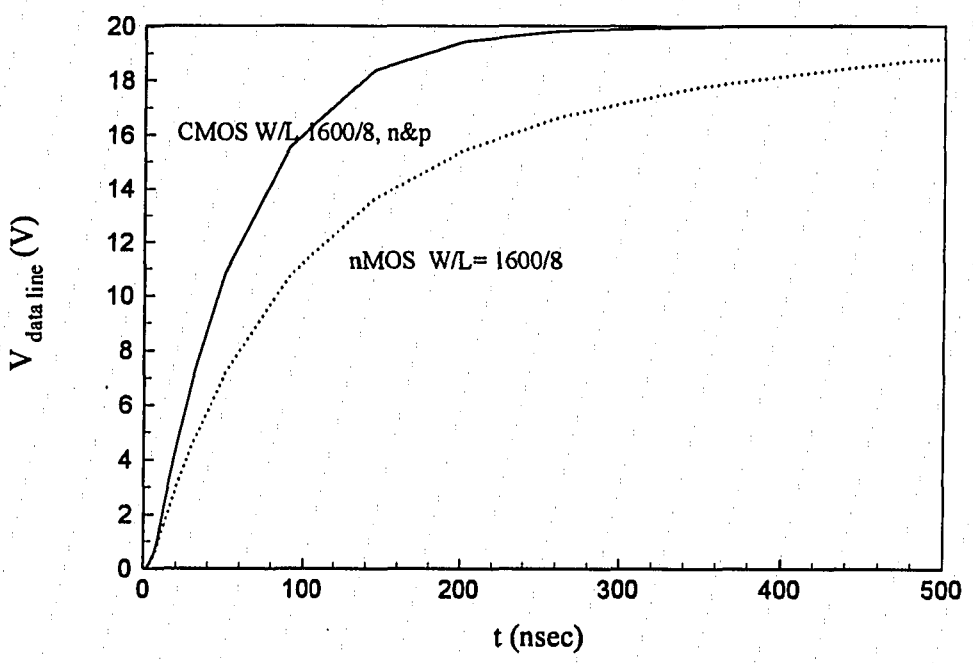


Figure 6-24. Rise Characteristic of Block-Switches

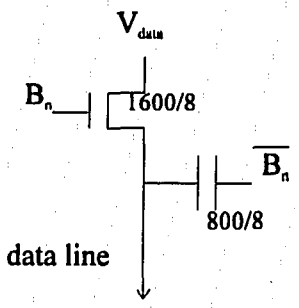


Figure 6-25. Sink Capacitor in nMOS Block Switch

6.3.2.2 CMOS Analog Switch

In the nMOS pass transistor, when the data line voltage rises, V_{GS} will decrease, reducing the current and requiring a longer time to charge the data line. Hence a wider device is needed. If a pMOS device were in parallel, this would not occur. Hence, the CMOS analog switch shown in Figure 6-23 (b) is a better option. In Figure 6-24, the rise characteristic of a CMOS switch is compared to the nMOS switch, where all of the device geometries are 1600/8. Since the CMOS switch has two devices in parallel, this comparison is unfair. The comparison of a CMOS switch where each device has half of the nMOS device width is a fair comparison of the data line driving characteristics, and is shown in Figure 6-26. Again, the CMOS switch is faster because of the continuous drive that the pMOS device provides as the data line voltage rises. The simulated geometry needed for the devices in the CMOS switch to drive the data line is only 500/8.

Besides a reduction in area, the analog switch features two additional benefits: redundancy and feedthrough protection. Because there are two devices in parallel, should one of them fail, the data could still be written. When the block period ends, and the switch turns off, the channel charges will dissipate to the sources and drains. The nTFT will distribute electrons, and the pTFT will distribute holes. The channel charges will recombine instead of propagating down the data line onto the pixels. This obviates

the necessity of increasing the pixel storage capacitance, or adding a charge-sink capacitor to the data line.

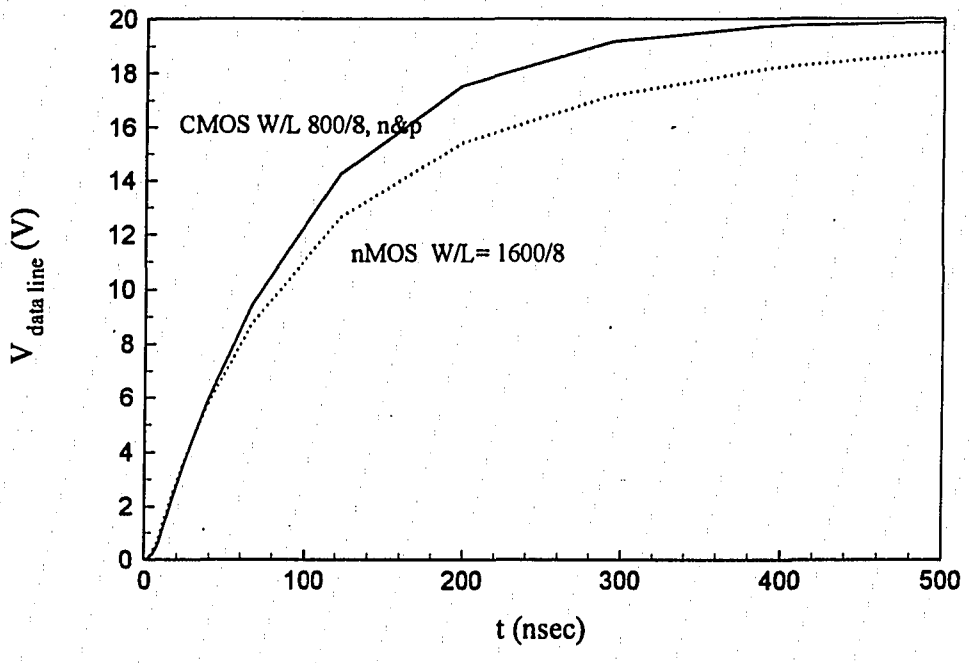


Figure 6-26. Rise Characteristics of Block-Switches with Equal Areas

6.4 Pixels in AMLCDs

The pixels are the fundamental elements of the display area. They are connected to the drivers by the scan and data lines. The components of a pixel are: data line connection, scan line, pixel TFT, storage capacitor, and the ITO flag. The layout and circuit equivalent schematic of a pixel are shown in Figure 6-1. Pixel design issues directly affecting the aperture ratio center around the amount of storage capacitance is required, and the size of the TFT.

6.4.1 Storage Capacitance

A capacitance needs to be added to the pixel node to maintain a nearly constant voltage through the frame period for two reasons: leakage, and channel charge feedthrough. These two components are examined below.

6.4.1.1 Leakage Current Charge Loss

In the off-state, amorphous and polysilicon TFTs conduct current (see Figures 1-1 and 1-2). For stored data voltages on the pixel node-- up to 20V-- the gate-to-source voltage for a non-selected TFT can be as much as V_{GS} = -20V. In order to maintain a given gray level for the entire frame period, there must be enough capacitance on the pixel node such that the charge loss due to the leakage current is less than one gray scale voltage. The capacitance necessary to prevent loss of one gray scale is:

$$I_{leak} = C_{st\ leak} \frac{V_{grayscale}}{t_{frame}} \tag{6.14}$$

$$C_{st\ leak} = \frac{I_{leak} \cdot t_{frame}}{V_{grayscale}} \tag{6.15}$$

6.4.1.2 Feedthrough Voltage Drop

After the data is written to the pixel, the TFT is turned off. Charge from the channel inversion layer leaves through the source and drain terminals. About half of the channel charge leaves through each, hence charge is dumped onto the pixel electrode, changing its potential when the TFT is turned off. Using equation 6.11, the change in the pixel voltage will be:

$$\Delta V_{pixel} = \frac{\Delta Q}{C_{pixel}} = \frac{C_G(V_G - V_T)}{2(C_{LC} + C_{st})} \tag{6.16}$$

and is negative because the charge imposed on the pixel node is from the channel electrons, having a negative charge.

In order to counteract the effects of both the leakage current and the feedthrough voltage drop, the total pixel capacitance needs to be at least the sum of $C_{st\ leak}$, $C_{st\ feedthrough}$, and the capacitance of the pixel flag across the liquid crystal, C_{LC}:

$$C_{st} = C_{st\,leak} + C_{st\,feedthrough} - C_{LC} \tag{6.17}$$

$$C_{st} = \left(\frac{I_{leak} \cdot t_{frame}}{V_{grayscale}} + \frac{C_G (V_G - V_T)}{2\, V_{grayscale}} \right) - C_{LC} \tag{6.18}$$

For a device with parameters as given in Table 6-3, the storage capacitance necessary is 520 fF.

I_{leak}	0.2pA	W	4μm
t_{frame}	$\frac{1}{60}$ sec	L	8μm
$V_{gray\ scale}$	0.25 V	V_G (select)	25 V
x_{ox}	1000Å	V_T	2 V
pitch	48μm	Aperture	50%
cell gap	4μm	C_{LC}	8 fF

Table 6-3. Example Parameters for Storage Capacitance Calculation.

6.4.2 Pixel TFT Size

The size of the pixel TFT can be a significant area in small pitch pixels. The load of the singular pixel is small; the pixel capacitance is less than 1 pF, whereas the data line

and scan line can be over 100 pF each. The aspect ratio of the device need be only large enough to permit sufficient charge transfer from the data line within the time the scan line is on. The minimum W/L for the pixel TFT can be derived using the Howard and Malmberg [85,86] analysis, as follows.

Once the scan and data lines are charged, the RC constant of the pixel should be less than $\frac{1}{3}$ of the charging time for the pixel. The resistance of the device is the sum of the source and drain sheet and contact resistances, and the channel resistance. The capacitance is the sum of the storage and liquid crystal capacitance, or C_{pix}.

$$RC < \tfrac{1}{3} t_{pix} \tag{6.19}$$

$$(R_{ON} + R_{SD})(C_{st} + C_{LC}) < \frac{1}{3} \frac{1}{frate \cdot 480 \cdot \frac{640}{data\,groups}} \tag{6.20}$$

The channel resistance, R_{ON}, is the inverse of the channel conductance when the device is in the linear region. In polysilicon TFTs, the source and drain series resistances are on the order of 1kΩ. Assuming this is much less than the inverse of the conductance, then the minimum aspect ratio of the pixel switching TFT can be determined as:

$$R_{ON} = \frac{1}{G_{ON}} \tag{6.21}$$

$$G_{ON} \equiv \frac{\partial I_D}{\partial V_{DS}} = \frac{W}{L} \mu C_g (V_G - V_T) \tag{6.22}$$

$$\therefore \frac{W}{L} > \frac{3(C_{st} + C_{LC})}{\mu C_g (V_G - V_T)} \frac{frate \cdot 480 \cdot 640}{data\,groups} \tag{6.23}$$

Using the parameters from Table 6-3, and mobility of 20 cm^2/V-sec, and 20 *datagroups* (20 parallel digital to analog converters), the minimum aspect ratio for a pixel TFT would be 0.090. The Howard & Malmberg analysis indicates that any polysilicon TFT should work in a pixel. The unusually low aspect ratio result is due to the high mobility and low series resistance compared to amorphous silicon TFTs, for which the analysis was derived.

6.5 Summary

The operation and control of an active-matrix liquid crystal display panel was discussed. Issues regarding scan and data methodologies were examined. The scan driver is a shift register, with a high voltage and high current output stage at each line. The data driver can be constructed of various complexities. Data can be written to the data lines of the display simulataneously, or in blocks. For block controlled data multiplexing, the data switches must be on-display. The switch control signals can be generated either on the display, or from external circuits. Full data integration suggests that digital-to-analog converters, amplifiers, data-block switches and their controllers be on the active panel of the display.

The mathematics for determining the timing specifications for driver performance were derived. The limiting factors in scan drivers were shown to be the the resistivity of the scan line, which requires that data be written in parallel blocks. Scan drivers discussed were level shifters and buffers, both of nMOS and CMOS circuit families. The CMOS circuits performed better, with saturated output voltages, lower device count, and faster switching times when compared to their nMOS counterparts. Simulations showed a significant improvement in speed of the scan drivers can be achieved by incorporating the silicidation process for TFTs demonstrated in Chapters 3 and 5.

For data drivers, the critical issue depends on the driver architecture. For low-level drivers, which use just mulitplexing block-switches, the issues are the technology and aspect ratio of the switch. For high-level drivers, which incorporate on-display DACs and any necessary amplifiers, the issues are the slew rate of the converter and amplifier, and the area of the driver circuit, which must be replicated over the data bus, which is *blocksize* wide. Data driver circuits of various architecture and technology (nMOS and CMOS) were compared. The CMOS circuits provided superior performance to the nMOS circuits, and required a smaller circuit area. Four digital-to-analog voltage conversion methods were presented, including the development of a new DAC based on current level. The new DAC, based on discrete current levels, has a low device count, and is easily upward expandable to more grayscales. The circuit requires the use of a resistor, which in non-silicided polysilicon technology is highly non-reporoducible. Silicides offer the ability to fabricate uniform, reproducible, small-valued resistors in a polysilicon-based circuit technology.

Pixel design issues were summarized, including charge storage and transistor geometry. The mechanisms of charge leakage from the pixel node were dicussed. By defining the maximum permissible charge loss to that of one gray level over one frame period, an analysis to determine the amount of storage capacitance necessary to limit the voltage loss over a frame period to one grayscale was presented. The leakage current and the feedthrough voltage were determined to be the significant factors affecting the storage capacitance. Depending on the pixel pitch, and the charactersitics of the pixel TFT, one or the other of these factors may dominate.

Due to the relatively high mobilities of polysilicon TFTs, the aspect ratio of the pixel TFT is not a design issue with respect to charging time of the pixel. Instead, the area required to include the TFT is the critical issue, especially in small pitch displays, where lithographic tolerances may dominate the pixel area.

Chapter 7
Summary, Conclusions, and Recommendations

7.1 Theory and Fabrication of Silicides

The principles of silicidation were presented and applied towards the fabrication of silicides on thin films of amorphous and polycrystalline silicon at low temperatures. The effects of the metal species and anneal temperature were considered. The metal species, its chemistry and silicidation, were related to device and display process applications. Electrical characterization methods for silicides were discussed. It was shown mathematically that reduction of external resistance by introduction of a self-aligned silicide will improve the on-current of the device. Accordingly, silicidation will improve TFT performance more dramatically as the external resistance becomes more significant, or comparable to the channel resistance, as in the cases of ultra-thin polysilicon and amorphous silicon TFTs. Circuit performance is also enhanced by silicides when applying polycide wiring and local interconnect technologies. These processes are compatible with AMLCD driver circuitry.

Surface preparation methods were compared for the fabrication of silicides. Isopropanol was shown to desiccate the surface while not destroying the passivation of the silicon surface after cleaning and passivating with HF-dip. The silicidation process developed in this work is applicable to large-area display substrates. The effect of the substrate structure and thickness was shown to affect the sheet resistance of the silicide grown upon it, especially on very thin films of polysilicon or amorphous silicon. In the lowest resistance phase, cobalt silicides were dependent on the silicon structure; polycrystalline silicon substrates produced silicides with a slightly higher sheet resistance. Cobalt silicides on ultra-thin silicon film produced silicides of again slightly higher sheet resistance, suggesting that low-resistance cobalt silicide is dependent on the availability of

silicon. Nickel silicides were independent of silicon structure and thickness above the monosilicide transition.

Cobalt and nickel were shown to produce low resistance silicides at glass-compatible temperatures. Nickel forms silicides on amorphous silicon and silicon-germanium at amorphous-TFT compatible temperatures. Germanium was observed to inhibit the silicidation reaction.

7.2 Amorphous Silicon and Silicon-Germanium Thin Film Transistors

Amorphous silicon and silicon-germanium thin film transistors were formed using ion implantation to delineate the source and drain, making them compatible with CMOS circuit design architectures. Blocking junctions and ohmic contacts were formed by annealing at 260°C. The silicon devices required long anneals; the silicon germanium effused its passivating hydrogen more rapidly then the silicon sample, preventing the silicon-germanium from forming low resistance conduction and contact layers. The devices are severely limited by series resistance. Silicides may improve the characteristics greatly, as the channel resistance is about the same as the extrinsic resistance. Three methods of correcting mobility data were compared. They focused on different issues, from process-related effects to device design. The structure of the device was shown to profoundly affect the device performance, and the extracted values of parasitics-- channel length and extrinsic resistance. The values of the parasitics were strong functions of the extraction method.

7.3 Polysilicon Thin Film Transistors

Polysilicon TFTs with silicided source and drain regions were fabricated for the first time. Cobalt and nickel silicides were studied, and characteristics of devices with cobalt and nickel silicides were compared against one another, and against devices without

silicide. The silicidation process was shown to affect device performance. The heat for silicidation caused more damage to the device than the plasma exposure. Nickel silicided devices, annealed at lower temperatures, did not require the hydrogen anneals as did the higher temperature, cobalt silicided devices. The improvement in device characteristics is a function of the thickness of the silicide film, indicating the dependence on extrinsic series resistance. Thicker silicides were shown to give more improvement to on-current. The devices in this study were formed using diffusion for source and drain regions. For a low-temperature process, ion implantation must be used. Since the activation anneal will not laterally diffuse the dopant under the gate, care must be taken to prevent silicide-channel shorting. The use of spacer oxides around the gate stripe, similar to those used in LDD-CMOS processing, should be used. In ion-implanted technologies, the source and drain sheet resistance is much higher than the values obtained herein from diffusion; the improvement by silicidation would be much more significant. The process developed in this work will also silicidize the gate line, permitting its use as a wiring layer, and for low resistance scan lines.

Ultra-thin (< 200Å) TFTs with silicides were fabricated for the first time. The on-current of U-TFTs without silicide is limited by series resistance of the source and drain. Silicidation removed this limitation, and the resulting device characteristics are comparable to, or better than, devices fabricated on thick islands with or without silicides. The U-TFTs exhibit a lower subthreshold swing, threshold voltage, and off-current, all attributable to the lower volume of defects under the gate. When considered with the additional advantages of ultra-thin films (faster crystallization and implant activation), the U-TFT may be a technology for fabricating lower-cost integrated driver circuits.

7.4 Active Matrix Liquid Crystal Displays

The construction, operation, and design of an active-matrix liquid crystal display was discussed. Integrated driver circuit design issues were presented. Scan and data-driving theories were translated into circuits. Circuits of both nMOS and CMOS architectures were compared by simulation. Simulations showed the increase in speed performance obtainable by silicided TFTs. The CMOS circuits were superior to the nMOS circuits because they had faster response, smaller area, and less standby current. The critical issues for scan and data driver design were determined to be the number of data blocks, the sheet resistance of the scan line, and whether the analog data voltages were realized on the display substrate, or delivered from an external source.

Scan circuit timing and line driving were determined to be based on the number of parallel data inputs, which were a function of the response times of the scan and data lines. Scan circuits for level-shifting and line driving were presented.

The components for data driver circuits were shown. For low-level data driving, data multiplexing by the use of nMOS pass transistors, and CMOS analog switches were compared. Circuits required for higher levels of complexity were presented, including amplifiers and digital-to-analog converters. Four methods of digital-to-analog conversion were compared. The switch-capacitor is large, and sensitive to the leakage of the capacitor dielectric leakage currents. Two MSI-level converters, based on oscillation and voltage division, required a very large device count, and circuit area. A new DAC, based on discrete levels of current, was developed, and shown here for the first time. The circuit uses a small-valued resistor, which without silicides would be impractical and unreliable in polysilicon technology. The DAC is easily expandable to longer data words (*i.e.* finer gray scaling) than the other converter circuits described.

For optimal display performance, thin polysilicon TFTs should be used, so that the pixel leakage is minimized. This decreased the required storage, thus decreasing the

capacitive loading on the scan and data drivers. The thin TFTs can be used in integrated drive circuitry only by the incorporation of silicides to eliminate their series resistance. Also, the thinner islands would provide devices with lower threshold voltages, and lower subthreshold swings, so that the power supply can be less, which would increase battery life for a portable display.

7.5 Recommendations for Future Study

Additional study on the stability of ultra-thin polysilicon is required to bring their circuit technology to maturity. Device processes, including cleaning, annealing, and silicidation need to be examined, and their effects on ultra-thin films understood. The causes for the "dissolution" of the thin silicon should be determined in order to solve the problems associated with their processing, and increase device and circuit yield. More analysis of the operation of the ultra-thin film transistor needs to be performed to optimize its performance. Both p-U-TFT and n-U-TFT device characterization must be performed, and a complementary-U-TFT fabrication process developed to use its demonstrated advantages in driver circuits.

The possibility of employing silicides in amorphous silicon TFT technology has been raised. While the channel mobilities of the devices are lower than the polysilicon, it has been shown that when the extrinsic resistance of the device is large, silicided source and drain improves device performance. It has also been shown that the amorphous devices have significant extrinsic resistance. Thus, silicided amorphous TFTs may improve the perfomance of amorphous silicon driver circuits.

The scan and data driver circuits which have been designed and simulated around the silicided polysilicon TFTs should be fabricated and compared to simulation. Only through this repetitive, closed-loop effort can an optimized display be produced.

References

1. T. Manuel. "Inside Electronics: The Picture Brightens in Flat-Panel Display Technology." *Electronics*, May 28, 1987. pg. 55.

2. "NEC Launches LCD Monitors for Desktop." *Electronic Egr. Times*, January 8, 1996. pg. 1.

3. E. Ratliff. "Survey of Display Technologies for Military Aircraft Cockpit Applications." *SPIE* **vol 1664:** High Resolution Displays and Projection Systems, pg. 66, (1992).

4. S.N. Lee, R.G. Stewart, A.H. Firester. "Integrated Driver Circuitry for Active Matrix Liquid Crystal Displays." *SPIE* **1664**: High Resolution Displays and Projection Systems, pg. 24, (1992).

5. Ji-Ho Kung, Ph.D. Thesis, Lehigh University, 1994.

6. Y. Takafuji, T. Yamashita, T. Shimada, Y. Akebi, T. Matsumoto, K. Tsubota, K. Fujioka, K. Awane. "A 1.9-in. 1.5 M-Pixel Driver Fully-Integrated Poly-Si TFT-LCD for HDTV Projection." *SID Digest of Technical Papaers, 1993*. pg. 383.

7. H. Lebrun, F. Maurice, J. Magarino, N. Szydlo. "AMLCD with Integrated Drivers Made with Amorphous Silicon TFTs." *J. Soc. Info. Display* **3/4**, pg.177 (1995).

8. M. Akiyama, M. Dohjo, T. Higuchi, H. Toeda, K. Suzuki, T. Aoki, Y. Oana. "An Active Matrix LCD with Integrated Driver Circuits Using Amorphous Silicon TFTs." *Japan Display* 1986, pg. 212.

9. A.T. Voutsas, M.K. Hatalis. "Structural Characteristics of as-Deposited and Crystallized Mixed Phase Silicon Films." *J. Elec. Matls.* **23**, 319, (1994).

10. A.T. Voutsas, M.K. Hatalis. "Crystallized Mixed Phase Silicon Films for Thin Film Transistors on Glass Substrates." *Appl. Phys. Lett.* **63**, 1546, (1993).

11. A.G. Lewis, I.-W. Wu, T.Y. Huang, A. Chiang, R.H. Bruce. "Active Matrix Liquid Crystal Display Design Using Low- and High- Temperature Processed Polysilicon TFTs." *IEDM Dig. Tech. Papers 1990*, pg. 843.

12. M. Simile. "Excimer Laser Annealing." *Information Display*, Nov. 11, 1995, pg. 18.

13. J.-H. Kung, M.K. Hatalis, J. Kanicki. "Performance of Polycrystalline Silicon Thin Film Transistors with Double Layer Gate Dielectric." *MRS Symp. Proc.* **284**, 431, (1993).

14. J.-H. Kung, M. K. Hatalis. "Investigations on the Quality of Polysilicon Film-Gate Dielectric Interface in Polysilicon Thin Film Transistors." *Thin Solid Films* **216**, 137, (1992).

15. M.K. Hatalis, J.-H. Kung, J. Kanicki, A.A. Bright. "Effect of Gate Dielectric on Performance of Polysilicon Thin Film Transistors." *MRS Symp. Proc.* **182**, 357, (1990).

16. D.M. Kim, F. Qian, M.J. Esralian, D.E. Whitlow, R.G. Culter, S.C. Thayer. "Characterization and Modeling of Polysilicon TFTs and TFT CMOS Circuits for Displays and Integrated Driver Applications." *SID Digest of Technical Papers, 1990.* pg. 304.

17. S.P. Murarka, Silicides for VLSI Applications. Academic Press. 1993.

18. M. Kobayashi, T. Nakazono, K. Mori, H. Nakamura, H. Sato, M. Nakagawa. "High Mobility Poly-Si TFTs with Tungsten Polycide Gate for 1.9MPixel HDTV LCD Projector." *Soc. for Info. Display Int'l Symposium Digest of Technical Papers, 1994.* pg. 75.

19. H. Jiang, C.M. Osburn, P. Smith, Z.-G. Xiao, D. Griffis, G.M. M^{c} Guire, G.A. Rozgonyi. "Ultra Shallow Junction Formation Using Diffusion from Silicides: I. Silicide Formation, Dopant Implantation and Depth Profiling." *J. Electrochem. Soc.* **139**, 196 (1992).

20. H. Jiang, C.M. Osburn, Z.-G. Xiao, G.M. M^{c} Guire, G.A. Rozgonyi. "Ultra Shallow Junction Formation Using Diffusion from Silicides: II: Diffusion in Silicides and Evaporation." *J. Electrochem. Soc.* **139**, 206 (1992).

21. C.-S. Yoo, T.-H. Lin, N.-S. Tsai, L.J. Ijzendoorn. "Si/W Ratio Changes and Film Peeling During Polycide Annealing." **29**, 2535, (1990).

22. H.J. Geipel, N. Hsieh, M.H. Ishagi, C.W. Koburger, F.R. White. *IEEE Electron Dev.* **27**, 1417 (1980).

23. L. Niewöhner, Th. Jäger. "Self-aligned $CoSi_2$ Formation by Ion Beam Mixing and its Application to MOS Devices." *Proc. 8th Int'l IEEE VLSI Multilevel Interconnection Conf., 1991.* pp 329.

24. W.J. Freitas, J.W. Swart. "Influence of Impurities on Cobalt Silicide Formation." *J. Electrochem. Soc.* **138**, 3067 (1991).

25. S. Wolf, R.N. Tauber. Silicon Processing for the VLSI Era, vol 1: Processing Technology Lattice Press, 1986.

26. M.E. Alperin, T.C. Hollaway, R.A. Haken, C.D. Gosmeyer, R.V. Karnaugh, W. D. Parmantie. "Development of the Self-Aligned Titanium Silicide Process for VLSI Applications." *IEEE J. Sol. St. Circuits* **20**, 61 (1985).

27. I.C. Chen, M. Rodder, H.J. Wann, D. Spratt. "Performance and Reliability Enhancement for CVD Tungsten Polycided CMOS Transistors Due to Fluorine Incorporation in the Gate Oxide." *Electron Dev. Lett.* **15**, 351, (1994).

28. A. Gruhle, H. Beneking, J. Heinz, H. v.Känel. "Application of MBE-Grown Epitaxial Si/$CoSi_2$/Si Heterostructures from Overgrown Si Permeable Base Transistors." *IEEE. Electron. Dev.* **38**, 1878 (1991).

29. C.M. Osburn. "Metal Silicide Technology for ULSI Devices." *MCNC Microelectronics Technical Bulletin, NCSU.* **vol 2** #6. pg. 1 (1990)

30. G.A. Rozgonyi, J.W. Honeycutt. "Silicidation Enhanced Diffusion of Buried Dopant Layers." ibid, pg. 17.

31. F. Lin, G. Sarcona, M.K. Hatalis, A.F. Cserhati, E. Austin, D.W. Greve. "Characterization of Cobalt Annealed on Silicon Germanium Epilayers." *J. Thin Solid Films* **250**, 20 (1994).

32. G. Sarcona, F. Lin, M.K. Hatalis, A.F. Cserhati, E. Austin, D.W. Greve. "Electrical and Structural Properties of Cobalt Annealed on Silicon Germanium Epilayers." MRS Proceedings **281** 647 (1993), ed. C. Tu.

33. D.K. Schroder. Semiconductor Material and Device Characterization. J. Wiley Interscience. 1990.

34. Scott Vincelette, MS. Thesis. Lehigh University, 1989.

35. B.L. Crowder S. Zirinsky. "1μm MOSFET VLSI Technology. Part VII: Metal Silicide Interconnection Technology." *IEEE Electron. Dev.* **26**, 369 (1979).

36. T. Mochizuki, K. Shibata, T. Inoue, K. Ohuchi. "A New MOS Process Using $MoSi_2$ as a Gate Material." *Jap. J. Appl. Physics* **17**, supplement 17-1, 37 (1978).

37. S. Zirinski, B.L. Crowder, "Refractory Silicides for High-Temperature Compatible IC Conductor Lines." *J. Electrochem. Soc.* **124**, 388, (1977).

38. B.L. Crowder, S. Zirinski, L. Ephrath. "The Use of Tungsten Silicide (WSi_2)/Polycrystalline Silicon as a Gate Material for MOS Devices." *J. Electrochem. Soc.* **124**, 464, (1977).

39. Q. Wang, C.M. Osburn, C.A. Canovai. "Ultra-Shallow Junction Formation Using Silicide as a Diffusion Source and Low Thermal Budget." *IEEE Electron Dev.* **39**, 2486 (1992).

40. H. Hayashida, Y. Toyoshima, H. Shinagawa, Y. Suizu, I. Kunishima, K. Suguro, K. Hashimoto. "Manufacturable Local- Interconnect Technology Fully Compatible with Titanium Silicide Process." *Proc. 8th Int'l IEEE VLSI Multilevel Interconnection Conf., 1991.* pp 332.

41. T.E. Tang, C.-C. Wei, R.A. Haken, T.C. Holloway, L.R. Hite, T.G.W. Blake. "Titanium Nitride Local- Interconnect Technology for VLSI." *IEEE Electron Dev.* **34**, 682 (1987).

42. D.J. Miller, T.I. Selinder, K.E. Gray. "The Role of Transient Phase Formation During the Growth of Epitaxial $CoSi_2$ by Annealing of Co/Ti Bilayers on (100) Silicon." *Materials Res. Soc. Symposium Proc.* **402**, (1996).

43. G.T. Sarcona, M.K. Hatalis. "Low Temperature Silicides for Poly-Silicon Thin Film Transistor Applications." ibid.

43. S.W. Russell, E.J. Jaquez, T.L. Alford. "Stability of Co/Ti Bilayers on SiO_2." ibid.

44. J. Cardenas, S.-L. Zhang, B.G. Svensson, S. Peterson. "On the Formation of Inhomogeneities in Epitaxial $CoSi_2$ Layers Grown from the Interaction of Co/Ti Bilayers with Si <100> Substrates." ibid.

46. J.S. Byun, J.M. Sun.J.W. Park, J.J. Kim. "Defect Generation During Epitaxial Growth of $CoSi_2$ on Miniature Sized (100)Si Substrate and its Effect on Electrical Properties." ibid.

47. T. Morimoto, T. Ohguro, H.S. Momose, T. Iinuma, I. Kunishima, K. Suguro, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, Y. Katsumata, H. Iwai, "Self-Aligned Nickel-Mono-Silicide Technology for High-Speed Deep Submicrometer Logic CMOS ULSI," *IEEE Trans. Electron Dev.* **42**, 915, (1995).

48. K. Maex. *MRS Fall 1995 Tutorial Session H: Silicide Technology.*

49. Microelectronics Center Technical Bulletin, Nov/Dec 1990. **vol 2** #6. North Carolina State University.

50. B.-S. Chen, M.-C. Chen. "Formation of Cobalt Silicided Shallow Junctions Using Implant Into/Through Silicide Technology and Furnace Annealing." *IEEE. Trans. Electron Dev.* **43**, 258, (1996).

51. H.C. Cheng, M.H. Juang, C.T. Lin, L.M. Huang. "A Silicidation Induced Process Consideration for Forming Scaled-Down Silicided Junctions." *Electron Dev. Lett.* **15**, 342, (1994).

52. D. Levy, P. Delpech, M. Paoli, C. Masurel, M. Vernet, N. Brun, J.-P. Jeane, J.-P. Gonchord, M.A. Hanifi, M. Haond, T. d'Ouville, H. Mignam. "Optimization of a Self-aligned Titanium Silicide Process for Submicron Technology." *IEEE Trans. Semicond. Mfg.* **3** 168 (1990).

53. H. Ronkainen, G. Drozdy, S. Franssila. "Use of Disposable Double-Spacer and Self-Aligned Cobalt Silicide for LDD MOSFET Fabrication." *IEEE Electron Dev. Lett.* **12**, 125 (1991).

54. T. J. King, K. C. Saraswat, *Elec. Dev. Lett.* **12**, 584, (1991).

55. H. Mishima, T. Yasui, T. Mizuniwa, M. Abe, T. Ohmi, "Particle-Free Wafer Cleaning and Drying Technology." *IEEE. Trans. Semiconductor Manufacturing.* **2**, 69, (1989).

56. H. Mishima, T. Ohmi, T. Mizuniwa, M. Abe, "Deposition Characteristics of Isopropanol (IPA) and Moisture from IPA Vapor Dried Silicon Wafers." *IEEE. Trans. Semiconductor Manufacturing.* **2**, 121, (1989).

57. Sze, S.M. Physics of Semiconductor Devices. J. Wiley & Sons, 1981.

58. Ghandi, S.K. VLSI Fabrication Principles. Silicon and Gallium Arsenide. J. Wiley & Sons, 1983.

59. W. H. Dumbaugh, P. L. Bocko, *Society for Information Display Digest of Technical Papers 1990,* **21**, 70, (1990).

60. R.G. Stewart, J. Dresner, S. Weisbrod, R.I. Huq, D. Plus, B. Mourey, B. Hepp, A. Dupont, *Society for Information Display Digest of Technical Papers 1995*, 89, (1995).

61. M. Stutzmann, R. A. Street, C. C. Tsai, J. B. Boyce, S. E. Ready, *J. Appl. Phys.* **66**, 569, (1989).

62. R. L. Weisfield, H. C. Tuan, L. Fennell, M. J. Thompson, *Materials Res. Soc. Symp. Proc.* **95**, 469, (1987).

63. K. Suzuki, M. Ikeda, M. Kikuchi, "Amorphous Silicon TFT", JARECT **6**, *Amorphous Semiconductor Technologies and Devices 1983*, Y. Hamakawa, Ed. publ. North-Holland Publishing Co. 1983.

64. R. E. I. Schropp, "Improved Material Properties of Amorphous Silicon from Silane by Fluorine Implantation: Application to Thin-Film Transistors." *J. Appl. Phys.* **65**, 3706, (1989).

65. G. Sarcona, M.K. Hatalis, A. Catalano, "Amorphous Silicon and Silicon-Germanium Thin Film Transistors Formed by Ion Implantation." *Materials Res. Soc. Symp. Proc. 1993*, **297**, 907, (1993).

66. G. N. Parsons, "Enhanced Mobility Top-Gate Amorphous Silicon Thin-Film Transistor with Selectively Deposited Source/Drain Contacts." *Elec. Dev. Lett.* **13**, 80, (1992).

67. J.G.J. Chern, P. Chang, R. Motta, N. Godinho, "A New Method to Determine MOSFET Channel Length," *Electron Dev. Lett.* **1**, 170, (1980).

68. J. Whitfield, "A Modification on 'An Improved Method to Determine MOSFET Channel Length.'" *Electron Dev. Lett.***6**, 109, (1985).

69. Y. Kaneko, T. Toyabe, T. Tsukada, "Analysis of Effective Channel Length in Amorphous Silicon Thin-Film Transistors." *Japanese J. Appl. Phys.* **31**, 3506, (1992).

70. P. Yan, N. N. Lichtin, D. L. Morel, "Amorphous Silicon, Germanium, and Silicon-Germanium Alloy Thin-Film Transistor Performance and Evaluation." *Appl. Phys. Lett.*, **50**, 1367, (1987).

71. N. Yamamuchi, J.-J.J. Hajjar, R. Reif. "Polysilicon Thin Film Transistors with Channel Length and Width Comparable to or Smaller than the Grain Size of the Film." *IEEE Trans. Electron Dev.* **38**, 55, (1991).

72. M. Bonnel, N. Duhamel, T. Henrion, B. Loisel. "Furnace and Rapid Thermal Annealing for Polysilicon Thin Film Transistors." *J. Electrochem. Soc.* **140**, 3548, (1993).

73. H.N. Chern, C.L. Lee, T.F. Lei. "Correlation of Polysilicon Thin-Film Transistor Characteristics to Defect States via Thermal Annealing." *IEEE Trans. Electron Dev.* **41**, 460, (1994).

74. M. Sasaki, T. Kimura. "The Impact of Oxidation of Channel Polysilicon on the Trap Density of Submicron Bottom-Gate TFT's." *Electron Dev. Letts.* **15**, 1, (1994).

75. Y.-M. Ha, J.-I. Han, C.-H Han, C.-K. Kim. "Hydrogenation Mechanism of Top-Gated Polysilicon Thin Film Transistors." *Materials Res. Soc. Symp. Proc.* **345**, 135, (1994).

76. Y. Shimada, T. Yamamoto, M. Goto, H. Morimoto. "Low-Resistivity Tantalum Film for TFT Gate Line." *Soc. for Information Display Digest of Technical Papers 1993,* pg. 467.

77. M. Dohjo, T. Aoki, K. Suzuki, M. Ikeda, T. Higuchi, Y. Oana. "Low Resistance Mo-Ta Gate-Line Material for Large Area Amorphous Silicon TFT LCDs." *Proc. SID.* **29/4**, 283, (1988).

78. B. Conner, S. Velamin, D. Mank. "Low Power 6-bit Column Driver for AMLCDs." *Soc. for Information Display Digest of Technical Papers 1994*, pg 351.

79. R.H. Bruce, S. Morozumi, M. Hack, A. Lewis, I.-W. Wu. "Polysilicon and Amorphous Silicon Technology Comparison for AMLCDs." *SPIE* **vol 1664:** High Resolution Displays and Projection Systems, pg. 14, (1992).

80. W.E. Howard, P.M. Alt, R.L. Wisnieff. "Eliminating Crosstalk in Thin Film Transistor Liquid Crystal Displays." *1988 Internat'l Display Res. Conf.* pg. 230.

81. Fleischer, David, L. Master's Thesis, Lehigh University, 1996.

82. H. Okada, S. Uehira, H. Fukuoka, Y. Kanatani, M. Hijikigawa. "TFT-LCDs Using Newly Designed 6-Bit Digital Data Drivers." *Soc. for Information Display Digest of Technical Papers 1993,* pg. 11.

83. T. Furuhashi, H. Nitta, I. Takita, H. Mano, S. Tsunekawa, M. Iwasaki, M. Arakawa. "A 64-Gray Scale Digital Signal Driver for Color TFT-LCDs." *Soc. for Information Display Digest of Technical Papers 1994,* pg. 359.

84. Gregorian, R., and Temes, G. Analog MOS Integrated Circuits for Signal Processing. Wiley Series on Filters. J. Wiley & Sons, 1986.

85. W.E. Howard. "Active Matrix Techniques for Displays." *Proc. SID.* **27/4**, 313, (1986).

86. P.R. Malmberg. "Active Matrix Addressing Technology." *SID Seminar Lecture Notes #3.2*, 1985.

Appendix

A.1 Silicidation Process

1. 5:1:1 H_2O:H_2O_2:NH_4OH, 5 min.
2. DI water rinse, 5 times.
3. 5:1:1 H_2O:H_2O_2:HCl, 5 min.
4. DI water rinse, 5 times.
5. 25:1 H_2O:HF, 30 sec. after surface is hydrophobic.
6. DI water rinse, 5 times.
7. Immersion in 2-propanol (IPA), 1 min
8. Nitrogen blow-dry.
9. Load into sputter system load-lock with vent N_2 purging.
10. Mechanical pumpdown to 1 torr.
11. Roots pumpdown to 100 mtorr.
12. Cryopump for 5 min. after pressure falls to 1 mtorr.
13. Load into sputter system main chamber.
14. Cryopump until pressure less than 1μtorr, or 5 min, whichever longer.
15. Turn on Ar, 9 mtorr. Typically 50 sccm.
16. Pre-sputter target 5 min.
17. Sputter onto sample. Ni: 60 or 120 sec. Co: 30, 60, or 120 sec.
18. Turn off plasma and Ar.
19. Cryopump until pressure less than 1μtorr.
20. Turn on quartz lamps.
21. When temperature goes above set point, begin 10 min of anneal.

22. Turn off lamps.
23. Cool 5 min.
24. Remove sample.
25. Metal Etch:
    a. Cobalt etch: 3:1 H_2O_2:HCl, 30 sec.
    b. Nickel etch: 3:1 H_2O_2:H_2SO_4, 30 sec.
26. DI water rinse, 5 times.
27. Measure sheet resistance using four-point probe.

A.2 Polysilicon TFT Fabrication Process

1. 5:1:1 H_2O:H_2O_2:NH_4OH, 5 min.
2. DI water rinse, 5 times.
3. 5:1:1 H_2O:H_2O_2:HCl, 5 min.
4. DI water rinse, 5 times.
5. 25:1 H_2O:HF, 30 sec. after surface is hydrophobic.
6. DI water rinse, 5 times.
7. Oxidation: 1100°C, 3h, steam, followed by 1100°C, 1h, dry O_2.
8. Island Silicon Deposition. 580°C, 200 mtorr. 23 min (1100Å) for thick island devices, 13 min (600Å) for thin island devices.
9. Crystallization anneal: 600°C, 3h, N_2.
10. Vapor prime: xylenes + HMDS, 5 min.
11. Island Pattern: spin photoresist, 5000 rpm, 60 sec.
12. Bake 95°C, 30 min.
13. Exposure: 14 sec, 4mW/cm^2. Photomask = Island.

14. Development: 1 min, 1:1 PRD Developer.
15. Bake, 120°C, 30 min.
16. Silicon etch: 1:50:20 $HF:HNO_3:H_2O$, 40-60 sec.
17. DI water rinse, 5 times.
18. Bake, 120°C, 10 min.
19. Strip Photoresist: Stripper, 80°C, 20 min.
20. RCA clean (steps 1 - 6).
21. Gate oxidation. 1000°C, dry O_2. 60 min (720Å) for thin island devices; 90 min (900Å) for thick island devices.
22. Gate silicon deposition: 580°C, 200 mtorr. 23 min (1100Å).
23. Gate Photolithography. (steps 10 - 15, Photomask = Gate).
24. Silicon etch: 1:50:20 $HF:HNO_3:H_2O$, 40-60 sec.
25. Gate oxide etch: 6:1 $NH_4F:HF$ (6-1 BHF), 70 sec.
26. RCA clean (steps 1-6).
27. $POCl_3$ Diffusion: 900°C, 5 min predeposition under $O_2+N_2+POCl_3$ flow; 15 min drive-in in N_2.
28. Oxide Etch: 6-1 BHF, 20 sec.
29. Electrical Measurement: "Initial Device".
30. Silicidation. (see **A.1**).
31. Electrical Measurement: "Cobalt Before PMA", "Nickel After Silicidation."
32. (Cobalt Silicided Devices only) PMA: 400°C, 2 h, H_2/N_2.
33. Electrical Measurement: "Cobalt After PMA".

Vita

Greg Sarcona was born on November 23, 1966 in Smithtown, NY, to Ethel and Thomas Sarcona. He attended Carnegie-Mellon University from 1984 to 1988, receiving the B.S. degree in Computer Engineering. He began graduate studies at Lehigh University in 1988. He was a teaching assistant, graduate student president, columnist for the school newspaper, and research assistant. His research efforts were under the advisement of Prof. Miltiadis K. Hatalis, in the Sherman-Fairchild Center for Solid State Studies and the Display Research Laboratory. His interests are in the design of active matrix liquid crystal display drivers and silicidation technologies. Mr. Sarcona is a member of IEEE and SID.