

1-1-1982

Build-up of inversion charge in MOS tunnel diodes by laser illumination.

Sanjay Jain

Follow this and additional works at: <http://preserve.lehigh.edu/etd>



Part of the [Electrical and Computer Engineering Commons](#)

Recommended Citation

Jain, Sanjay, "Build-up of inversion charge in MOS tunnel diodes by laser illumination." (1982). *Theses and Dissertations*. Paper 2422.

This Thesis is brought to you for free and open access by Lehigh Preserve. It has been accepted for inclusion in Theses and Dissertations by an authorized administrator of Lehigh Preserve. For more information, please contact preserve@lehigh.edu.

BUILD-UP OF INVERSION CHARGE IN MOS
TUNNEL DIODES BY LASER ILLUMINATION

by
Sanjay Jain

A Thesis
Presented to the Graduate Committee
of Lehigh University
in Candidacy for the Degree of
Master of Science
in Electrical and Computer Engineering

Lehigh University

1982

ProQuest Number: EP76698

All rights reserved

INFORMATION TO ALL USERS

The quality of this reproduction is dependent upon the quality of the copy submitted.

In the unlikely event that the author did not send a complete manuscript and there are missing pages, these will be noted. Also, if material had to be removed, a note will indicate the deletion.



ProQuest EP76698

Published by ProQuest LLC (2015). Copyright of the Dissertation is held by the Author.

All rights reserved.

This work is protected against unauthorized copying under Title 17, United States Code
Microform Edition © ProQuest LLC.

ProQuest LLC.
789 East Eisenhower Parkway
P.O. Box 1346
Ann Arbor, MI 48106 - 1346

ACKNOWLEDGEMENTS

I wish to express my gratitude to my teacher, Professor W. E. Dahlke, for his advice on this problem.

Thanks are also due to Rajan Varughese, Julie A. Shimer and David Greve for the samples.

I gratefully acknowledge the support of a National Science Foundation research project during the course of this work.

The solid state laser used in this work was a kind gift from the RCA Laboratories, Princeton.

TABLE OF CONTENTS

	<u>Page</u>
Acknowledgements	iii
Table of Contents	iv
List of Figures	v
Notation	vii
Abstract	1
1. Introduction	2
2. Theory	4
2.1 Trap kinetics	4
2.2 Measurement of trap occupancy	6
2.3 Previous measurements of tunneling time constant	7
3. Experimental	8
3.1 Sample preparation.	8
3.2 Electrical characterization of samples.	9
3.3 Laser assembly.	11
3.4 Photocapacitance measurements	13
4. Discussion	14
5. Conclusions.	17
6. References	19
7. Figures.	20
8. Vita	44

LIST OF FIGURES

1. Energy band diagram of MOS tunnel diode showing interface trap emission and capture processes.
2. Energy band diagram showing trap communicating only with the metal and the conduction band.
3. Equivalent circuit for an n-Si MOS tunnel diode.
4. Structure of MOS tunnel diode.
5. Circuit for measuring I-V characteristics.
6. Circuit for admittance measurements at 5 KHz and 1 MHz.
7. Circuit for admittance measurements using a Lock-In Amplifier.
8. Circuit for quasistatic measurements.
9. J-V characteristic of Cr-45Å SiO₂-n-Si device.
10. J-V curves of Cr-31Å SiO₂-nSi devices.
11. Oxidation time vs. oxidation thickness data.
12. Interface trap density vs. trap energy for Al-50Å SiO₂-pSi device.
13. Block diagram of automated data acquisition system.
14. Interface trap distributions for different annealing conditions.
15. Laser slab.
16. Copper block for cooling laser.
17. Lens and laser assembly.
18. Circuit used for driving laser.
19. Output light intensity vs. laser bias current.
20. Circuit used for measuring photocapacitance transients.

21. Photocapacitance transients for 24 Å device.
Curve 1: in dark; curve 2: at $\phi = 6.10^{16} \text{cm}^{-2} \text{s}^{-1}$;
curve 3: at $\phi = 2.10^{19} \text{cm}^{-2} \text{s}^{-1}$.
22. Trap occupancy vs. trap energy.
23. Photocapacitance transient for 55 Å device.
24. Normalized photocapacitance transients for 24 Å
and 55 Å devices.

NOTATION

(a) = $(f_m - f) / \tau_T$	Emission of hole by tunneling into the metal.
(b) = $\bar{n}(1-f)$	Capture of an electron from the conduction band.
(c) = $(e_n^t + e_n^o)f$	Emission of an electron, thermally or optically, into the conduction band.
(d) = $\bar{p}f$	Capture of a hole from the valence band.
(e) = $(e_p^t + e_p^o)(1-f)$	Emission of a hole, thermally or optically, into the valence band.
f	Trap occupancy
ϕ	Photon flux, energy $h\nu$
$f_m = \left[1 + e^{(E_t - F_m)/kT} \right]^{-1} = \begin{cases} 1 & E_t < F_m \\ 0 & E_t > F_m \end{cases}$	Tunneling controlled occupancy
$f_n = \left[1 + e^{(E_t - F_n)/kT} \right]^{-1} = \begin{cases} 1 & E_t < F_n \\ 0 & E_t > F_n \end{cases}$	Electron thermal recombination controlled occupancy
$f_p = \left[1 + e^{(E_t - F_p)/kT} \right]^{-1} = \begin{cases} 1 & E_t < F_p \\ 0 & E_t > F_p \end{cases}$	Hole thermal recombination controlled occupancy
$f_L = \sigma_p^o (\sigma_p^o + \sigma_n^o)^{-1}$	Optically controlled occupancy
f_u	Unmodulated trap occupancy.
$\tau_T = \tau_o e^{\alpha d_{ox}}$	Tunneling time constant
τ_o	Inverse attempt to escape frequency
α	Attenuation coefficient in oxide
d_{ox}	Oxide thickness
$\bar{n} = v_n e^{-(E_c - F_n)/kT}$	Thermal electron capture rate per active trap
$e_n^t = v_n e^{-(E_c - E_t)/kT}$	Thermal electron emission rate per active trap

e_n^o	Optical electron emission rate per active trap
$\bar{p} = v_p \bar{e}^{(F_p - E_v)/kT}$	Thermal hole capture rate per active trap
$e_p^t = v_p e^{-(E_t - E_v)/kT}$	Thermal hole emission rate per active trap
$e_p^o = \phi \sigma_p^o$	Optical hole emission rate per active trap
σ_n^t, σ_p^t	Thermal capture cross sections for electrons and holes
$v_n = v_{th} \sigma_n^t N_c$	Electron escape frequency
$v_p = v_{th} \sigma_p^t N_v$	Hole escape frequency
F_n, F_p	Electron and hole quasi-Fermi levels
$\tau = [1/\tau_n + 1/\tau_p + 1/\tau_T + 1/\tau_L]^{-1}$	Trap relaxation time
$\tau_n = (e_n^t + \bar{n})^{-1}$	Thermal electron recombination controlled relaxation time
$\tau_p = (e_p^t + \bar{p})^{-1}$	Thermal hole recombination controlled relaxation time
τ_T	Tunneling controlled relaxation time
$\tau_L = [\phi(\sigma_n^o + \sigma_p^o)]^{-1}$	Optically controlled relaxation time
J_{cm}	Tunneling current density from silicon conduction band to metal
J_{ct}	Current density from conduction band to interface traps
J_{tm}	Tunneling current density from interface traps to the metal
J_{total}	Total current density
$C_o = k_o \epsilon_o / d_{ox}$	Oxide capacitance per unit area

$C_d = k_s \epsilon_o / W$	Depletion capacitance per unit area
$C = [1/C_o + 1/C_d]^{-1}$	High frequency device capacitance
V_g	Applied gate voltage
ΔQ_{it}	Change in charge in interface traps
ΔQ_p	Change in minority carrier charge at interface

ABSTRACT

An InP/InGaAs/In laser has been set up to obtain high photon flux of up to $10^{19} \text{ cm}^{-2} \text{ s}^{-1}$ at 0.74 eV photon energy. High light intensities are useful in the study of interface states in MOS tunnel diodes using photocapacitance and photocurrent transients. Photocapacitance transients have been measured on an n-Si MOS capacitor with a 24 Å thick oxide, at various light intensities between 10^{16} - $10^{19} \text{ cm}^{-2} \text{ s}^{-1}$. At low light intensity it is found that the relaxation of the interface state occupancy is dominated by tunneling from the metal into the interface states. At high light intensity, however, the relaxation is found to be dominated by the thermal generation and recombination of holes, and not by tunneling. This is confirmed by similar measurements on a thick oxide capacitor.

Introduction

The exchange of charge between interface states and the conduction and valence bands of silicon has been studied extensively.¹ In MOS capacitors with ultrathin oxides (45 Å) interface states can exchange charge with the metal too. This process is characterized by a tunneling time constant τ_T which depends upon the nature of the trap, the properties of the oxide and decreases exponentially with decreasing oxide thickness. Furthermore, fluctuations in oxide thickness result in a distribution of tunneling time constants. Thus knowledge of the tunneling time constant for different oxide thickness provides useful information about both the nature of the oxide and the trap.

Shimer and Dahlke² have recently reported a simple and direct method for determining the mean value and the spread of the tunneling time constants from isothermal capacitance transients both with and without illumination. The optical technique requires that the rate at which light empties the interface traps be larger than the rate at which the metal fills these traps. For thinner oxides where the tunneling time constant is smaller a higher light intensity is required. Using a Nernst glower emitting a maximum of $5 \cdot 10^{16}$ photons $\text{cm}^{-2} \text{s}^{-1}$, Shimer and Dahlke could measure tunneling time constants for oxide thicknesses down to 24 Å. A higher

light intensity is required to measure time constants for thinner oxides.

This thesis presents results of a study of the thermal growth of pinhole free oxide films 15-50 Å thick on both n- and p-type silicon substrates. Uniform pinhole free oxide films have been grown reproducibly and forming gas anneals have been successfully used to obtain interface state densities as low as $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$.

A solid state laser has been used to provide light intensities up to $10^{19} \text{ cm}^{-2} \text{ s}^{-1}$. Measurements of the photocapacitance transients are presented for a 24 Å thick oxide under varying light intensity. It is found that for a valid measurement of the tunneling time constant τ_T , the light time constant τ_L should not be significantly less than τ_T . If $\tau_L \ll \tau_T$, inversion charge builds up and the relaxation of the trap occupancy is no longer dominated by tunneling but by the recombination of holes.

Section 2 presents a discussion of the trap kinetics. Section 3 describes the sample fabrication, the measurement apparatus, experimental sequence and the measured data. This data is explained in Section 4. Finally, conclusions are stated in Section 5.

2. Theory^{3,4}

2.1 Trap kinetics

We consider a trap at the interface of an MOS device, illuminated with light $h\nu < E_G$. The trap can exchange charge with the metal and semiconductor bands by the following processes, illustrated in Fig. 1:

- (a) Hole emission (or electron capture) by tunneling into the metal.
- (b) Electron capture from the silicon conduction band.
- (c) Electron emission (thermal or optical) into the silicon conduction band.
- (d) Hole capture from the silicon valence band.
- (e) Hole emission (thermal or optical) into the silicon valence band.

Using Fig. 1 and the expressions in the Notation, the rate equation for the trap can be written as

$$\frac{df}{dt} = \frac{f_u - f}{\tau} \quad (1)$$

where f_u is the unmodulated trap occupancy and

$$f_u = \frac{\tau}{\tau_n} f_n + \frac{\tau}{\tau_p} f_p + \frac{\tau}{\tau_T} f_m + \frac{\tau}{\tau_L} f_L \quad (2)$$

$$\frac{1}{\tau} = \frac{1}{\tau_n} + \frac{1}{\tau_p} + \frac{1}{\tau_T} + \frac{1}{\tau_L} \quad (3)$$

Equation (1) is a first order differential equation with solutions that decay exponentially in time, with a relaxation time τ .

Since the thermal emission rates, given in the Notation, depend exponentially on trap energy, the relaxation time τ depends strongly upon the trap energy. Furthermore, the faster the process (e.g. electron emission), the smaller is the corresponding time constant (τ_n) for a given trap. The net relaxation time τ is determined by the fastest process. Similarly the occupancy f_u is also determined by the fastest process.

This is illustrated in Fig. 2, where a hypothetical interface trap communicates only with the conduction band of the semiconductor and the metal. We consider a trap with energy E_t between F_m and F_n . If the trap occupancy f is larger than the electron recombination occupancy f_n , then electrons are emitted by the trap into the conduction band at a rate τ_n^{-1} , and f approaches f_n . But simultaneously since $f_m > f$, electrons tunnel from the metal into the trap. If the tunneling time constant τ_T is much smaller than the electron emission time constant e_n^{t-1} , then the trap is filled up by tunneling much faster than it can be emptied by electron emission and the trap occupancy f is approximately equal to f_m . On the other hand, if $e_n^{t-1} \ll \tau_T$ then the trap is emptied by electron emission faster than it can be filled by the metal and f approaches f_n . Thus, the steady state occupancy is determined by the fastest process.

2.2. Measurement of trap occupancy

Several techniques have been developed to determine these time constants. Conceptually the method is simple: disturb the trap occupancy and observe the relaxation back to steady state.

As the occupancy relaxes, there is a change in the charge at the interface. This charge is displaced partly into the semiconductor space charge region and partly into the metal. This results in an external current which can be measured and related to the relaxation of the trap occupancy. Figure 3 shows the corresponding equivalent circuit; the symbols are defined in the Notation.

Under constant V_G , straightforward circuit analysis yields

$$J_{\text{total}} = -\frac{C}{C_o} J_{\text{TM}} - \frac{C}{C_d} J_{\text{CT}} - J_{\text{CM}} \quad (4)$$

Note that the equivalent circuit is valid regardless of the time dependence of the various currents. Since the measurements are performed when the semiconductor surface is depleted, $C \approx C_d \sim 0.01 C_o$. Under these conditions

$$J_{\text{total}} \approx -\frac{C_d}{C_o} J_{\text{TM}} - J_{\text{CT}} - J_{\text{CM}} \quad (5)$$

Thus only a very small fraction of the current between the interface traps and the metal appears in the external circuit. In addition, there is an appreciable dark current J_{CM} flowing in the circuit. Thus monitoring the trap occupancy by measuring the external current is

difficult in dark. However, under illumination, by using chopped light and phase sensitive detection, the trap-related currents and the dc reverse current can be separated. Since the present work relates to occupancy changes in dark, current transients were not studied.

Capacitance measurements provide another means of monitoring the trap occupancy. Since the bias across the device is constant, a change in the gate charge results in a change in the device capacitance. The measured change in capacitance is related to the change in total charge at the interface by the following relation:

$$\Delta Q_{it} + \Delta Q_p = \frac{K_s \epsilon_o q N_D C_o}{C^3} \Delta C \quad (6)$$

where it is assumed that $\Delta C/C \ll 1$. Thus the change in capacitance is directly proportional to the change in interface charge. If ΔQ_{it} is positive so is ΔC and vice versa.

2.3 Previous measurements of tunneling time constants

In Ref. (5), the following quantities were determined from capacitance transients measurements with and without light.

$$\alpha = 0.5 \text{ \AA}^{-1} \pm 10\%$$

$$\tau_o = 10^{-5} \text{ s}$$

Also it was found that the variation in α with trap energy is only about 10%. For a 24 \AA device this corresponds to $\tau_T \approx 50\text{s}$ near the conduction band edge and

$\tau_T \approx 200$ s near the valence band edge. The variation in τ_T due to oxide thickness variations was determined to be within a factor of 3 from its nominal value.

These results are important for interpreting the present work as is shown in subsequent chapters.

3. Experimental

3.1 Sample preparation

The growth of uniform pinhole free oxide films is essential for reliable studies of tunneling in MOS devices. Band-to-band tunneling currents are especially sensitive to defects in the oxide which result in low resistance paths through the oxide. This is because mobile carriers are free to move laterally, and therefore current flow occurs preferentially through such defects. On the other hand, since interface traps are localized in space, tunneling into these traps is relatively insensitive to defects in the oxide.

In collaboration with a colleague, Mr. Rajan Varughese, a study was undertaken to study the growth of pinhole-free oxide films. MOS capacitors (Fig. 4a) were fabricated on n- and p-type silicon <100> orientation, 6-14 Ω cm and on 4 Ω cm epitaxial p- on p⁺-Si substrates. The surface was degreased in solvents and etched in HF prior to oxidation. Oxidation was carried out in dry oxygen at 865°C in a fused silica tube for times varying between 1 and

30 minutes. Particular care was taken to avoid dust during wafer handling. After the oxidation the wafer was left close to the furnace mouth, to cool for about 5 min. This was done to prevent uncontrolled oxide growth which occurs upon introducing the hot wafer to the humid environment. Some wafers were then annealed in N_2 at $865^\circ C$ or in forming gas at $425^\circ C$ for 20 minutes. Chromium or aluminum front contacts were then evaporated on to the wafers in an ion pump system. After removing the back surface oxide, aluminum was evaporated on the back.

After preliminary results, photolithographic processes were used to fabricate structures shown in Fig. (4b). The details have been presented elsewhere.⁶

3.2 Electrical characterization of samples

Electrical measurements were made using a spring-loaded probe in a light-tight box. The box was continuously flushed with dry nitrogen to reduce surface leakage and anomalous inversion layer effects. Current-voltage characteristics were measured using the circuit shown in Fig. 5. Device admittance was measured at 5 KHz and 1 MHz using the Boonton model 75C-513 and 75A-58, respectively. The circuit is shown in Fig. 6. At other frequencies varying from 10 Hz to 100 KHz, admittance was measured using a PAR model 129A lock-in amplifier, as shown in Fig. 7. For devices of 45 \AA or

more oxide thickness, where the dc leakage current was extremely small, quasistatic capacitance voltage characteristic was measured using the circuit shown in Fig. 8.

Both device structures shown in Fig. 5 exhibited similar characteristics. Here, we present only the major results of the study. Figure 9 shows a typical J-V characteristic for a 45 Å thick oxide. Here J_F and J_R denote forward and reverse current densities. The cross denotes the current density reported in Ref. (7) for a similar device at a gate voltage of +1V. For two 32 Å devices the curves are shown in Fig. 10. These devices were made in separate runs, but for the same oxidation time. This demonstrates that oxide films can be grown fairly reproducibly. Though not shown in the figure, current densities are very uniform across entire surfaces of individual wafers. We have estimated that the variation in oxide thickness is less than 3 Å over a wafer and less than 5 Å from run to run. Also shown in Fig. 10 are the current densities reported in Refs. (7-9) for similar oxide thicknesses. It is found that for the same oxide thickness current densities in our devices are orders of magnitude smaller than those reported previously. This, combined with the fact that there is little variation in current density from device to device, wafer to wafer, we believe, is satisfactory proof that these oxide films are pinhole free. Figure 11 shows the oxidation

thickness vs. time data obtained after several runs.

The control of interface state density was a second major aim of this study. Figure 12 shows the interface trap distribution for a Al-50Å SiO₂-pSi sample as obtained from quasistatic and 10 Hz capacitance measurements. It is seen that the quasistatic gives a higher interface trap density. This was consistently found to be true, although the reasons are not clear yet. To facilitate rapid measurement of the quasistatic, an analog to digital converter and an HP85 computer were used to automate the measurement and analysis. A block diagram of the circuit is shown in Fig. 13. Figure 14 depicts the effect of annealing on interface trap density.

In conclusion, thin pinhole-free oxide films have been grown reproducibly. Using forming gas anneals, interface trap density of $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ has been obtained.

3.3 Laser assembly

Photocapacitance measurements were performed using an InP/InGaAs/In semiconductor laser operating at 1.68 μm. Figure 15 shows a schematic of the copper slab on the left end of which the laser is mounted. The p⁺ end of the laser is in contact with the slab. The n⁺ end is bonded to a wire which leads to a metal plate sitting on the insulator. The laser emits only from the side facing away from the slab towards the left. In order to

prolong the life of the laser, it must be prevented from heating up. This is done by mounting the laser on a copper block which in turn is cooled by a thermoelectric cooler. Figure 16 shows the copper block with the laser slab in place.

Since the laser beam diverges at roughly 25° angles, it is necessary to use a lens with an $f\#$ close to unity or less in order to collect all the radiation. A microscope objective mounted next to the laser as shown in Fig. 17 has been used to focus the beam roughly 22 cm away from the laser. The lens and laser assembly is then mounted onto a three-dimensional micropositioner to facilitate accurate alignment of the spot on the sample.

In order to obtain the highest intensity the spot size was adjusted to about 0.2 mm diameter. In order to prevent vibrations from shifting to spot position, the lens and laser assemblies were kept firmly in place by applying apezion wax.

Figure 18 shows the circuit used for pulsing the laser current at a frequency of 10 KHz and a 25% duty cycle ratio. The current is monitored by measuring the voltage drop across a wire wound 0.5Ω resistor placed in series with the laser. The base drive of the transistor is pulsed at the desired frequency and duty cycle. The switch in the base lead is used to switch the laser on

and off. Since currents up to 0.5 A have to be switched at high frequencies, special care must be taken to prevent the power supply from oscillating. In particular, thick interwoven copper wires are used for the supply, to minimize lead inductance. Further, a 200 μ F capacitor is used in shunt across the transistor to stabilize the voltage at that point. The light intensity was measured using a Precision Laser model kT-20101H pyroelectric detector as described previously.⁴ Figure 19 shows the measured light intensity as a function of a laser bias current. Neutral density filters, placed between the laser and the device, were used to vary the intensity of light falling on the device.

3.4 Photocapacitance measurements

Two samples with 24 Å and 56 Å thick oxides were measured in this study. The sample is mounted in a cryostat and can be maintained at temperatures from 77K to 300K. The operation of the cryostat and the temperature controller was described in detail earlier.⁴ Figure 20 shows the circuit used for measurement of the photocapacitance transients. The Boonton capacitance meter has a response time of 2 ms and a maximum sensitivity of 1V/pF.

The experimental sequence is as follows. The device is cooled to 81K and forward biased to 1V for a period

of two minutes. At time $t=0$, the bias is switched to $-1V$ and the subsequent capacitance transient is recorded on an X-Y recorder. At $t=10s$ the light is switched on. At $t=75s$ the light is switched off.

Figure 21 shows the measured capacitance transients for the 24 \AA device. The curve labeled 1 is the capacitance transient when the sample is kept in dark all the time. Curves 2 and 3 show the transients at different light intensities.

4. Discussion

Figure 22 shows the trap occupancy as a function of trap energy. At $t=0$ all the interface traps up to the conduction band are filled. As soon as the bias is switched to $-1V$, electrons are thermally emitted into the conduction band. The rate at which this process occurs is determined by e_n^t . Since the time constant for thermal emission of electrons is exponentially dependent on trap energy, the rate of emission is largest for traps near the conduction band edge. Shallow traps are emptied first and deeper traps later.

Thus the rate of emission is initially large and becomes slower with the passage of time. At the same time the traps are exchanging charge with the metal too, at a rate determined by the tunneling time constant τ_T .

The resulting capacitance transient can be used to obtain the tunneling time constant, as described in Ref. (5).

For the light intensity in curve 2, the light time constant τ_L is smaller than the tunneling time constant. At $t=10\text{s}$, the dynamic trap Fermi level is at the level shown by $F_{tn}(t=10\text{s})$. After the light intensity is switched on the light controlled occupancy f_L is established in time τ_L . For a photon flux of $5 \cdot 10^{16} \text{ cm}^{-2} \text{ s}^{-1}$, $\tau_L \approx 20\text{s}$. After the light is switched off, the capacitance is seen to decay slowly. A decrease in the capacitance means that the net charge in the interface traps Q_{it} is decreasing. It was shown in Ref. (2) that this decay in capacitance occurs because electrons tunnel from the metal into the interface traps. This process takes a time of the order of the tunneling time constant.

Curve 3 shows the transient at $\phi = 2 \cdot 10^{19} \text{ cm}^{-2} \text{ s}^{-1}$. As before, after the light is switched on, the light controlled occupancy is established in a time τ_L . In this case, however, $\tau_L \approx 50 \text{ ms}$ and so the capacitance transient is almost abrupt. After the light is switched off, the capacitance decays rapidly initially and slowly later. This behavior is markedly different from curve 2

where the capacitance decay was significantly slower.

For curve 2, the decay in capacitance after light is switched off is attributed to tunneling from the metal. If this were true for curve 3 too, then one would expect the capacitance to decay at the same rate as in curve 2. Clearly, this is not the case. The capacitance decays initially with a time constant of roughly 0.2 sec in curve 3. Some other process which occurs much more rapidly than tunneling is now dominant. This process can not be capture of electrons since the device is in deep depletion and the electron capture time is extremely long.

Now, at high light intensities, electron hole pairs are generated at a very large rate, and an inversion charge builds up. This means that states start capturing holes and the trap occupancy changes from its light controlled value. Thus the interface charge increases because of the capture of holes. This explains the fact that the higher the light intensity the higher is the change in capacitance from its value in dark.

As soon as the light is switched off, the previously captured holes are now thermally emitted back into the valence band. The rate at which this process occurs is given by the inverse of the time constant for thermal emission of holes, e_n^t . Since this time constant is

exponentially dependent on trap energy, traps close to the valence band emit holes at a faster rate, and are therefore emptied of holes first. Deeper traps emit holes at a slower rate. This explains the rapid initial decay in capacitance which becomes slower as time passes.

Now, if the initial rapid decay is indeed due to thermal emission of holes and not due to tunneling, then one should observe the same effect in a thick oxide device. This is indeed observed as shown in Fig. 23. The thin and thick devices have different interface trap densities. For comparing the time dependence of the decay in capacitance for the two cases, normalized capacitance transients are plotted in Fig. 24. Here, the capacitance at the instant light is switched off, is taken to be unity, and the final limiting value of capacitance in dark is taken to be zero. It is seen that capacitance decay curves for both the 24 Å and 56 Å devices are very similar at high light intensity, and both differ markedly from the transient at low light intensity for the thin oxide. This is evidence that the initial rapid decay of the capacitance transient is due to thermal emission of holes.

5. Conclusions

Photocapacitance transients in MOS tunnel diodes have been measured at varying light intensities. We

find for $\tau_L < \tau_T$ the relaxation of the trap occupancy is dominated by the tunneling time constant τ_T . At high light intensity such that $\tau_L \ll \tau_T$ inversion charge builds up, and the relaxation is no longer dominated by tunneling but instead by the recombination of holes. In future studies we propose to measure tunneling time constants for oxides less than 24 Å thick, using the laser. New models for interface traps will be studied in order to account for the measured tunneling time constants. Using these models the field dependence of the thermal and optical cross sections will also be studied. MOS tunnel diodes on p-Si have been fabricated, which will be used to measure hole photoionization cross section of interface traps.

REFERENCES

1. A. Goetzberger, E. Klausman, M. J. Schulz in
CRC Critical Reviews in Solid State Sciences,
Jan. 1976.
2. J. A. Shimer and W. E. Dahlke. App. Phys. Lett.
40 (1982) 734.
3. W. E. Dahlke and D. W. Greve. Solid State Electron.
22 (1979) 893.
4. D. W. Greve. Ph.D. Dissertation, Lehigh University,
1979.
5. J. A. Shimer, Ph.D. Dissertation, Lehigh University,
1982.
6. Rajan Varughese. Internal Progress Report, Lehigh
University, 1981.
7. P. V. Dressendorfer. Ph.D. Dissertation, Yale
University, 1978.
8. V. Kumar. Ph.D. Dissertation, Lehigh University.
9. Current density was measured on a device made by
D. W. Greve at Lehigh University, 1979.

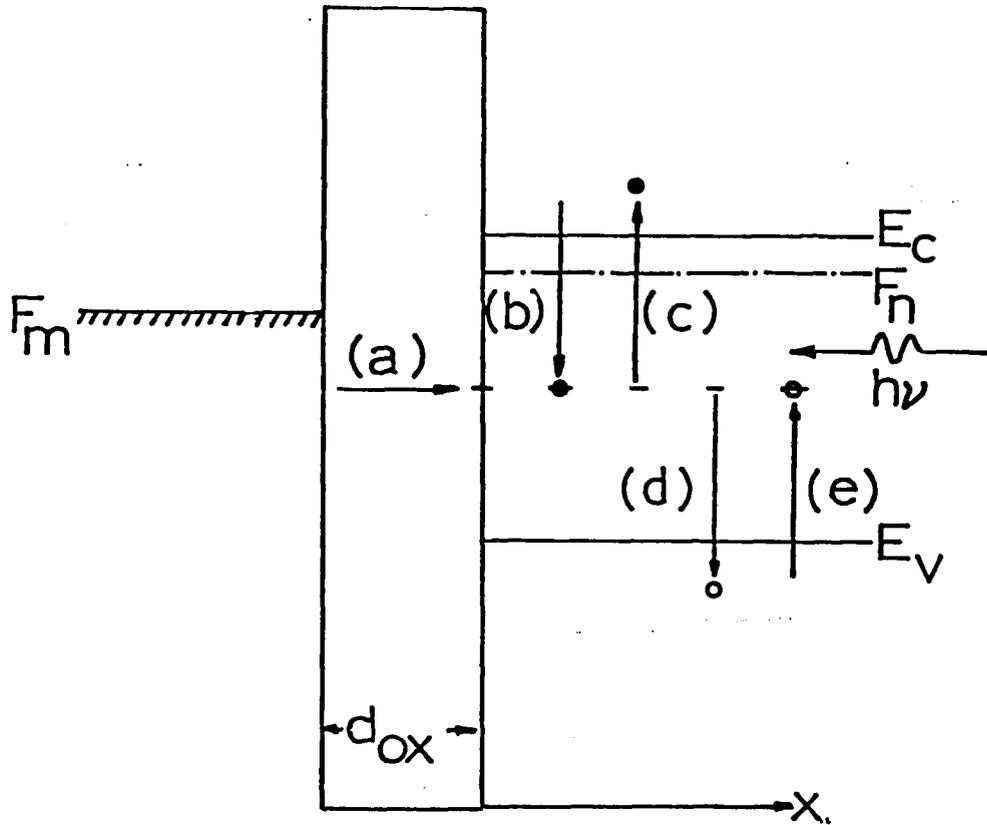


Fig. 1 Energy band diagram of MOS tunnel diode showing interface trap emission and capture processes.

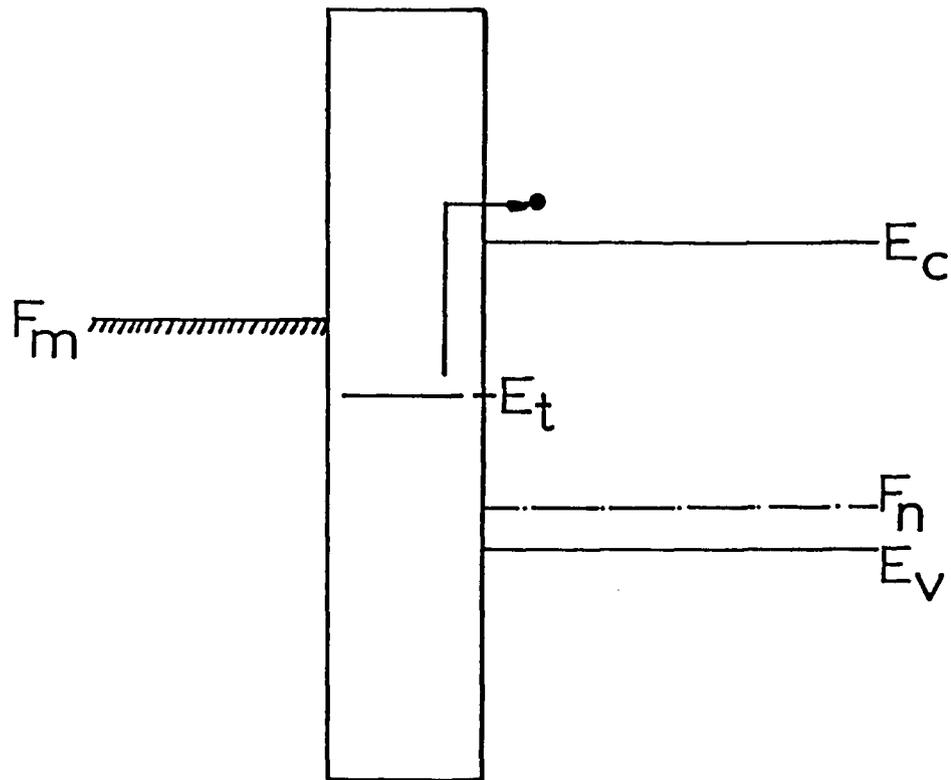


Fig. 2. Energy band diagram showing trap communicating only with the metal and the conduction band.

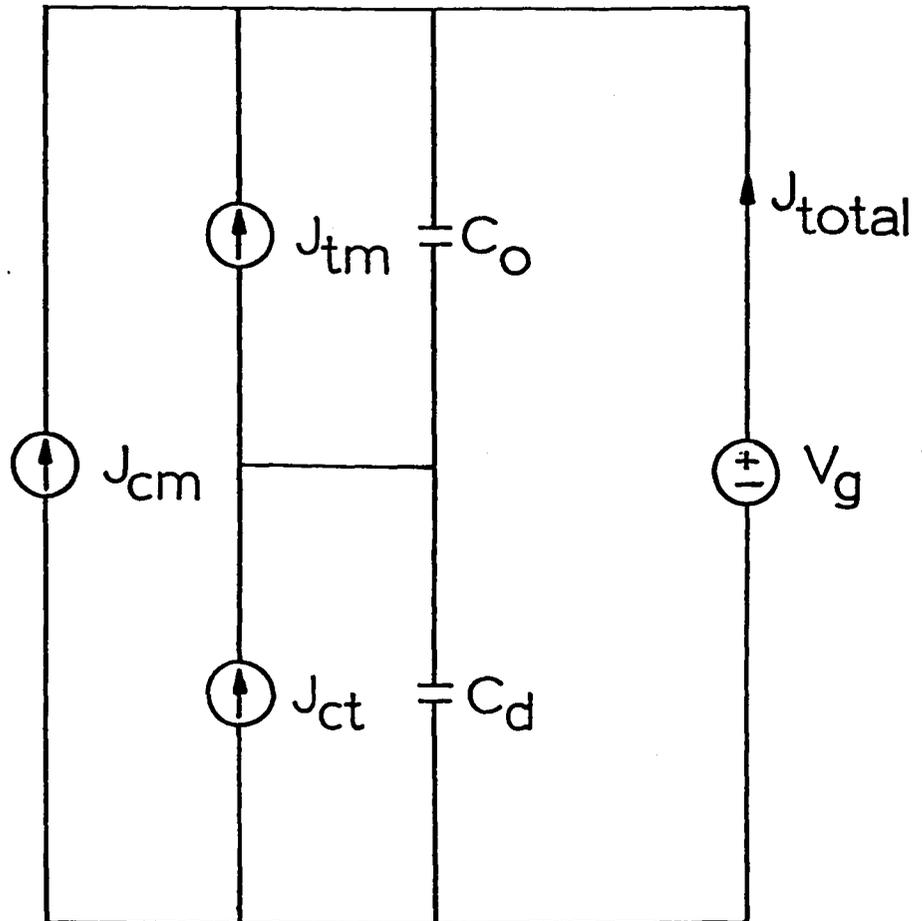


Fig. 3. Equivalent circuit for an n-Si MOS tunnel diode.

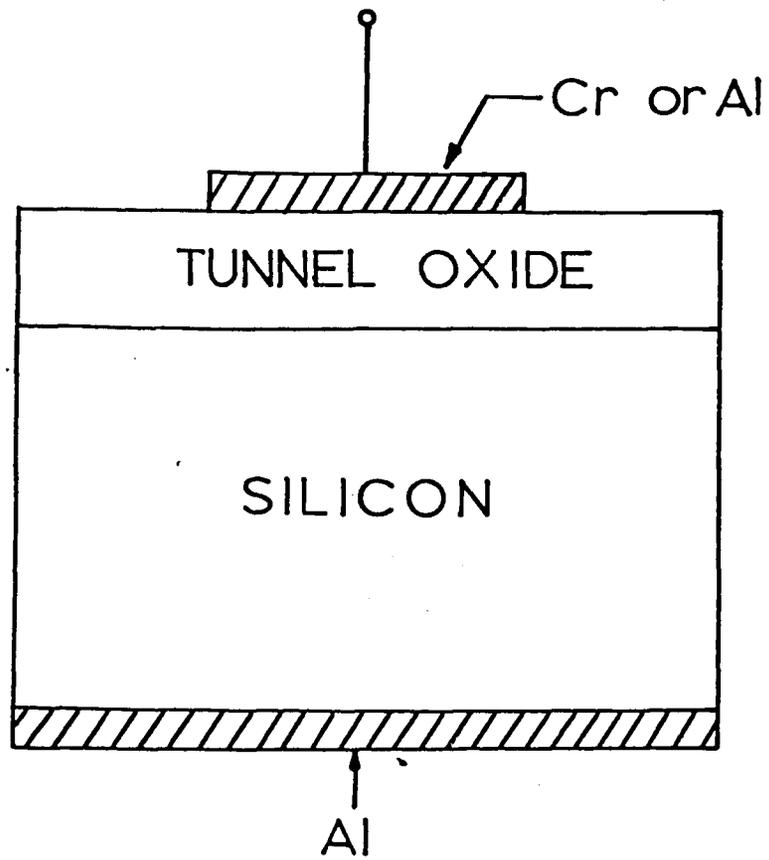


Fig. 4a. Structure of MOS tunnel diode.

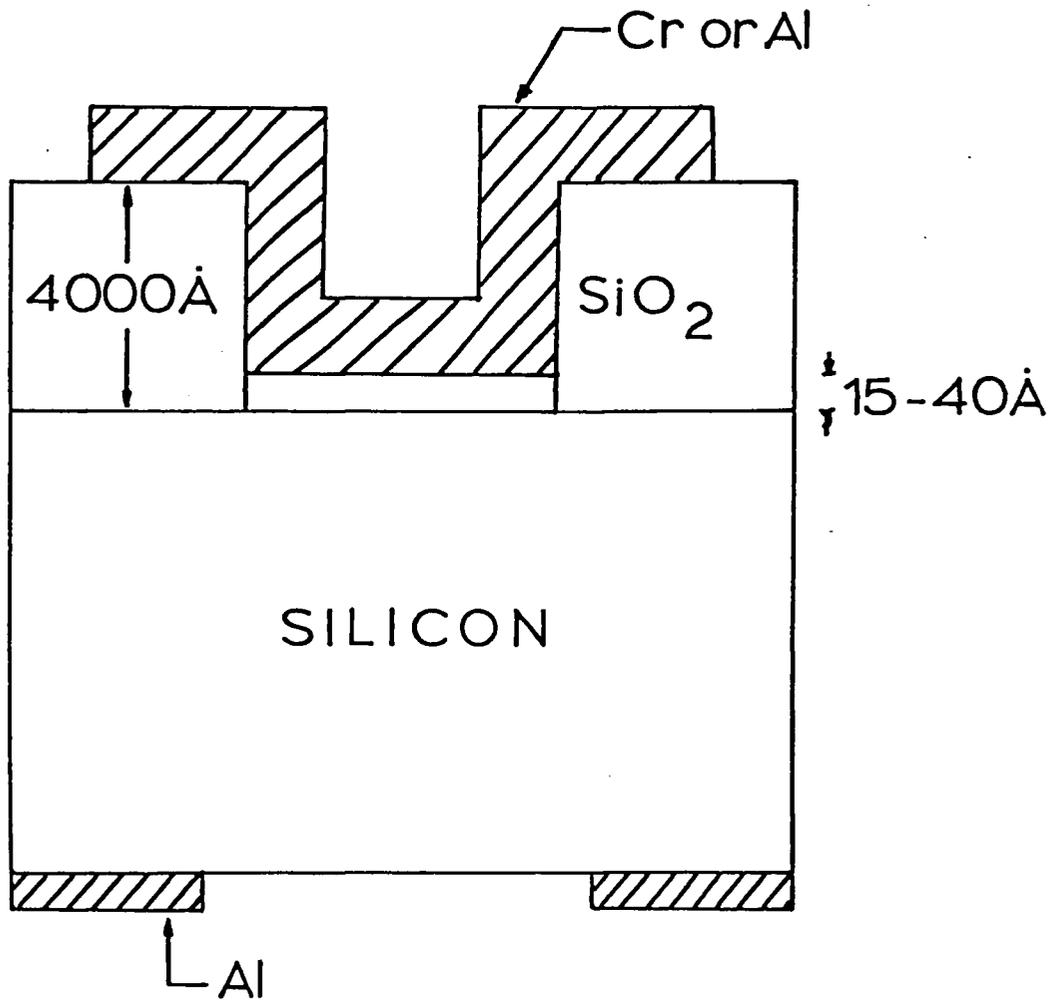


Fig. 4b. Structure of MOS tunnel diode.

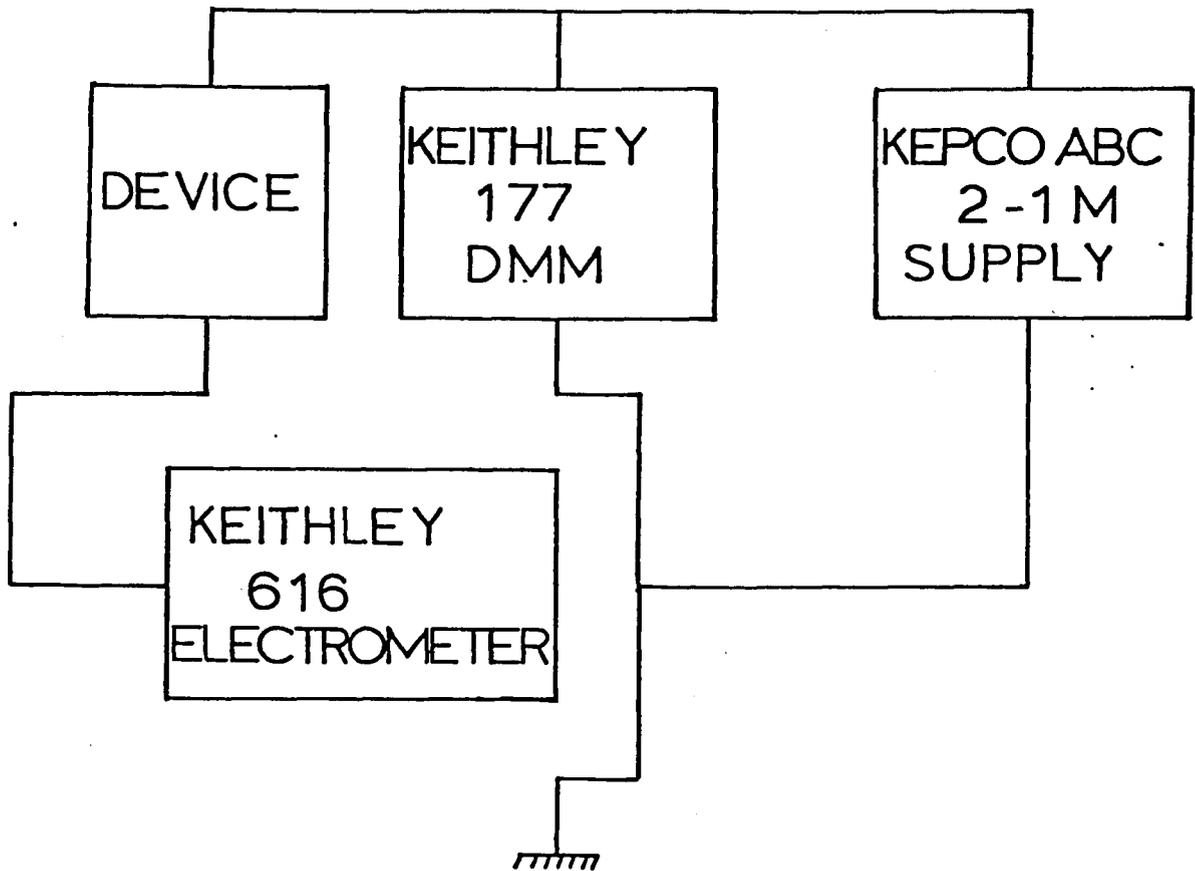


Fig. 5. Circuit for measuring I-V characteristics.

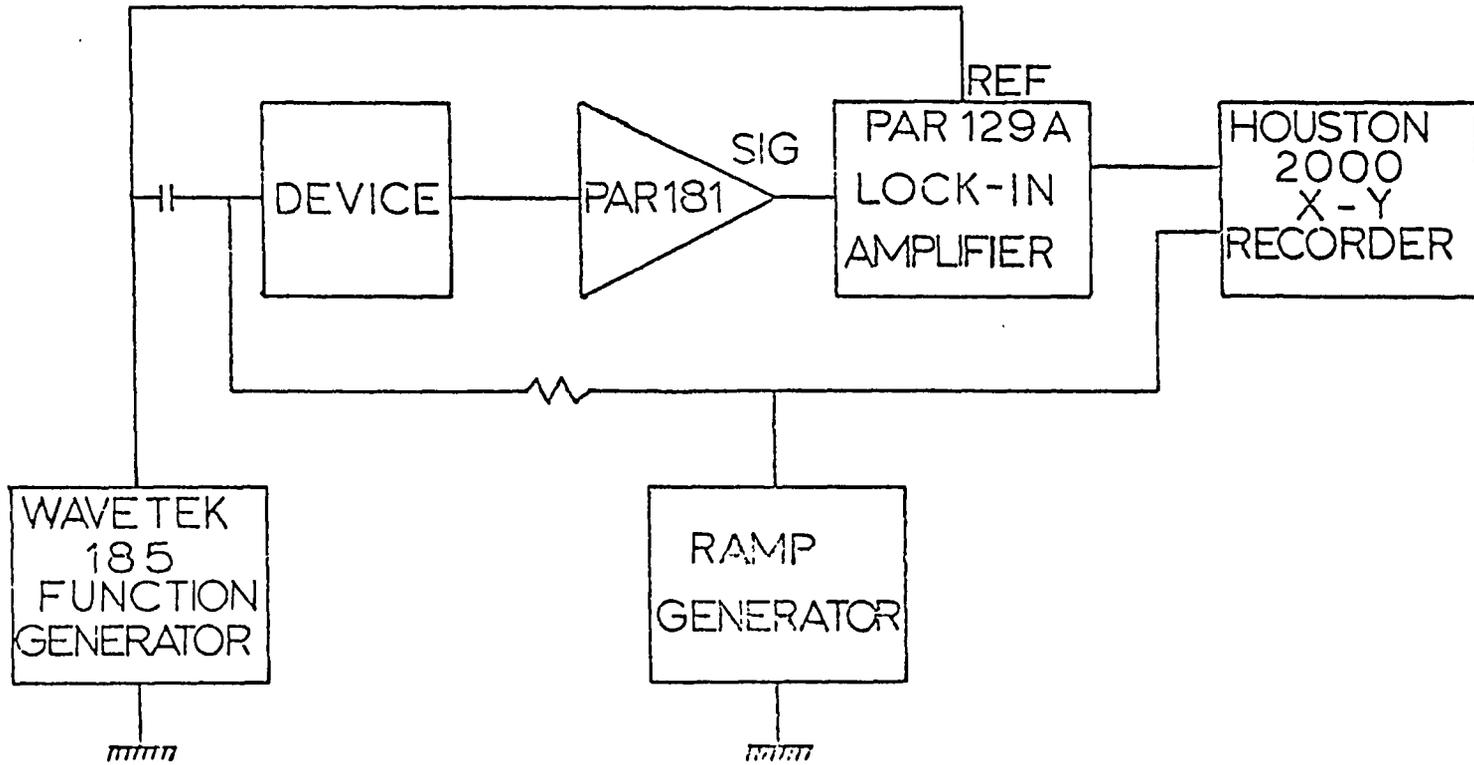


Fig. 7. Circuit for admittance measurements using a Lock-In Amplifier.

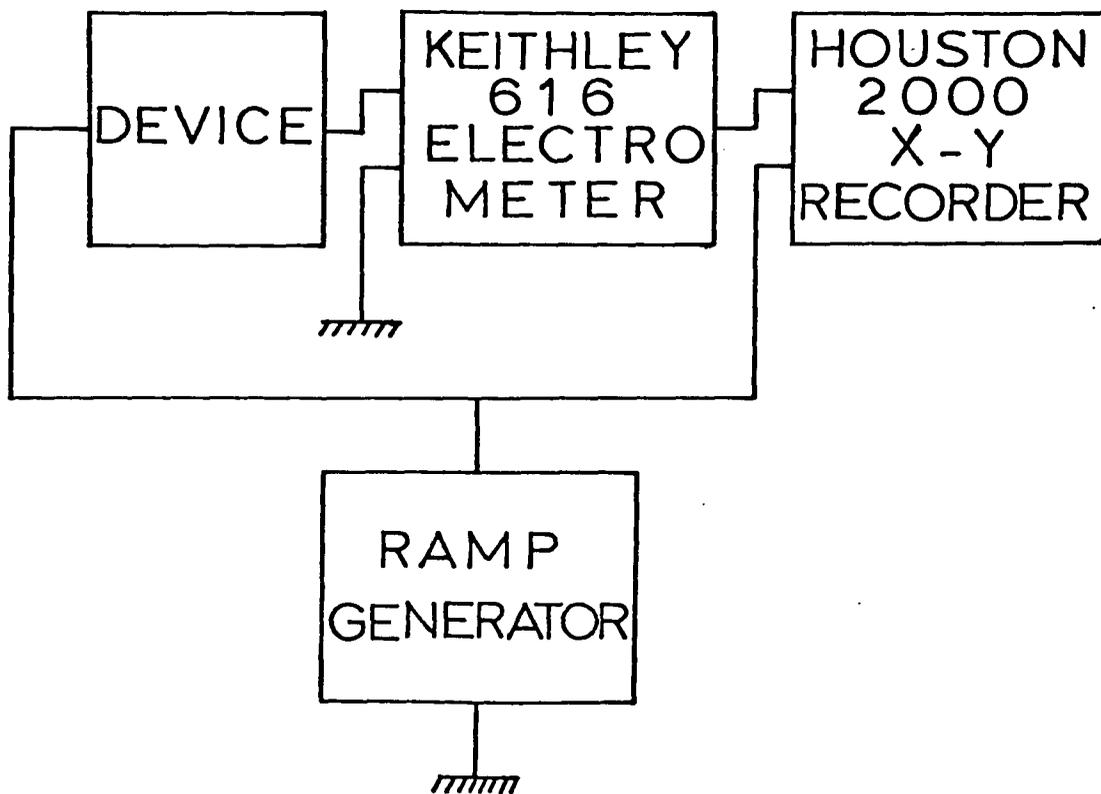


Fig. 3. Circuit for quasistatic measurements.

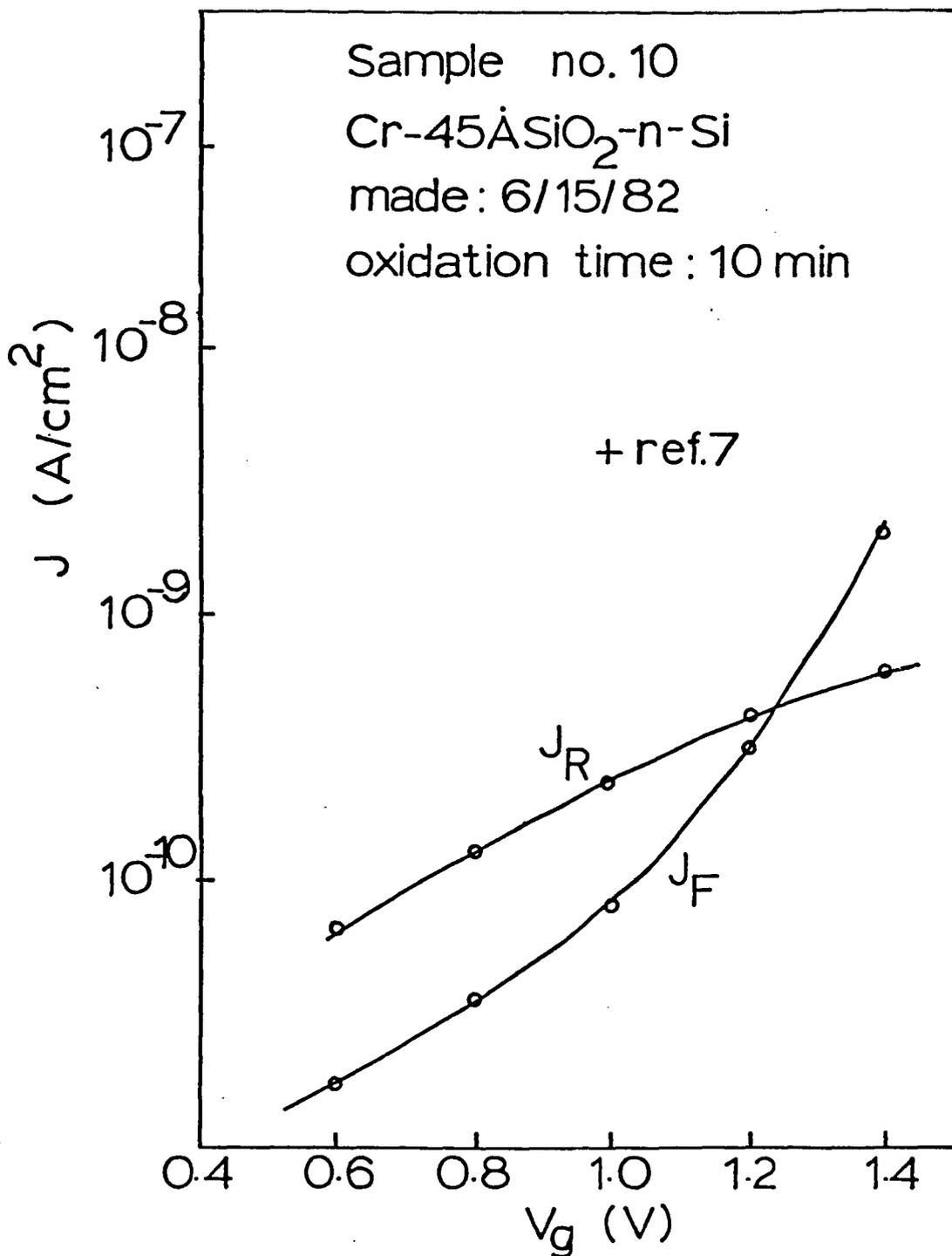


Fig. 9. J-V characteristic of Cr-45ÅSiO₂-n-Si device.

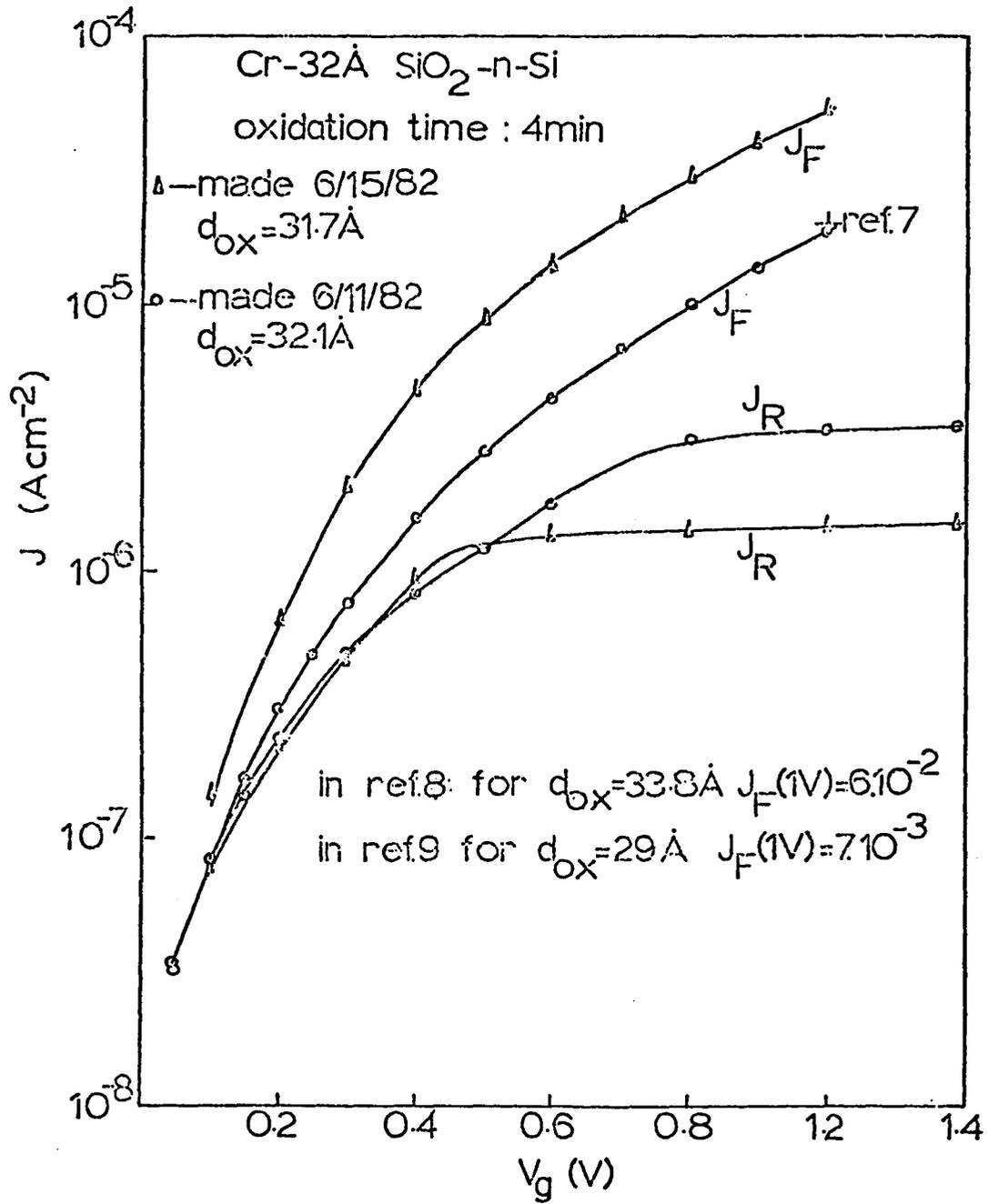


Fig. 10. J-V curves of Cr-31Å SiO₂-nSi devices.

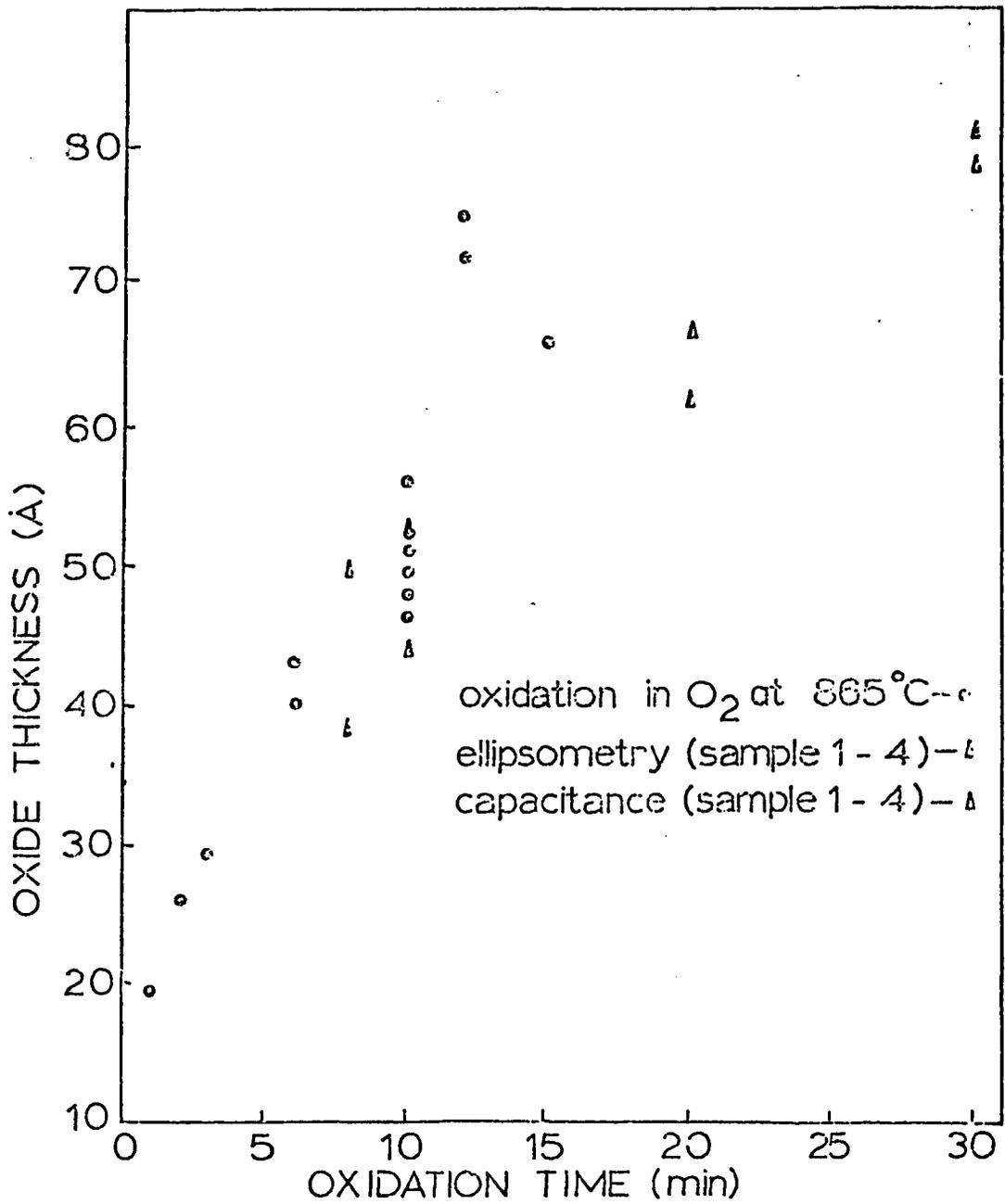


Fig. 11. Oxidation time vs. oxidation thickness data.

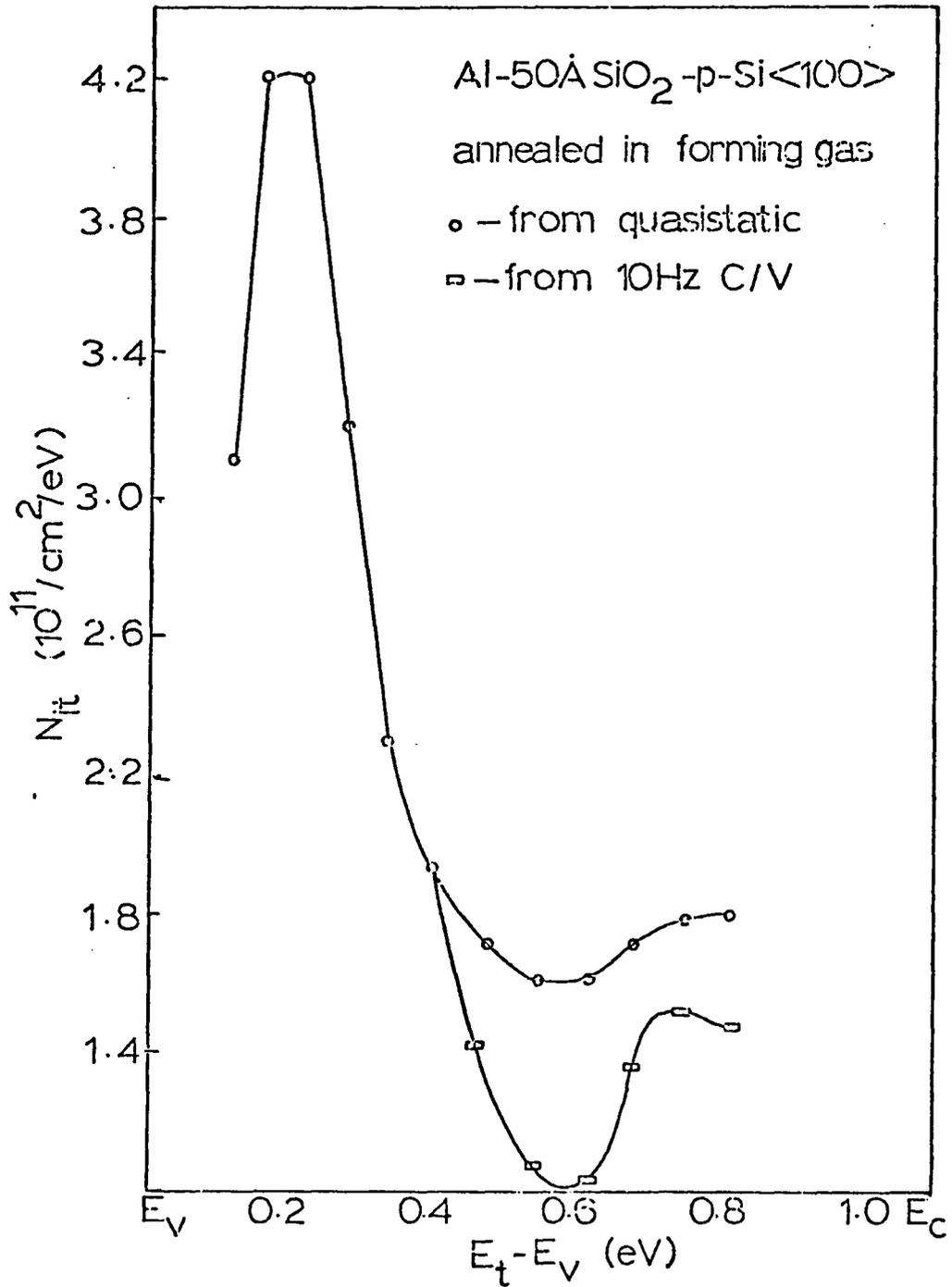
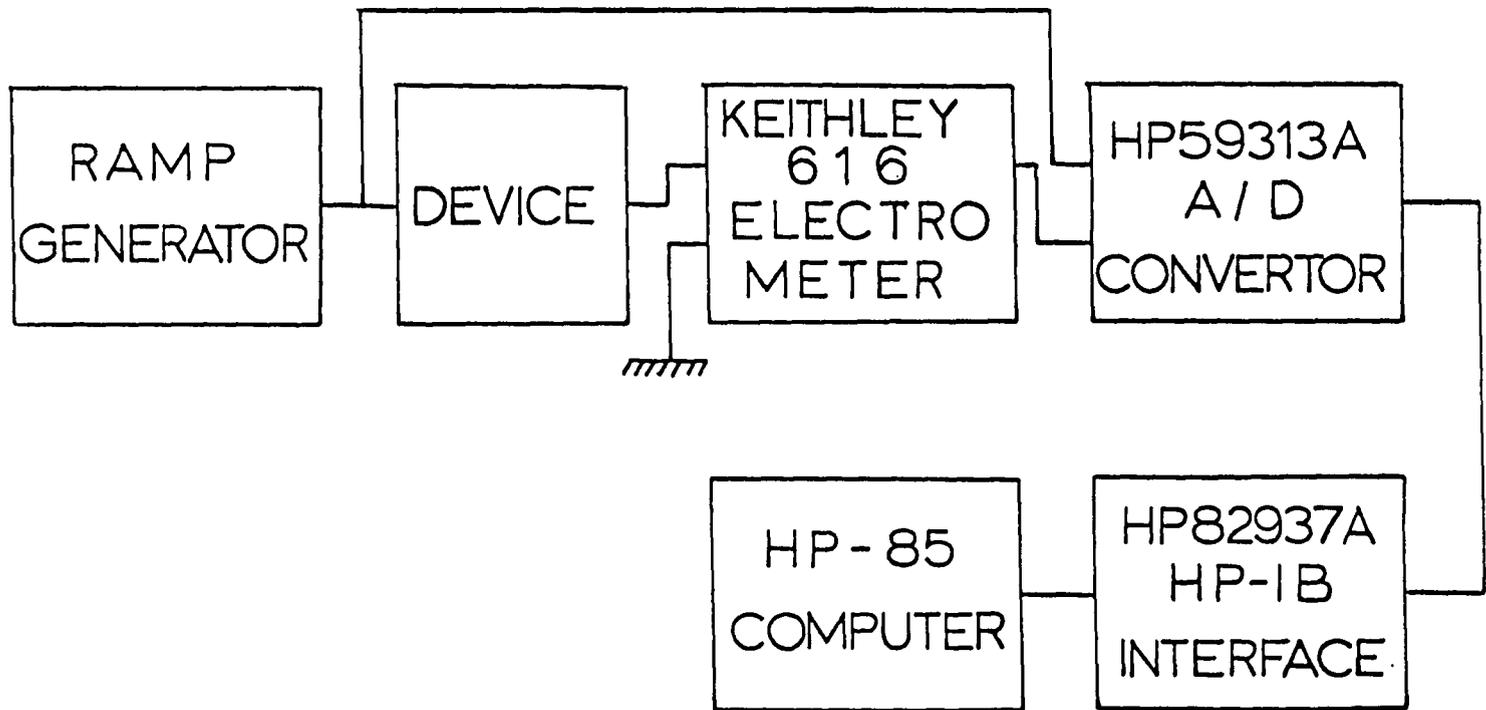


Fig. 12. Interface trap density vs. trap energy for Al-50Å SiO₂-pSi device.



32

Fig. 13. Block diagram of automated data acquisition system.

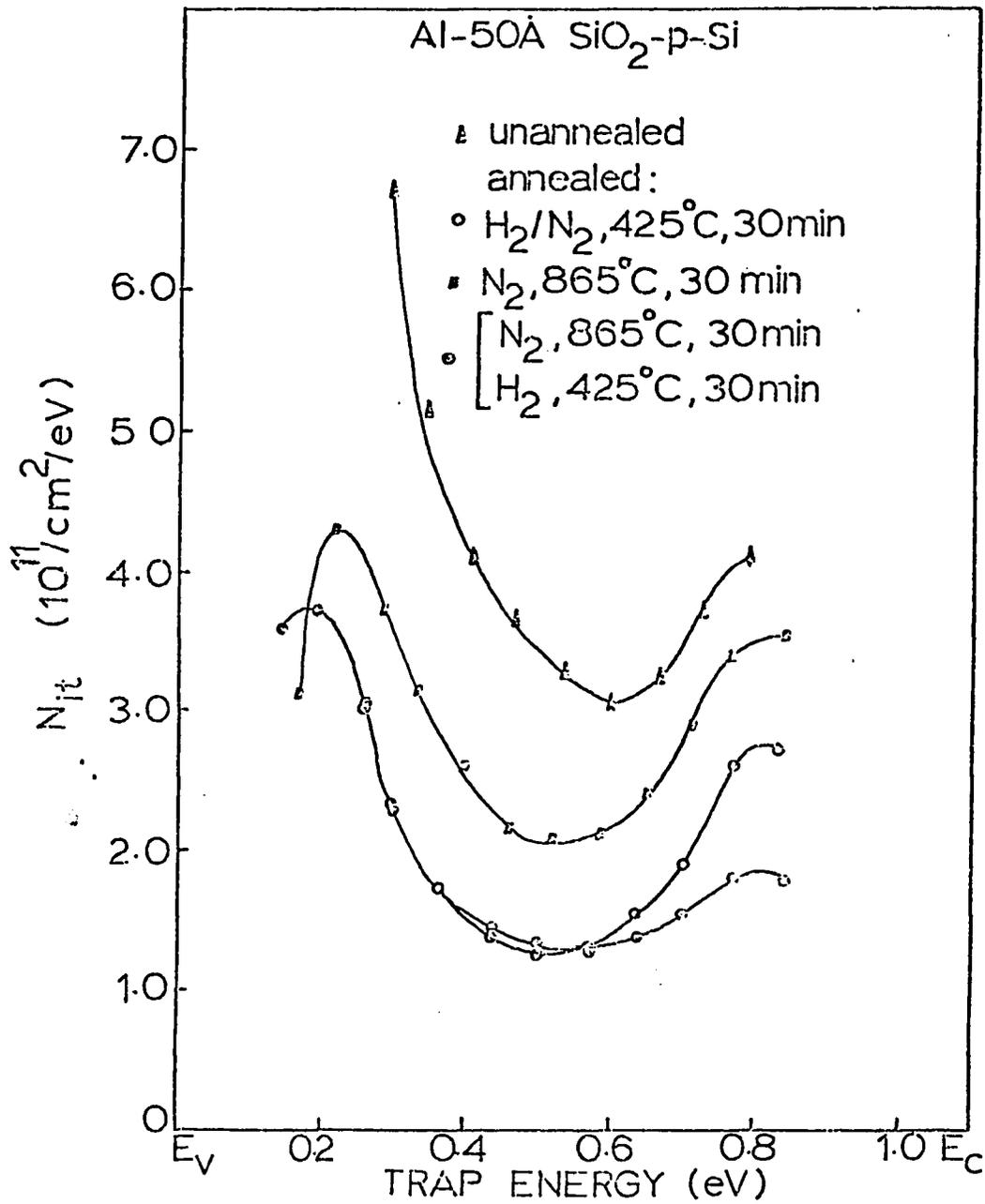


Fig. 14. Interface trap distributions for different annealing conditions.

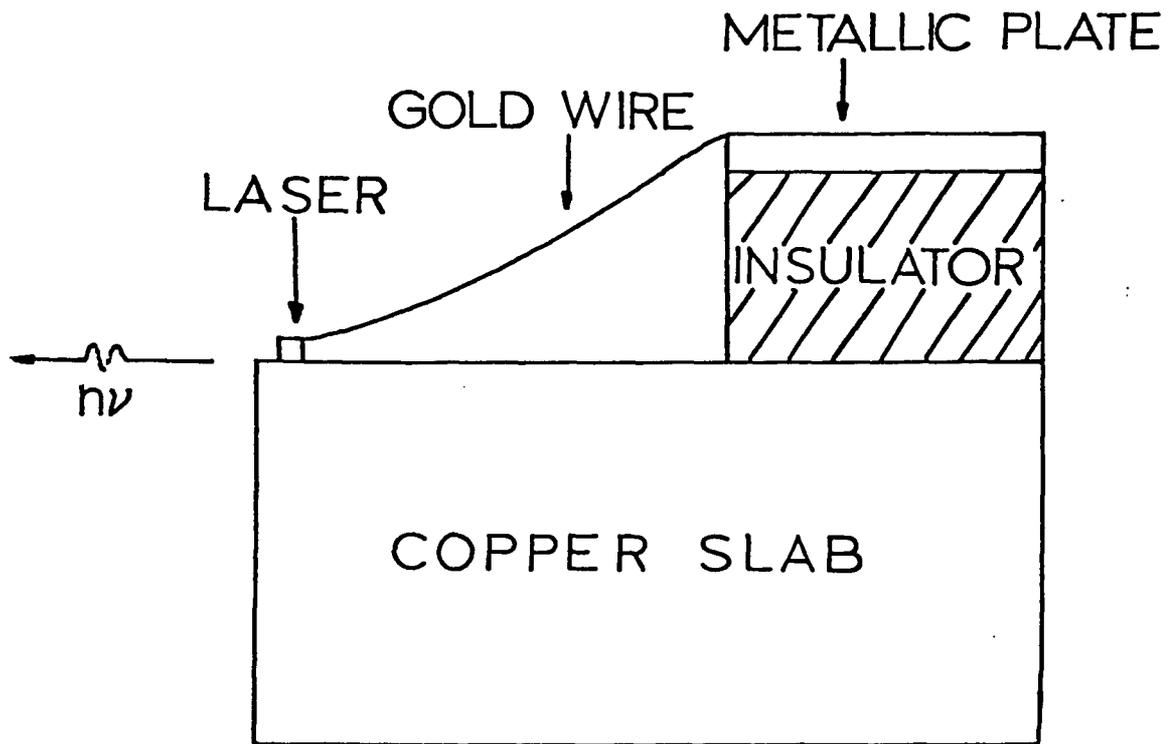


Fig. 15. Laser slab.

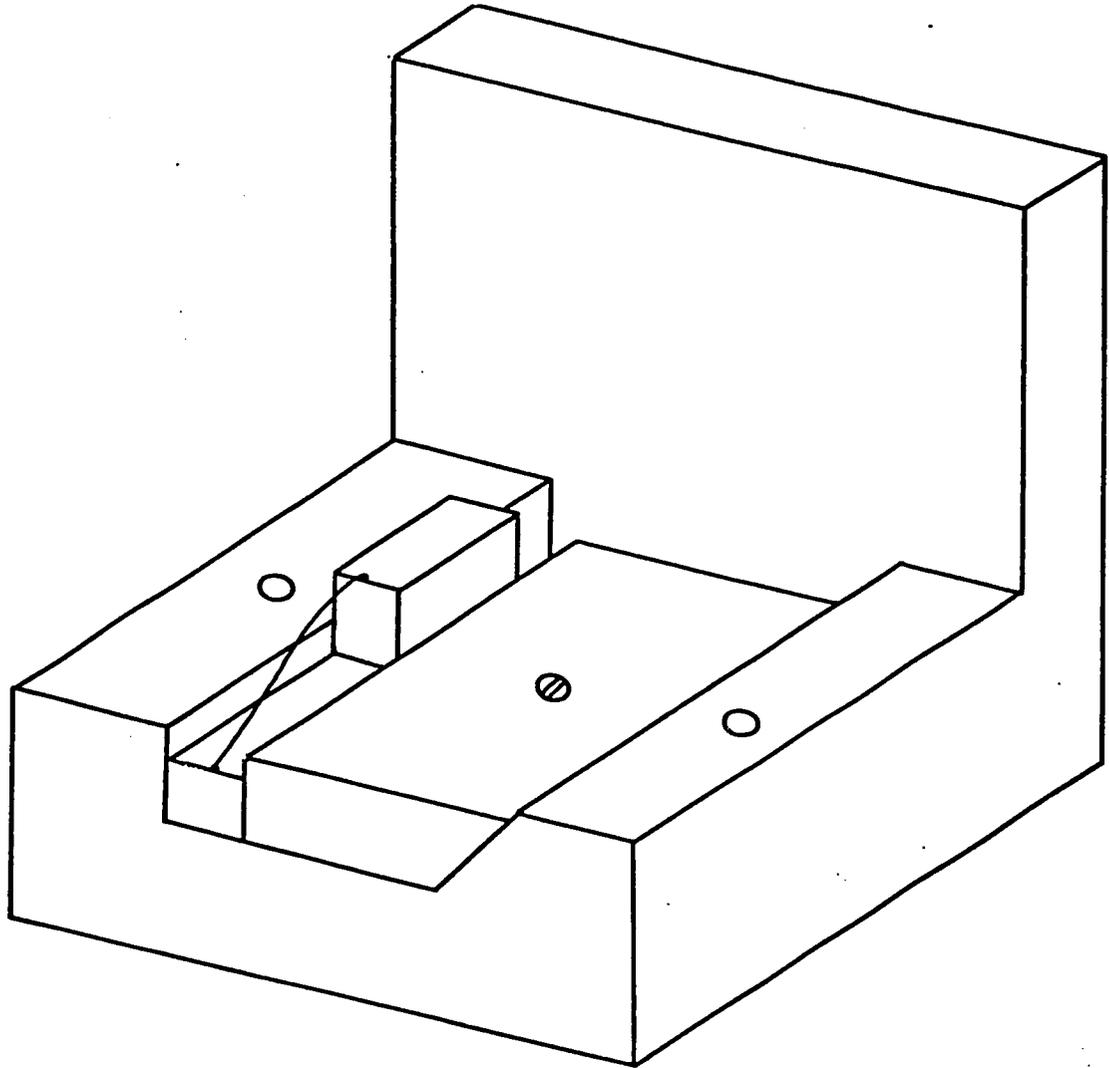


Fig. 16. Copper block for cooling laser.

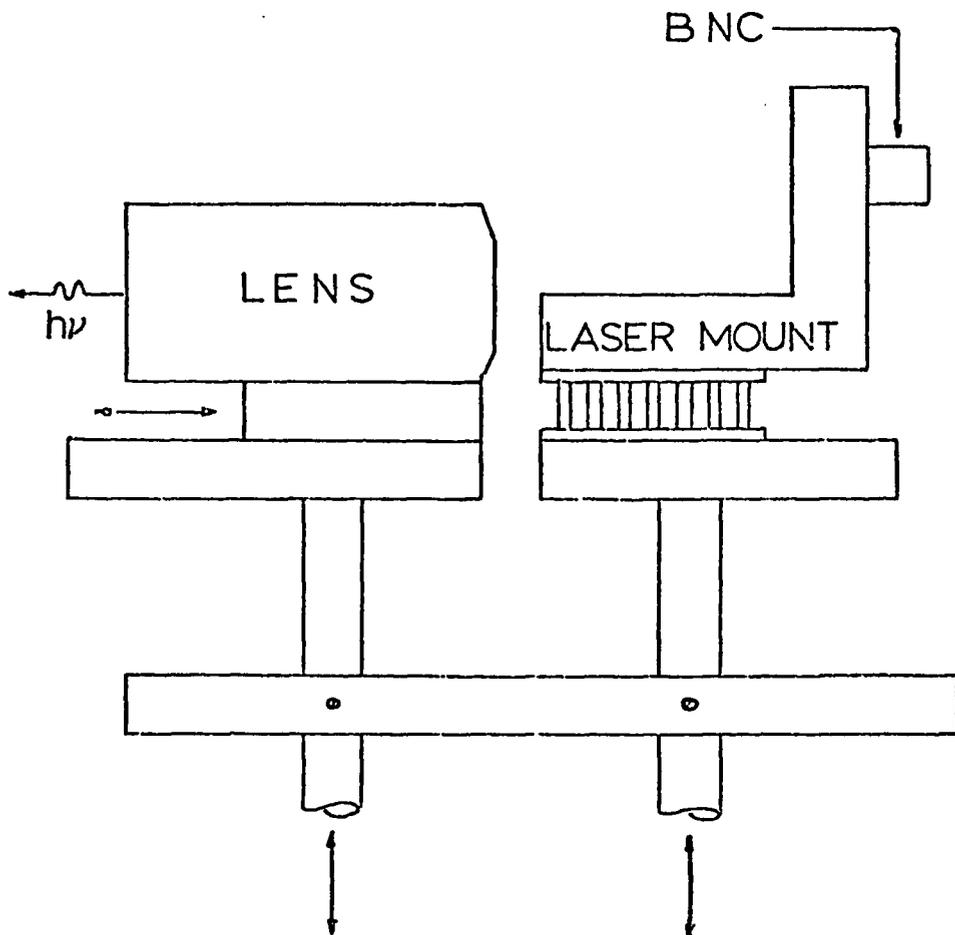


Fig. 17. Lens and laser assembly.

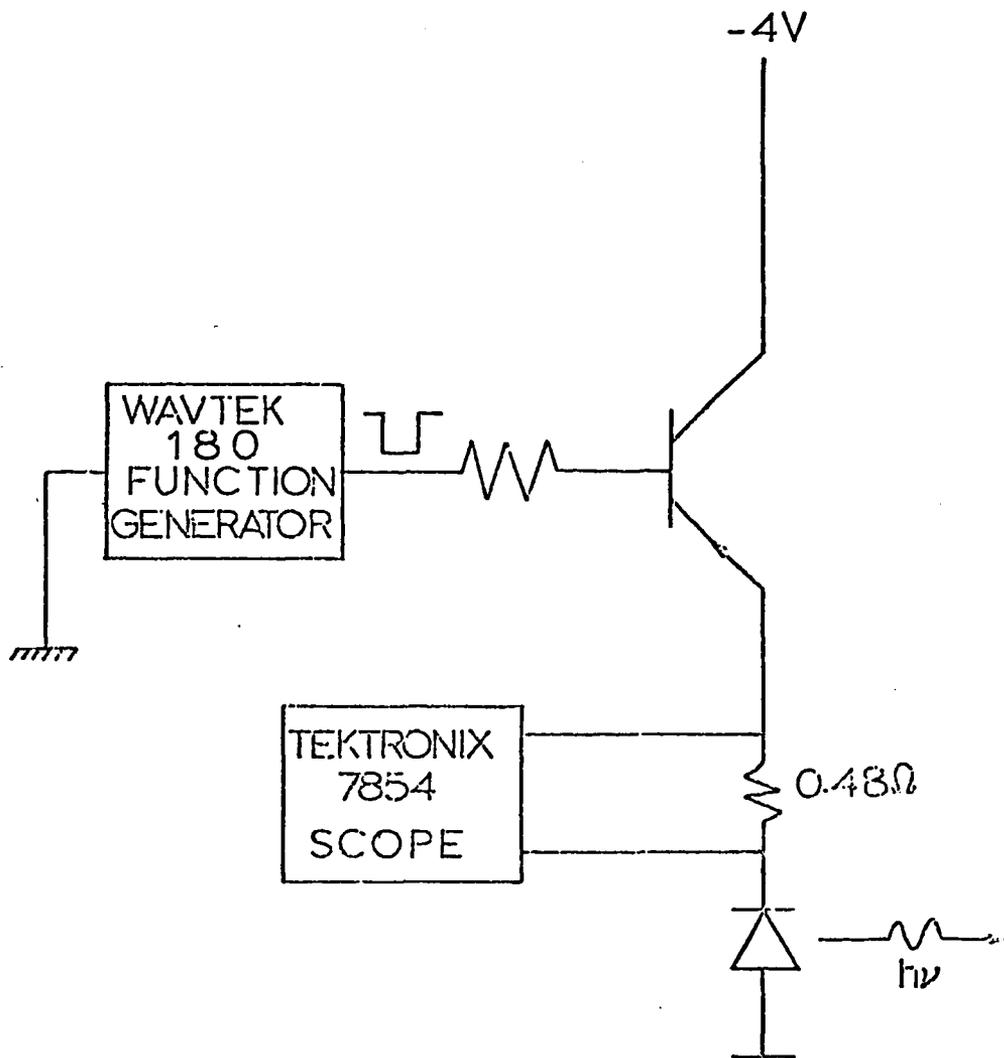


Fig. 18. Circuit used for driving laser.

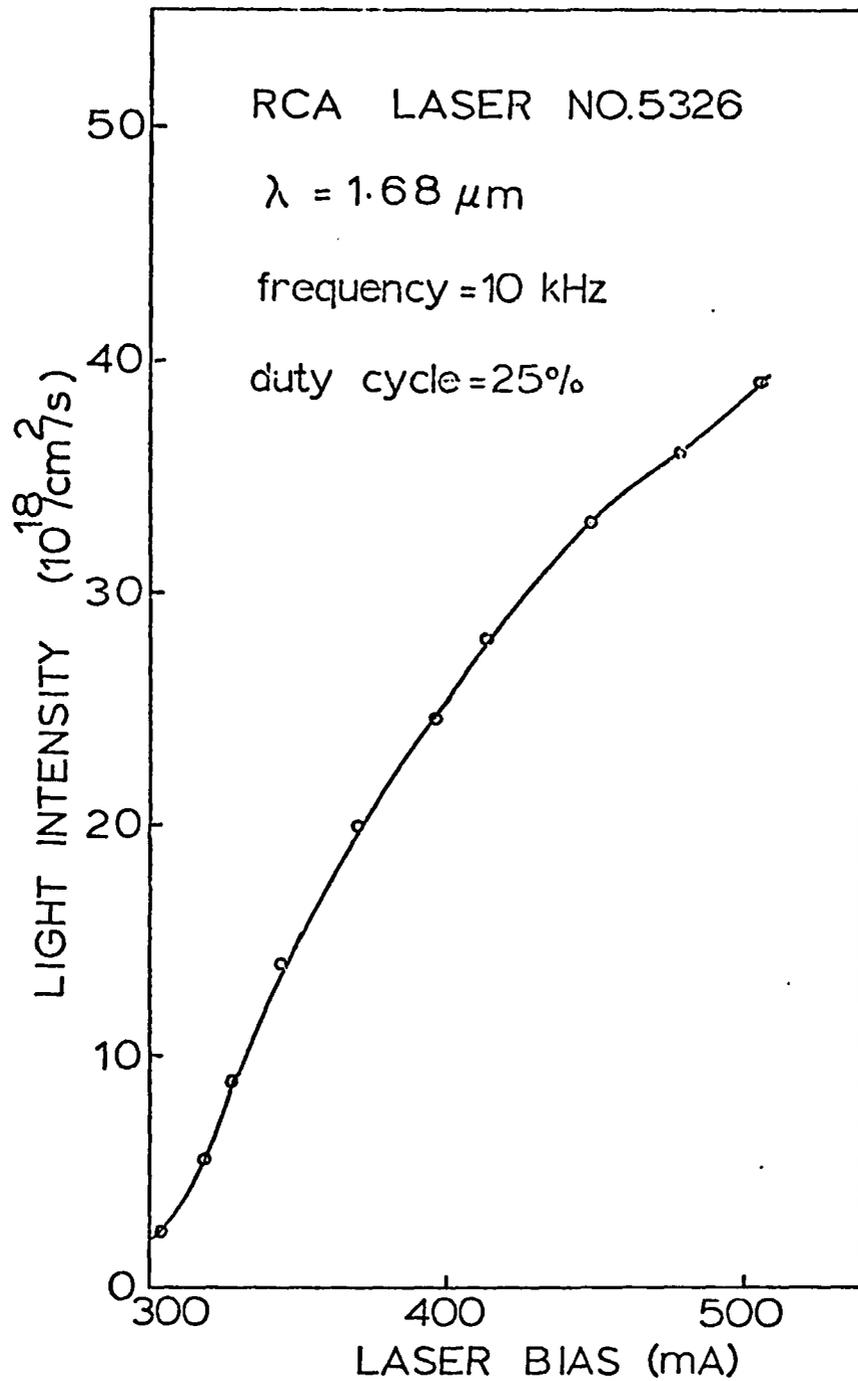


Fig. 19. Output light intensity vs. laser bias current.

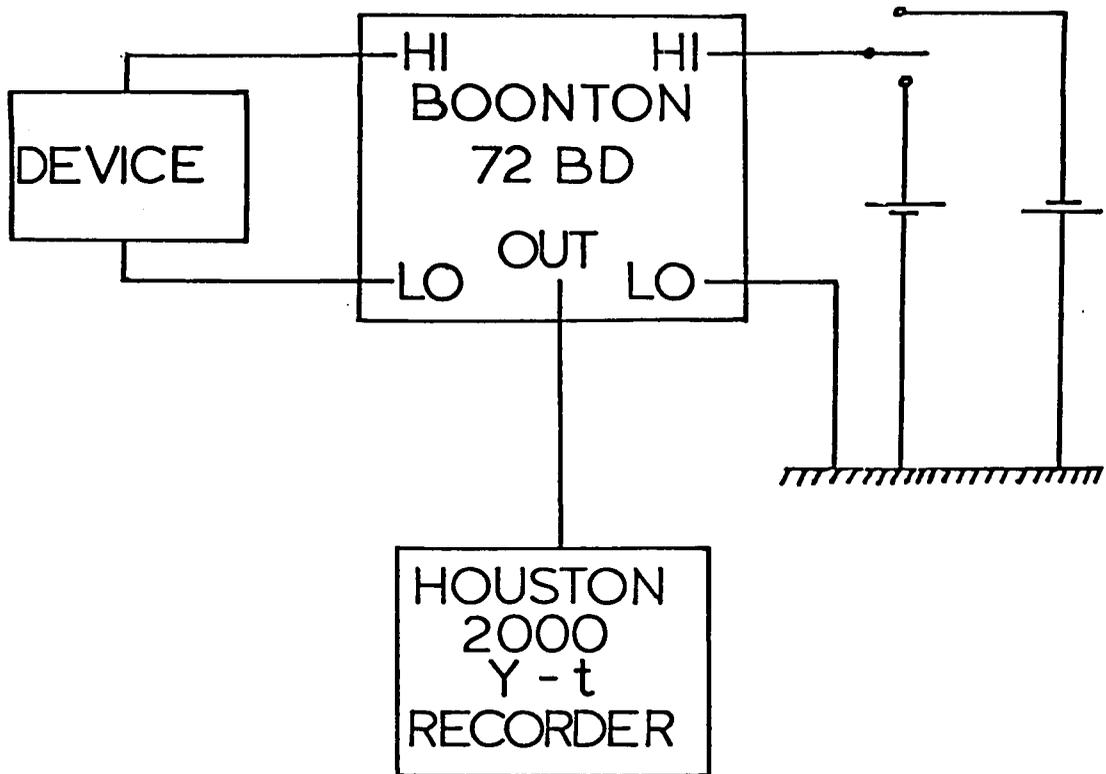


Fig. 20. Circuit used for measuring photocapacitance transients.

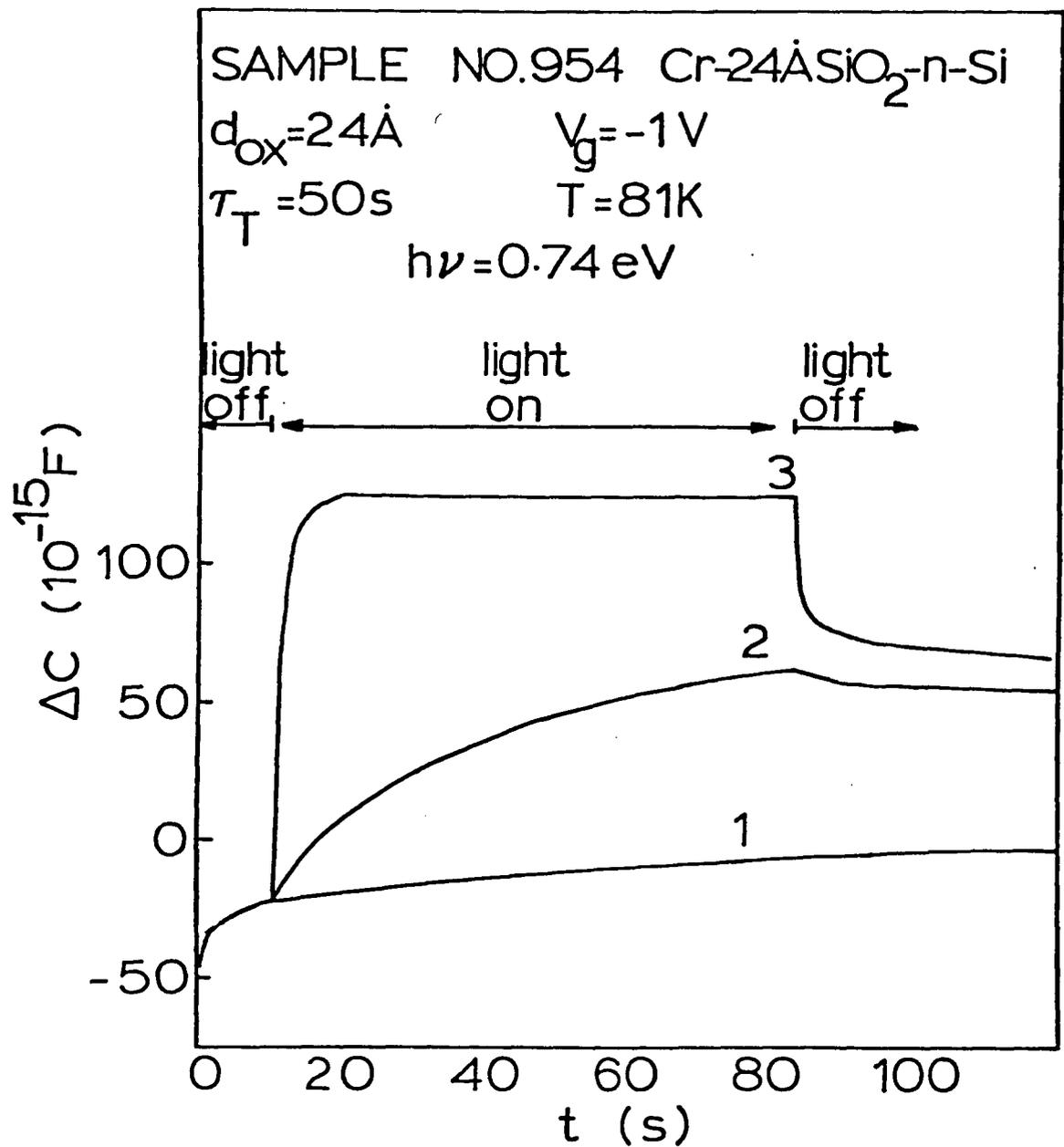


Fig. 21. Photocapacitance transients for 24 Å device.
 Curve 1: in dark; curve 2: at $\phi = 6.10^{16}$
 $\text{cm}^{-2}\text{s}^{-1}$; curve 3: at $\phi = 2.10^{19}$ $\text{cm}^{-2}\text{s}^{-1}$.

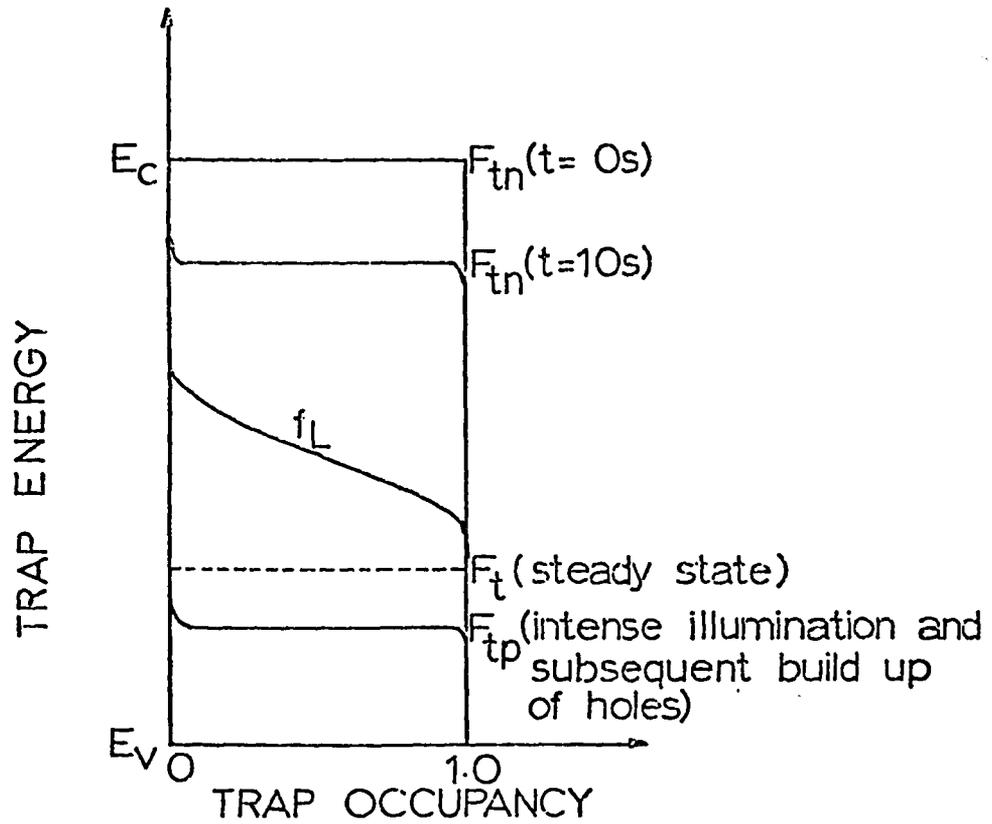


Fig. 22. Trap occupancy vs. trap energy.

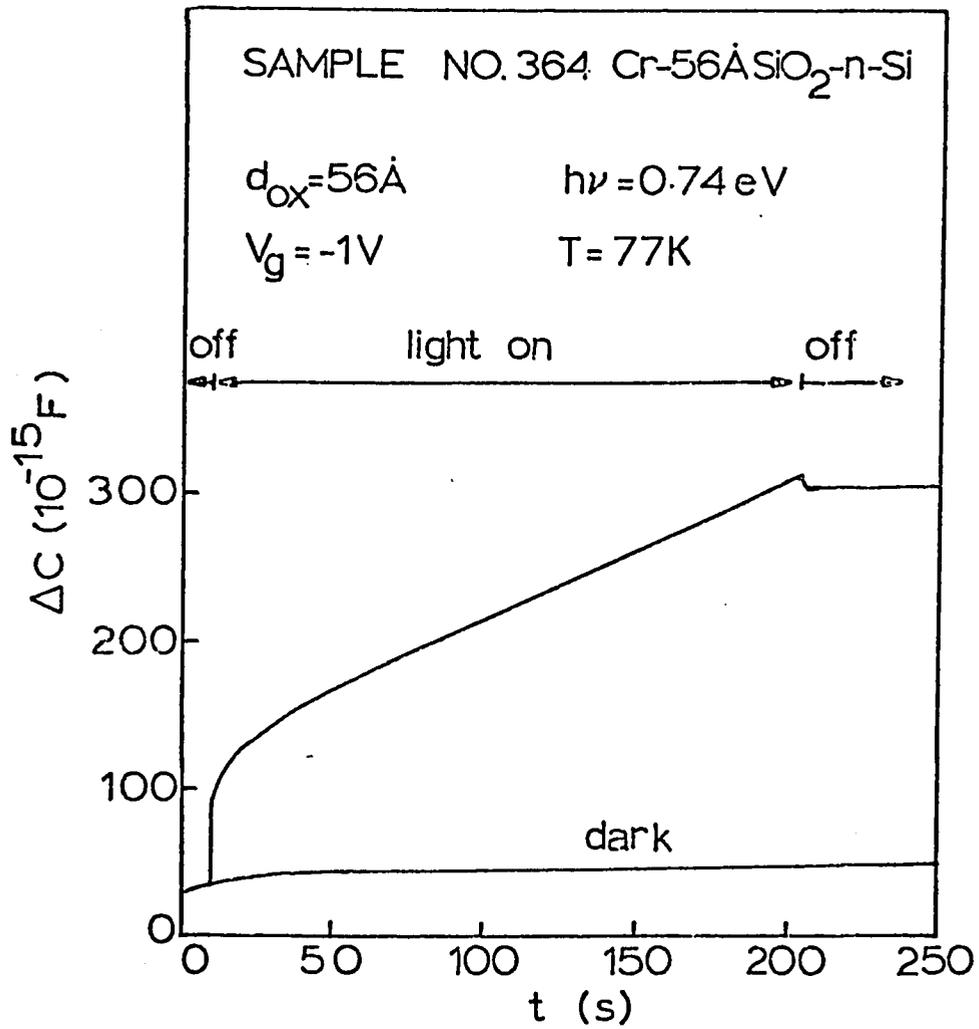


Fig. 23. Photocapacitance transient for 55 Å devices.

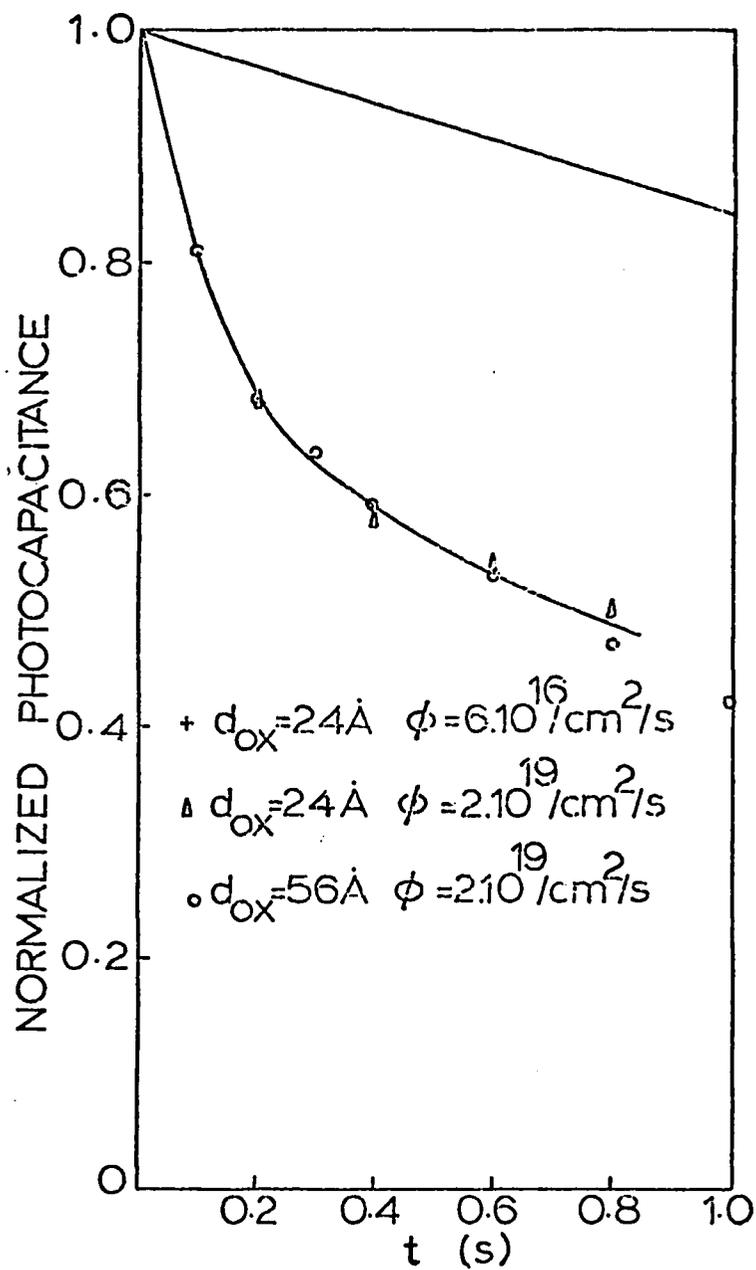


Fig. 24. normalized photocapacitance transients for 24 Å and 55 Å devices.

VITA

Sanjay Jain was born on January 10, 1959, in Agra, India, to Ram Narain Agarwal and Uma Agarwal. He holds the degree of Bachelor of Technology from the Indian Institute of Technology, Kanpur.