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An RTL/TTL compatible CMOS LSI design.

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AN RTL/TTL COMPATIBLE CMOS LSI DESIGN

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ABSTRACT

A CMOS LSI integrated circuit has been designed which can interface with both TTL and RTL logic families. CMOS technology was selected for this circuit, due to its low power dissipation and the wide operational power supply range which is required by the interfacing with both logic families.

The main problem associated with this circuit is the interfacing to the two different logic families. A special programmable input buffer has been designed to handle this interfacing. The analysis, circuit simulation, and characterization are presented. In addition, it is necessary to incorporate into this buffer and in some output buffers, additional circuitry to isolate the chip from the system until chip power has been supplied. This isolation is also discussed here.

I. INTRODUCTION

A single CMOS integrated circuit chip has been designed to replace circuitry previously implemented using small-scale and medium-scale integration. This chip is designed to interface to either of two logic families, RTL logic or TTL logic.

There are two main differences between the RTL and the TTL families. First, both operate using a different power supply range. The RTL power supply ranges from a 3.6V minimum value to a 4.4V maximum value with a nominal voltage of 4.0V. The TTL power supply is nominally 5.0V with a 4.5V minimum and a 5.5V maximum value.

Second, both logic families provide different input voltage levels to the chip. The TTL levels range from 0.8V maximum input low voltage to 1.8V minimum input high voltage. A maximum low voltage of 0.56V and a minimum high voltage of 1.0V is provided to the chip from the RTL family. Therefore the TTL has a voltage margin of 1.0V while the RTL has a voltage margin of 0.44V.

The new chip design uses CMOS Technology. The operating power supply range for CMOS is as low as 2.0V to over 5.5V. Since the chip is to be used in interfacing two logic families, one with a power supply of 4.0V $\pm$ 10%, the other with a supply of 5.0V $\pm$ 10%, operation has to be guaranteed from 3.6V to 5.5V; a range

that is easily handled by CMOS. CMOS is also attractive because of its low power consumption since both applications have strict power requirements. The only power drawn by standard CMOS is dynamic power during switching. Therefore the only DC power consumed by the chip will be that drawn by the linear stages of the buffer.

There are several problems to be considered in the design of this new chip. Since this circuitry is to be used with two logic families, it is desirable to have one chip for either the RTL or the TTL version. Therefore it must be able to interface directly to either TTL or RTL logic. Normally, interfacing to RTL logic is done off chip with discrete devices. It was desirable to do all buffering on chip to eliminate the use of external devices. A special input buffer has been designed to selectively handle the interfacing to either RTL or TTL logic. The design of this buffer including circuit simulation and results are presented.

Another problem to be considered in the design involves how the chip is used in actual practice. Once these chips are mounted on circuit boards along with additional circuitry they are inserted into frames. Usually these boards are plugged directly into an already powered up or "hot" frame. Because of the physical design of the circuit board, which cannot be altered, the connector fingers of the inputs, some outputs, and ground make

connection before the power connector. If any inputs are in the high state without power being connected, input static protection diodes are forward biased, providing pseudo power to the chip. Since CMOS uses little power, this pseudo power is often sufficient to operate the entire chip. Under these conditions static charge or input propagation could allow open collector outputs to draw current from common external bus lines thereby propagating false signals. For these reasons all the inputs and the open collector outputs must be isolated from the external circuitry until full power has been applied to the chip. The design of the isolation circuitry for both inputs and outputs is also discussed here.

II. INPUT BUFFER DESIGN

A special input buffer is needed to perform the interfacing between the incoming RTL or TTL signals and the CMOS logic. RTL logic, with a voltage margin (defined as the span between the maximum low level and the minimum high level) ranging from 0.56V worst case for low input levels to 1.0V worst case for high input levels, does not directly interface to CMOS logic which has a voltage margin of $0.2V_{DD}$ to $0.8V_{DD}$. In the same manner, standard TTL levels, ranging from 0.8V to 1.8V, must also be shifted in order to be compatible to the CMOS logic. Figure 1 shows the voltage margins for the RTL, TTL, and CMOS logic.

Ideally, a single input buffer capable of handling either RTL or TTL inputs is desired. To handle either type of input the buffer would have a small voltage margin ranging from 0.8V to 1.0V. Considering all power supply requirements and variations in the process it is impossible to guarantee this exact margin and still be within the power supply requirements of the two families. The buffer therefore consists of two parallel buffers, one TTL compatible and the other RTL compatible, with an additional signal and its inverse to perform the selection between the two. The design of the RTL buffer is presented in Section A. Section B discusses the TTL

buffer while section C covers the composite buffer with input isolation.

A. RTL Buffer Circuit

1. Input Stage

The RTL portion of the buffer is designed to handle worst case RTL input levels. The buffer consists of two inverting stages for a total non-inverting buffer. Because it is limited to a voltage margin of only 0.44V, the first stage, or the input stage, uses a high gain linear amplifier which performs the necessary amplification around the dc operating point.

A self-biased amplifier was chosen for the input stage and is shown in figure 2. The basic circuit consists of transistors TP1 and TN2 to perform the inversion with TN3 acting as the high resistance feedback path. When the selection lead, labeled B in figure 2, is at a logic high voltage, TN3 is on with a resistance of approximately 800KΩ. Transistor TN1 is also turned on when the selection lead is high. The purpose of this transistor is to provide power to the input stage, in particular TP1 and TN2. When on, TN1 acts as an MOS diode providing a voltage to TP1 that is approximately a threshold down from the chip power supply. Therefore,

$$V_{I1} = V_{DD} - V_{T_{TN1}} \qquad (2.1)$$

By providing a lower voltage, the p-channel transistor, TP1 remains in saturation for a wider range of V_G, thereby allowing the dc operating point of the inverter to be shifted lower than if the chip power supply voltage had been applied at this node.

To provide a switching operation, the amplifier must have its switching point or dc operating point centered midway through the voltage margin. A simplified circuit of the input stage with TN3 replaced by the resistor R is shown in figure 3. This amplifier must therefore be biased as follows,

$$V_{IN} = V_{OUT} = 0.78V \tag{2.2}$$

and

$$(V_{IN} - V_{OUT})/R = I_{DP1} + I_{DN2} \tag{2.3}$$

but since

$$V_{IN} = V_{OUT} \tag{2.4}$$

Therefore,

$$0 = I_{DP1} + I_{DN2} \tag{2.5}$$

therefore,

$$I_{DP1} = -I_{DN2}. \tag{2.6}$$

The equations for the drain currents of the n-channel and the p-channel transistors, I_{DN2} and I_{DP1}, respectively, can be written. For the p-channel load device,

$$I_{DP1} = u_p \frac{W}{L} C_{ox} \left((V_G - \phi_{MS} - \phi_B + \frac{Q_{ox}}{C_{ox}})(V_D - V_S)\right.$$
$$-1/2(V_D^2 - V_S^2) - 2/3 \frac{(2\varepsilon_s q N_D)^{1/2}}{C_{ox}} \left((-(V_D - V_S) - \phi_B)^{3/2}\right.$$
$$\left.\left. - (-(V_S - V_B) - \phi_B)^{3/2}\right)\right) \tag{2.7}$$

where V_G is the gate voltage, ϕ_{ox} is the oxide charge, and C_{ox} is the oxide capacitance. ϕ_B is the potential barrier, or the total bending of the energy bands under strong inversion and is shown in the band diagram of figure 4. It is equal and opposite to twice the fermi potential,

$$\phi_B = -2\phi_F. \tag{2.8}$$

The work function difference ϕ_{MS} and the oxide charge present on the gate cause a bending of the energy bands at the gate. V_{FB} is the voltage needed to cause the

bands to flatten out, known as the flat band condition. The flat band voltage is therefore

$$V_{FG} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}}. \tag{2.9}$$

Substituting these values into equation (2.7);

$$I_{DP1} = u_p \frac{W}{L} C_{ox}((V_G - V_{FB} + 2|\phi_F|)(V_D - V_S) - 1/2\ (V_D^2 - V_S^2) - 2/3 \frac{(2\varepsilon_s qN_D)^{1/2}}{C_{ox}} ((-(V_D - V_B) + 2|\phi_F|)^{3/2} - (-(V_S - V_B + 2|\phi_F|)^{3/2})) \tag{2.10}$$

Further simplifying,

$$I_{DP1} = \mu_p \frac{W}{L} (C_{ox}(V_G - V_{FB} + 2|\phi_F| - 1/2\ V_D - 1/2V_S)(V_D - V_S) - 2/3(2\varepsilon_s qN_D)\ ((-(V_D - V_B) + 2|\phi_F|)^{3/2} - (-(V_S - V_B) + 2|\phi_F|)^{3/2})). \tag{2.11}$$

Similarly, for the n-channel device, the simplified drain current equation is as follows:

$$I_{DN2} = \mu_n \frac{W}{L}(C_{ox}(V_G - V_B - 2|\phi_F| - 1/2V_D - 1/2V_S)(V_D - V_S)$$

$$- 2/3(2\varepsilon_s qN_A)^{1/2}((2|\phi_F| + V_D - V_B)^{3/2}$$

$$- (2|\phi_F| + V_S - V_B)^{3/2})). \qquad (2.12)$$

The simplified equations for the drain currents of the p- and n-channel devices given by equations (2.11) and (2.12) are valid so long as both transistors are under strong inversion where an inversion charge exists across the entire channel. During the transition between the logic levels of a CMOS inverter, however, both the n-channel and the p-channel devices are in saturation, meaning the channels are pinched off. For the n-channel device, the gate voltage, V_G, and the drain voltage, V_D, are increased sufficiently to allow $Q_n(L)$, the charge in the channel at Y=L or next to the drain to go to zero. Therefore,

$$Q_n(L) = 0 = -C_{ox}(V_G - V_{FB} - 2|\phi_F| - V_{D_{sat}})$$

$$+ (2\varepsilon_s qN_A(2|\phi_F| + V_{D_{sat}} - V_B)^{1/2}. \qquad (2.13)$$

Solving for $V_{D_{sat}}$ the saturation drain voltage is

$$V_{D_{sat}} = V_G - V_{FB} - 2|\phi_F| - \frac{\varepsilon_s q N_A}{C_{ox}^3}\left(\left(1 + \frac{2C_{ox}^2}{\varepsilon_s q N_A}(V_G - V_{FB} - V_B)\right)^{1/2} - 1\right). \quad (2.14)$$

Since the oxide thickness, x_o, is small compared to the width of the surface depletion region, $x_{dmax,0}$, where

$$x_{dmax,0} = (2\varepsilon_s(2|\phi_F|)/qN_A)^{1/2} \quad (2.15)$$

$V_{D_{sat}}$ reduces to the following:

$$V_{D_{sat_n}} \cong V_G - V_{FB} - 2|\phi_F|. \quad (2.16)$$

A similar derivation for the p-channel device would produce

$$V_{D_{sat_p}} \cong V_G - V_{FB} + 2|\phi_F|. \quad (2.17)$$

Still under the assumption that $x_o << x_{dmax,0}$ and substituting equations (2.16) and (2.17) into equations (2.12) and (2.11), respectively, the saturation equations for the drain currents are as follows:

$$I_{D_{sat_n}} = \mu_n \frac{W}{2L} C_{ox} V_{D_{sat_n}}^2$$

$$= u_n C_{ox} \frac{W}{2L} (V_G - V_{FB} - 2|\phi_F| - |V_S|)^2 \qquad (2.18)$$

and

$$I_{D_{sat_p}} = \frac{u_p W C_{ox}}{2L} V_{D_{sat_p}}^2$$

$$= u_p C_{ox} \frac{W}{2L} (V_G - V_{FB} + 2|\phi_F| + |V_S|)^2 \qquad (2.19)$$

or further reducing,

$$I_{D_{sat_n}} = \frac{u_n W C_{ox}}{2L} (V_G - V_{T_n})^2 \qquad (2.20)$$

where the threshold voltage is defined as follows:

$$V_{T_n} = V_{FB} + 2|\phi_F| + |V_S| \qquad (2.21)$$

and

$$I_{D_{sat_p}} = \mu_p \frac{W}{2L} C_{ox} (V_G - V_{T_p})^2 \qquad (2.22)$$

where

$$V_{T_p} = V_{FB} - 2|\phi_F| - |V_S|. \qquad (2.23)$$

To bias the first stage as indicated by equation (2.2) it is required to meet the condition stated by equation (2.6). For both transistors in saturation,

$$I_{D_{sat_{p1}}} = I_{D_{sat_{n2}}} \tag{2.24}$$

$$u_p \frac{C_{ox}W}{2L} (V_G - V_{T_p})^2 = u_n \frac{C_{ox}W}{2L} (V_G - V_{T_n})^2. \tag{2.25}$$

Defining the betas of the two transistors,

$$\beta_{p1} = u_p \frac{C_{ox}W_{p1}}{L_{p1}} \tag{2.26}$$

and

$$\beta_{n2} = u_n \frac{C_{ox}W_{n2}}{L_{n2}} \tag{2.27}$$

then,

$$\frac{\beta_{p1}}{2} (V_G - V_{T_p})^2 = \frac{\beta_{n2}}{2} (V_G - V_{T_n})^2 \tag{2.28}$$

From the relationship of equation (2.28), the beta ratio of TP1 and TN2 can be found. Solving,

$$\beta_R = \frac{\beta_{n2}}{\beta_{p1}} = \frac{(V_G - V_{T_p})^2}{(V_G - V_{T_n})^2} \tag{2.29}$$

From the above equation and using V_G = 0.78V, the desired switching point, the geometries of the p-channel and the n-channel devices are chosen. Computer simulations of the first stage were done varying the geometries of transistors TP1 and TN2 to optimize this stage so that the operating point was well centered around 0.78V over the entire range of processing and environmental variations. The final geometries and threshold voltages for these two transistors are found in Table 1.

2. Second Stage

The second stage of the RTL buffer is shown in figure 5. This stage also uses a linear self-biased amplifier. The transient characteristics for the first stage, such as rise and fall times, are slow due to the low beta ratio necessary to perform the shifting of the dc operating point to 0.78V. The linear configuration of the second stage has a higher gain than the normal CMOS inverter therefore making the switching speeds of the complete buffer faster.

The selection lead B, as shown in figure 5, turns transistor TN4 on, again providing a high resistance feedback path to the input of this stage. Transistors TP2 and TN5 perform the inverting operation.

Equation (2.29) is used for the second stage to determine the geometries for TP2 and TN5 necessary to

provide the desired switching point of V_G=2.0V, midway through the voltage margin. Optimization of these geometries is achieved through computer simulation with the results shown in Table 1.

3. Composite RTL Buffer

The composite RTL buffer is shown in figure 6. The two stages, as discussed in sections A.1 and A.2, are used with one additional transistor, TN6, which is part of the selection circuitry.

The selection of the RTL buffer is done by two leads, B and C, where B is the inverse of C. To select the RTL buffer, lead C must be set at a logic low level therefore forcing lead B to reach a logic high voltage. Transistors TN1, TN3, and TN4 are turned on, enabling both stages for operation. Transistor TN6 is off, therefore not effecting operation of the buffer.

When the TTL buffer is selected and the RTL portion is not the C lead is tied high while the B lead is low. This state turns TN3, TN4, and TN1 off and TN6 on. Turning off TN1 and TN3 completely disables the first stage of the RTL buffer while turning off TN4 disables the second stage. With these stages turned off the RTL buffer should not draw any dc power. Yet this does not insure zero power consumption. There is still the risk that node I2 is at an indeterminate state known as floating. This floating state could possibly turn on

both TP2 and TN5, providing a direct path from the power supply to ground through these transistors. Node I2 is kept from floating through the use of transistor TN6. When the RTL buffer is off TN6 is on drawing node I2 low. This turns TN5 off and TP2 on. The output Z1 is forced high but still no dc power is drawn. With the output Z1 high, the RTL and the TTL outputs can be combined into a common node through a 2-input and gate.

B. TTL Buffer Circuit

1. Basic Buffer

The TTL portion of the buffer is designed to handle the worst case TTL input levels. These range from 0.8V maximum low level to 1.8V minimum high level. Since this buffer is in parallel with the RTL buffer it must be non-inverting, therefore it also has two stages. The basic TTL buffer circuit is shown in figure 7. The configuration of this buffer is one of an existing TTL buffer. The design of this buffer involved scaling the transistor sizes to minimize the area of the buffer and to decrease the power drawn in operation.

The switching point of the TTL buffer should also be midway through the voltage margin, approximately 1.3V. Since the normal switching point of CMOS is 2.0V, something must be done to shift this point lower. In comparison with the RTL signal, the TTL buffer has a total swing of 1.0V and does not require a linear input stage.

Only a normal inverting stage with its operating point lowered is needed. As in the RTL buffer the operating point can be lowered by decreasing the power supplied to the inverter. Power is supplied to the source of the p-channel load transistor, TP3, in figure 7, through a diode, transistor TP4. The voltage at node I3 is

$$V_{I3} = V_{DD} - |V_{T_{p4}}| \tag{2.30}$$

In this configuration the gate of the diode formed by transistor TP4 is tied to the drain at node I3. Once node I3 reaches a high voltage level, it shuts off, storing the high level at node I3.

As in the RTL buffer the switching point occurs at a point where both TP3 and TN7 are in saturation. At the switching point the two drain currents are equal, or,

$$-I_{D_{p3}} = I_{D_{n7}} \tag{2.31}$$

The equations for the p-channel drain current and the n-channel drain current are found in equations (2.22) and (2.20), respectively. Equating these two equations and reducing, as in section 2, an equation similar to that of (2.29) is found,

$$\beta_R = \frac{\beta_{n7}}{\beta_{p3}} = \frac{(V_G - V_{T_p})^2}{(V_G - V_{T_n})^2} \qquad (2.32)$$

This equation is used to determine the transistor sizes needed to produce the desired switching point. The optimized values of the transistor sizes for this stage are found by computer simulation and are summarized in Table 1. DC power is consumed since the devices are biased in the linear region. Therefore, the device sizes are kept small to decrease this power without significantly decreasing the speed of operation.

The second stage serves the purpose of equalizing the inversion between the RTL buffer and the TTL buffer. It is a single CMOS compatible inverter with an operating point of approximately 2.0V. The sizes used in this stage are also summarized in Table 1.

The operation of this buffer is as follows. When the input at node A is high, transistor TP3 is off and TN7 is on, drawing the voltage on node I4 low. With I4 low, the second stage performs an inversion pulling node Z2 high to a good CMOS level through TP5. When the input at A is low, transistors TP4 and TP3 are on forcing a high voltage at node I4 while TN7 is off. The high on node I4 turns on TN8, drawing Z2 low.

2. Composite TTL Buffer

The composite TTL buffer with selection is shown in figure 8. The basic buffer, consisting of transistors TP4, TP3, TN7, TP5, and TN8, is as described in section B.1. Transistors TN9, TP6, TN10, and TN11 are for the selection between this buffer portion and the previously discussed RTL portion. The purpose of selection is two-fold. First and most important, when the buffer is selected it must transmit the input signal through to its output and when it is not selected it must force the output to a high voltage. Second, it must inhibit current flow, or dc power consumption, when the circuit is disabled. This selection is now discussed.

When this buffer is selected lead C is at a high voltage and its inverse, B, is low. This combination turns TN9, TP6, and TN10 on while turning TN11 off. The transistor pair of TN9 and TP6 form a transmission gate which, when enabled by turning both transistors on, allows the output from the first stage to propagate to the input of the second stage. In this state TN10 provides a path from the driver devices of both stages to ground, allowing them to be able to pull their output stages low if the input so dictates. Therefore, with the transistors in the mentioned selection states, the buffer is completely operational.

Lead C low and B high selects the RTL circuit, disabling the TTL portion. Leads C and B in this state turn TN9, TP6, and TN10 off while turning on TN11. When the transmission gate pair of TN9 and TP6 is off no data can be transmitted from the first stage to the second stage. With the transmission gate off there is the chance of node I5 being left in a floating state. Again it is possible that the floating state will allow both TP5 and TN8 to be on letting a floating voltage propagate to the output of the buffer. If the second stage of the buffer is floating it will be drawing current through both devices to ground for as long as the buffer is in this state, an indefinate amount of time. This would increase the amount of power being dissipated by the entire chip. Transistors TN11 eliminates this problem by drawing node I5 to a solid low level, thereby insuring a high voltage at the output.

C. Combined RTL/TTL Buffer

1. Implementation

The RTL compatible circuitry and the TTL compatible circuitry discussed in sections II.A and II.B respectively are combined into a single input buffer configuration to be used on the chip. The composite buffer consists of the two self-contained RTL and TTL buffers, two common selection leads, B and C, a common pad with input protection and isolation, and two output leads, one from

the RTL buffer and one from the TTL buffer. These outputs can be combined into one signal through the use of a NAND gate as shown in figure 9, the block diagram of the buffer. The logical equivalent circuit is shown in figure 10.

The input circuitry for the buffer consists of the input pad, the static input protection, and isolation circuitry to keep the input signal from propagating to the buffer before the power is suppliied to the chip. Figure 11 shows the pad with the protection and isolation of the buffer. Standard CMOS input protection consists of the resistor RIN and the diodes D1 and D2. If the input is raised to a voltage higher than the power supply then diode D1 is forward biased limiting the voltage at node A to the voltage of the power supply. Should the input signal at the pad be drawn to a negative voltage D2 is forward biased, protecting any gate connected to a node A from any high negative spikes at the input.

The input signal is isolated from the buffer circuitry by transistor TNI. This transistor acts as a transmission gate which is turned on by the voltage on the power bus. Before power is applied to the chip TNI will be turned off, isolating the internal buffer from the signal on the pad. Once power is supplied TNI is turned on allowing any signal applied to the pad to

propagate to the buffer. In order for this isolation scheme to perform properly a high value resistor of approximately 1MΩ must be connected from the external power lead to ground to drain off any static charge stored on the chip power bus before the actual power has been supplied. Transistor TNI is protected from static discharge by field oxide transistor TNP. This protection device is an n-channel device designed by Jack Keller of Bell Telephone Laboratories in Allentown, Pennsylvania and has a breakdown voltage of approximately 15V.

2. Circuit Simulation

The combined RTL/TTL buffer was simulated using SPICE. The RTL circuit and the TTL circuit were simulated separately through the use of the selection leads B and C. The following parameters were incorporated into the simulations.

RTL PARAMETERS

1.	Temperature range 0 to 85	°C
2.	Voltage Supply 4.0 ± 10%	Volts
3.	Threshold Voltage Variation ±0.3	Volts
4.	Input Voltage Level	
	Vil 0 to 0.56	Volts
	Vih 1.0 to Vdd at 3.6V 85°C	Volts
	1.12 to Vdd at 3.6V 0°C	Volts
5.	Selection C='0' B='1'	Logic Values

TTL PARAMETERS

1.	Temperature range -40 to 85		°C
2.	Voltage 5.0 ± 10%		Volts
3.	Threshold Voltage Variation ±0.3		Volts
4.	Input Voltage Levels	Vil 0 to 0.8	Volts
		Vih 1.8 to Vdd	Volts
5.	Selection C='1' B='0'		Logic Values

In performing computer simulations on the buffer a performance window is used to set the design region of parameter and processing variations. The four worst corners of operation of the buffer over variations in process and parameters are defined in figure 12. Simulation over these four corners as well as nominal operation should be sufficient to insure proper operation of the buffer over all variations in parameters and processing.

A variety of simulations was done to verify the operation of the buffer. The DC operating point of both the RTL and the TTL portions were simulated over the full range of power supplies, temperature, and processing variation. Examples of nominal transfer characteristics for nominal power supplies over a variety of temperatures are shown for the RTL and TTL buffers in figures 13 and 14, respectively. Transient responses of the buffer were also simulated over the full design window. The switching capabilities and propagation delays over the design range

were verified through these simulations. RTL and TTL transient responses with a capacitive loading of 5pf are shown in figures 15 and 16. Additional simulation results can be found in section III where simulations are compared to actual results.

3. Layout

The layout of the buffer was done using an interactive layout aid. The main consideration in the layout was to minimize the size of the overall buffer. Since the buffer is located along side the pad, the size of the buffer influences the area needed for the pads surrounding the internal circuitry. If the buffers are large they may make the chip pad limited, meaning that the overall chip size is dictated by the area necessary to place the pads around the perimeter. The result of this would be a large chip with a significant amount of inactive and therefore wasted space.

The second reason for minimizing the size of the buffer is to decrease the internal resistance and the capacitance of the buffer circuit. This is an important factor in determining the speed of the buffer.

The final layout of the composite buffer is shown in figure 17. This diagram shows the gate, source and drain areas, as well as the interconnections.

III. OUTPUT ISOLATION

As mentioned in section I, because of the manner in which the circuit boards are placed into the main frames it is necessary to isolate certain outputs from the external circuitry until chip power has been supplied. The outputs that need this isolation are those that go to common data busses. On this chip there are three such outputs, all which interface to the bus through open drain output buffers. A special open drain output buffer was designed to interface to the bus with the isolation built into the circuitry. This buffer is shown in figure 18 with the device geometries summarized in table 1.

Although the design of this buffer will not be discussed, a look at its operation with regard to the isolation is appropriate. The inverter formed by transistors TN12 and TP7 is a buffering stage for TN13. Transistor TN13 is the open drain output and acts only as a pull down device. Since the requirement of this buffer is a maximum output low voltage of 0.25V, TN13 is a wide device. The device which handles isolation is transistor TN14. When power has not yet been supplied to the chip TN14 will be turned off. Any static charge stored on node I2 that would normally turn TN13 on has no effect on the output of the buffer since TN14 has inhibited any sinking of current from the output to ground. Once

power is provided to the chip, TN14 is turned on, now providing a path to ground. Since the buffer has such a low output voltage reuqirement it is necessary to have TN14 be transparent to the buffer operation once power has been provided. It must have a small resistance in order to insure a low output voltage below 0.25V. For this reason TN14 was designed with a wide gate to decrease the resistive path to ground.

The layout of the buffer was done with the use of an interactive layout aid. This layout is shown in figure 19. During layout it was found that transistor TN14 was too large to place all in one area next to the pad. Therefore it was divided into two parallel devices. By dividing it into two parts and placing the additional part below the main buffer the width of the overall buffer is decreased thereby not increasing the overall size of the chip.

IV. RESULTS

A. Measurements

The RTL/TTL buffer is used for eight inputs on the LSI chip. All measurements were taken on these inputs from wafers processed the same except for a P-tub implant variation of $0.6x10^{13}$, $0.8x10^{13}$, $1.0x10^{13}$ to provide variation in the p-type substrate resistance. This variation in implant was done only as a processing test, not for design verification.

On the RTL buffer the desired switching point is 0.78V. The measured value for the $0.6x10^{13}$ implant ranges from 0.74V at 3.6V VDD to 0.98V at 4.4V VDD. The $0.8x10^{13}$ implanted wafer ranges from 0.78V to 0.98V over the full power supply range while the $1.0x10^{13}$ wafer ranges from 0.84V to 1.15V.

The TTL buffer was designed to have a switching point of 1.3V. The measured values for the $0.6x10^{13}$ wafer range from 1.38V at 4.5V to 1.68V at 5.5V. The $0.8x10^{13}$ implanted wafer measured from 1.28V to 1.62V and the $1.0x10^{13}$ wafer measured from 1.09V to 1.76V over the supply range. The results for the RTL and the TTL buffer sections are summarized in Table 2.

In addition to the results summarized above, which were found through manual probing, testing of the entire chip was performed using a Fairchild Sentry test set. This testing included exercising the buffer at the worse

case input levels at both 25°C and 85°C. This additional verification proved that all design parameters were met by the processing insuring operation of the buffer. More results of this testing can be found in Section B.

B. Characterization

Both the RTL and the TTL buffer circuits are characterized from simulated and measured results. This characterization includes ranges of DC operating point voltages, propagation delay as a function of capacitive loading, maximum input frequency, and DC power dissipation.

The range of DC operating points determine what the acceptable input voltage levels will be. The simulated results for the RTL and the TTL portions are found in figures 20 and 22, respectively while the measured results are found in figures 21 and 23. As a result of these values a summary of acceptable input levels is given in Table 3.

Propagation delay as a function of capacitive loading for the RTL and the TTL portions are shown in figures 24 through 27. These values are the results of worst case input levels and were measured at the 50% rise or fall point. The simulated values represent the worst case slow and worst case fast ends of operation at 25°C. The measured values fall within the ranges that were predicted by the simulations.

The maximum frequency of operation was measured with an input signal of worst case levels and a 50% duty cycle. This maximum frequency was measured when the signal output from the buffer no longer met standard CMOS logic levels. These values were measured at the low power supplies for the RTL and the TTL buffer and are summarized in table 3.

As mentioned previously, the only DC power drawn by these buffers is due to the linear input stages. The worst case power is drawn when worst case inputs are applied to these buffers. The results of applying these conditions with regard to the worst case power dissipation for the buffer can be found in table 3.

V. CONCLUSIONS

The purpose of this design was to produce an input buffer that would provide an interface from RTL or TTL logic to CMOS logic. Two separate buffers, one RTL compatible and the other TTL compatible, were designed with one lead and its inverse providing selection between the two.

The design of each buffer was handled separately. The RTL buffer required linear amplification stages to shift the logic swing to the desired levels. The overall buffer is non-inverting and each of the two stages were designed separately. The worst case acceptable levels for this portion of the buffer range from 0.56V maximum low input to 1.0V minimum high input. The RTL buffer has a worst case power dissipation of 0.86mW at 3.6V power supply and at 85°C.

The design of the TTL portion of the buffer did not require linear stages but did require a level shifting diode to provide power to the first stage of two. The resulting buffer is capable of handling standard worst case TTL input levels of 0.8V maximum input low to 1.8V minimum input high level. Power dissipation of this portion of the buffer is also low at 0.43mW at 4.5V power supply and 85°C.

Measurements made on fabricated wafers show both the RTL and the TTL portions operate as predicted in the

design. The worst case input levels are accepted with still some margin built in. Also verified by testing was the reliability of the input and output isolation. Without power connected to the power bus no input high voltages are able to leak onto the bus and provide power to the chip. As a result the open drain output buffers are unable to sink current off the external bus until power has been applied.

The need for these buffers in CMOS LSI design is apparent. Most CMOS buffers must be capable of interfacing to TTL, one of the most commonly used logic families. In the case of the RTL, a buffer is needed to interface to this family since it is expensive to provide discrete off-chip circuitry to provide this interface. Custom LSI should be able to incorporate any necessary interface logic on-chip to further reduce the number of components needed to operate the chip. This buffer is capable of providing this interface in either case.

TABLE 1

Transistor Sizes and Threshold Voltages

Device Name	Defect Size W/L ($\frac{\mu m}{\mu m}$)	Threshold Voltage
N-Channel:		
TN1	380/6	0.6V ± 0.3V
TN2	550/6	0.6V ± 0.3V
TN3	6/200	0.6V ± 0.3V
TN4	6/200	0.6V ± 0.3V
TN5	25.5/6	0.6V ± 0.3V
TN6	6/6	0.6V ± 0.3V
TN7	27/6	0.6V ± 0.3V
TN8	51/6	0.6V ± 0.3V
TN9	25.5/6	0.6V ± 0.3V
TN10	1500/6	0.6V ± 0.3V
TN11	6/6	0.6V ± 0.3V
TNI	100/6	0.6V ± 0.3V
TN12	150/6	0.6V ± 0.3V
TN13	1000/6	0.6V ± 0.3V
TN14	5000/6	0.6V ± 0.3V
P-Channel:		
TP1	75.5/6	-0.6V ± 0.3V
TP2	52.5/6	-0.6V ± 0.3V
TP3	65.0/6	-0.6V ± 0.3V
TP4	65.0/6	-0.6V ± 0.3V
TP5	60.5/6	-0.6V ± 0.3V
TP6	52.5/6	-0.6V ± 0.3V
TP7	300/6	-0.6V ± 0.3V

TABLE 2

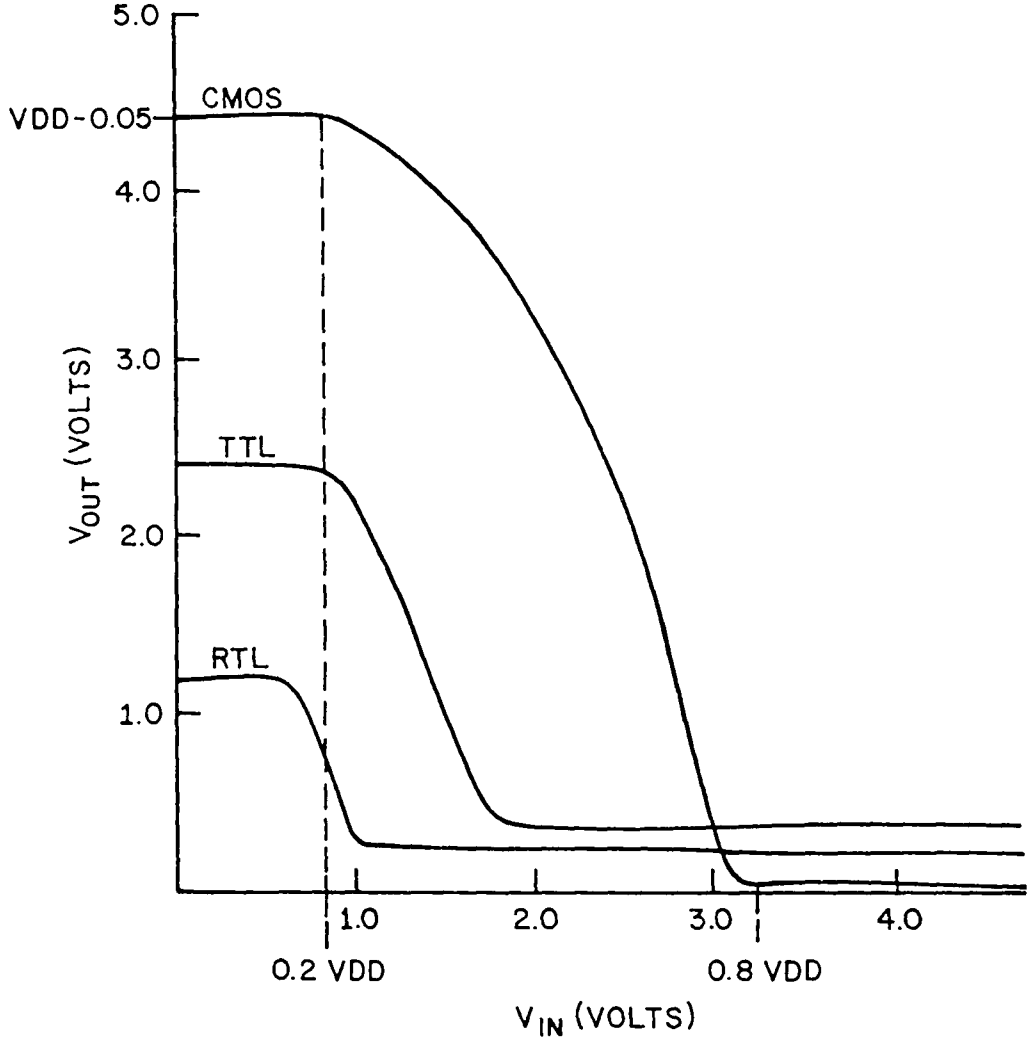
Circuit Implementation

P-Substrate Doping	Threshold Voltages N-Channel	P-Channel	DC Switching Point RTL	TTL
0.6×10^{13} cm^{-3}	0.56V	-0.68V	0.79V @ V_{DD} = 3.6V	1.36V @ V_{DD} = 4.5V
0.8×10^{13} cm^{-3}	0.62V	-0.68V	0.80V @ V_{DD} = 3.6V	1.32V @ V_{DD} = 4.5
1.0×10^{13} cm^{-3}	0.77V	-0.67V	0.84V @ V_{DD} = 3.6V	1.36V @ V_{DD} = 4.5

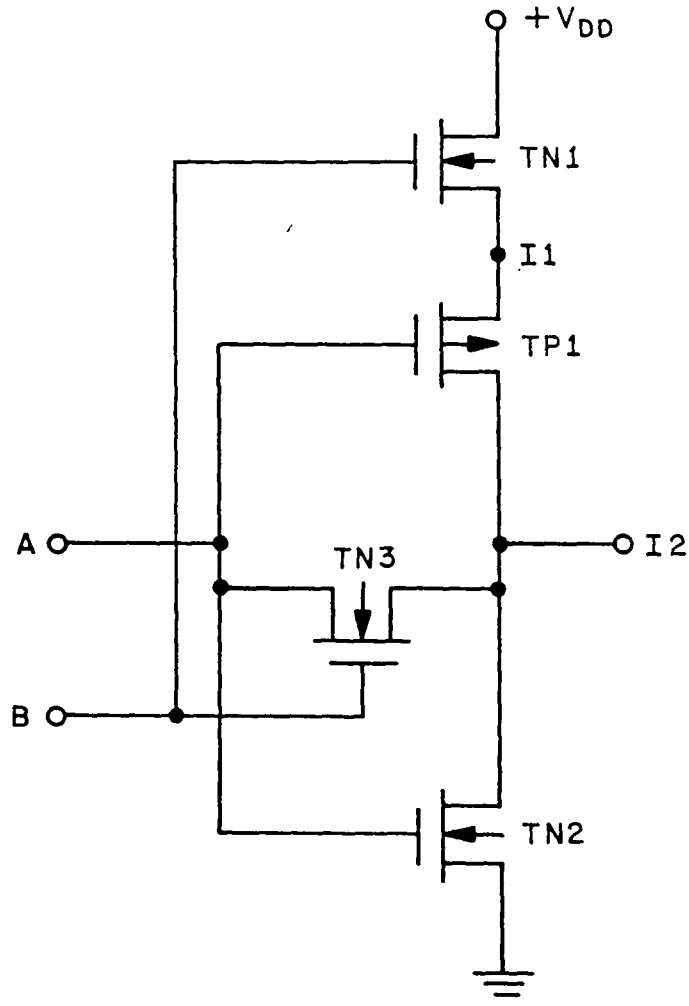
TABLE 3

Buffer Characterization Summary

	RTL	TTL
Input Levels:		
Vil, max.	0.56V @ 3.6V 0°C - 85°C	0.8V @ 5.0V ± 10% -40°C - 85°C
Vih, min.	1.12V @ 3.6V °C 1.2V @ 4.0 - 4.4V 0°C - 85°C	1.8V @ 5.0V ± 10% 1.8V @ 5.0V ± 10% -40°C - 85°C
Propagation Delay:		
t_{plh}	See Figure 23	See Figure 25
t_{phl}	See Figure 24	See Figures 26
Maximum Input Frequency Measured	850 KHz @ 3.6V	1.1 MHz @ 4.5V
Power Dissipation	0.86 mW @ 85°C V_{DD} = 3.6V	0.43 mW @ 85°C V_{DD} = 4.5V

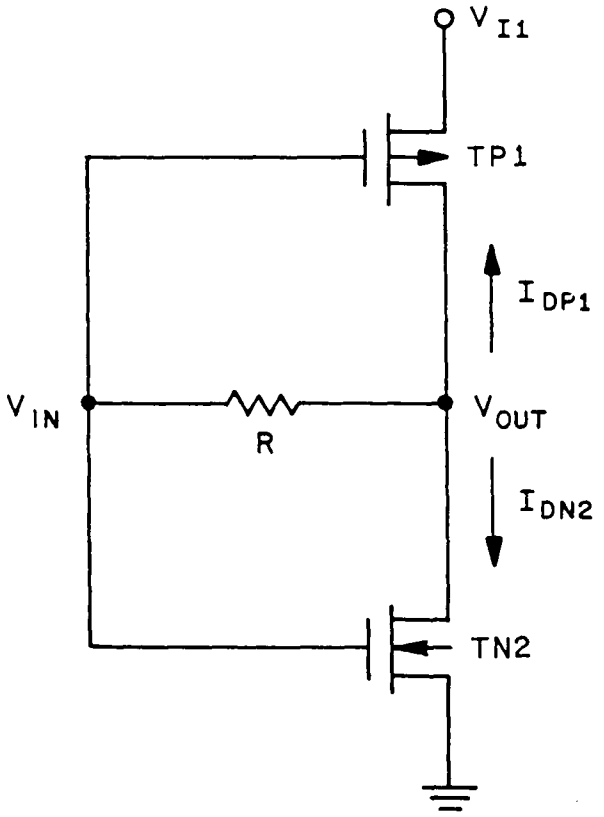


COMPARATIVE NOISE MARGINS
FIGURE 1



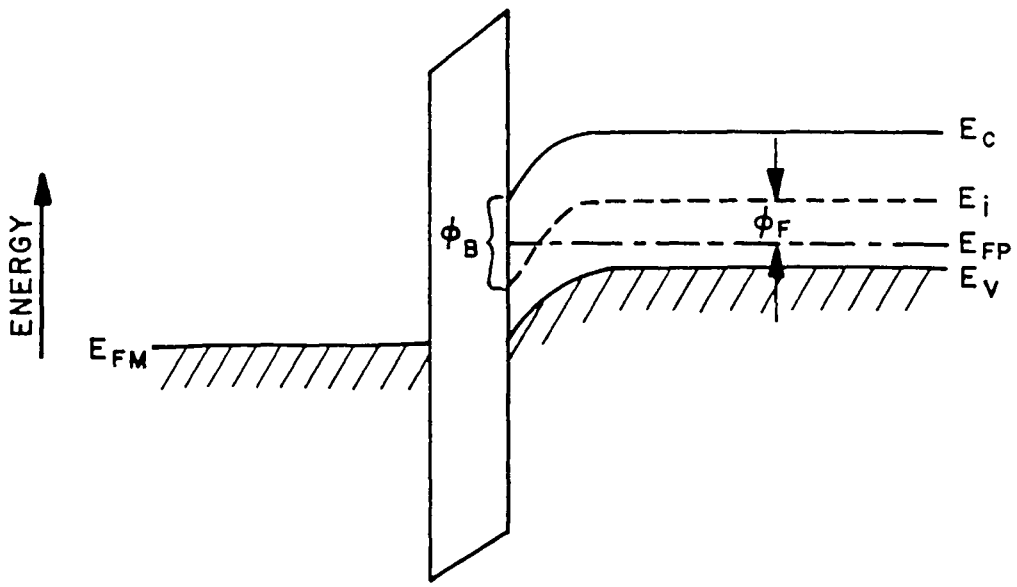
1ST LINEAR STAGE
RTL BUFFER

FIGURE 2



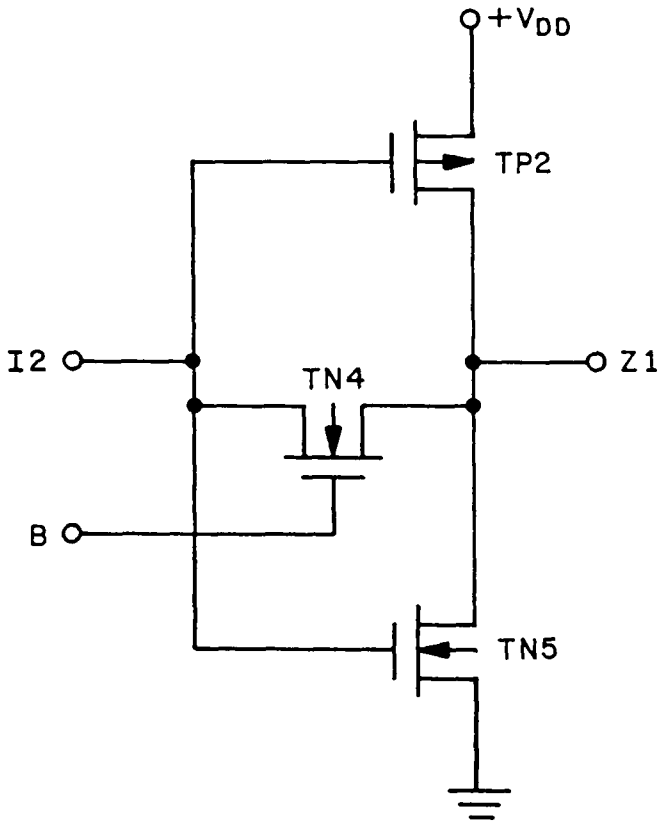
SIMPLIFIED RTL INPUT STAGE

FIGURE 3



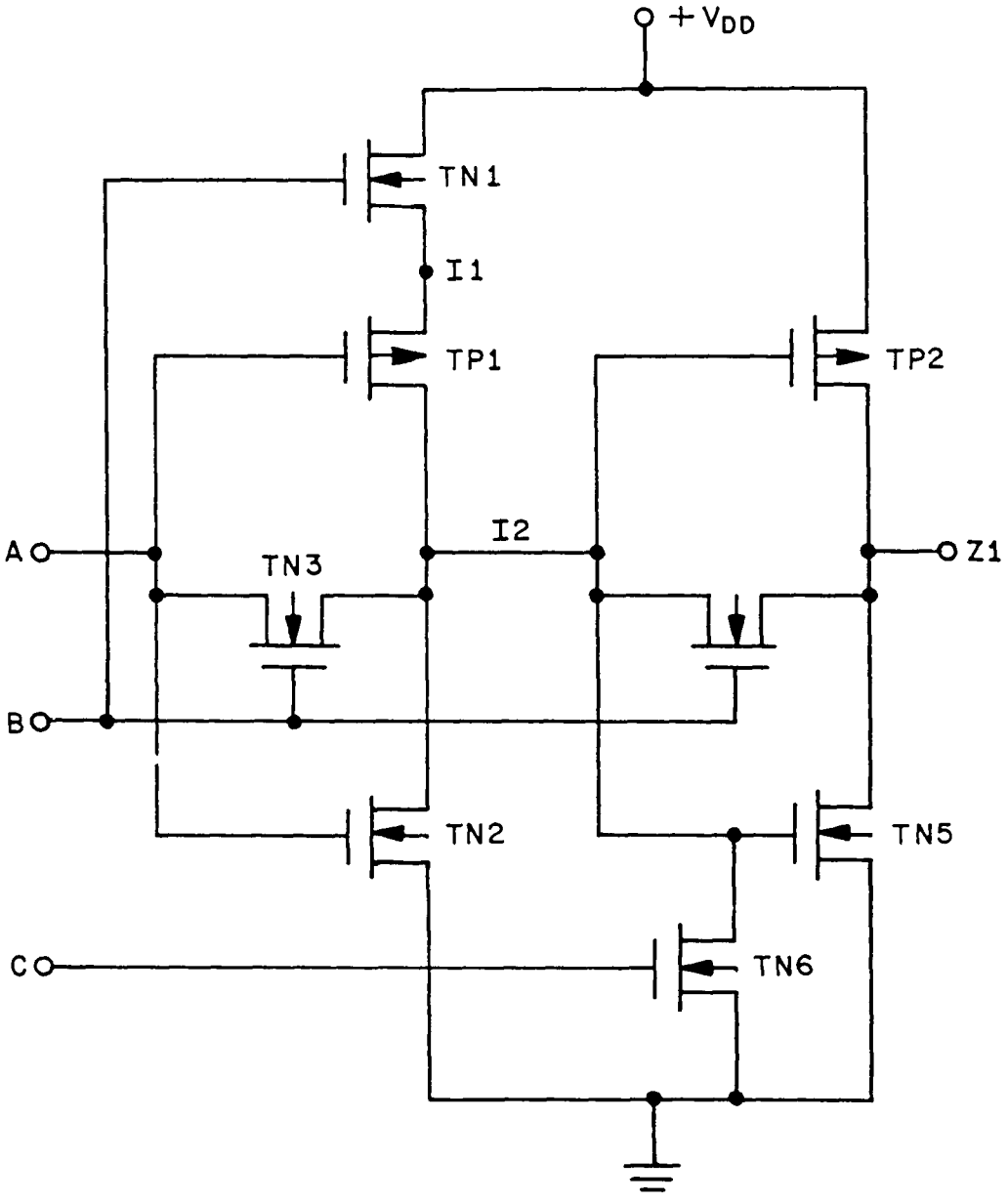
ENERGY BAND DIAGRAM–STRONG INVERSION
P-TYPE

FIGURE 4



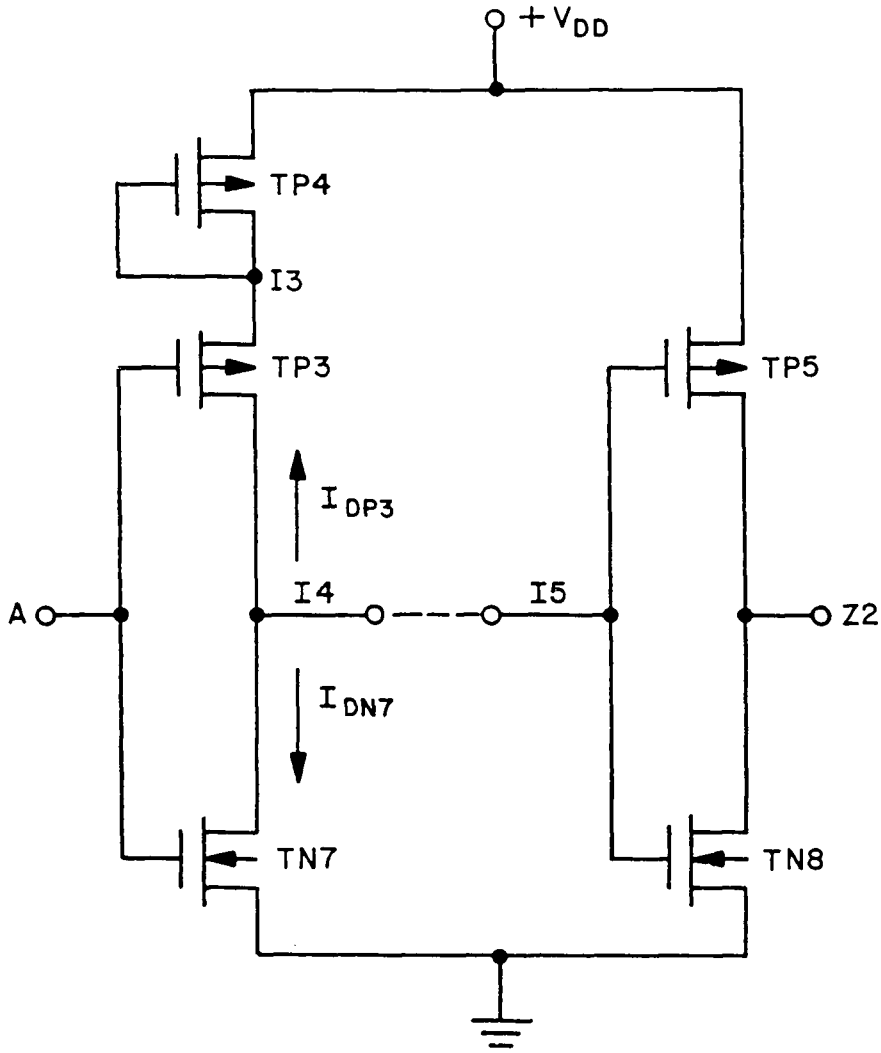
2ND LINEAR STAGE
RTL BUFFER

FIGURE 5



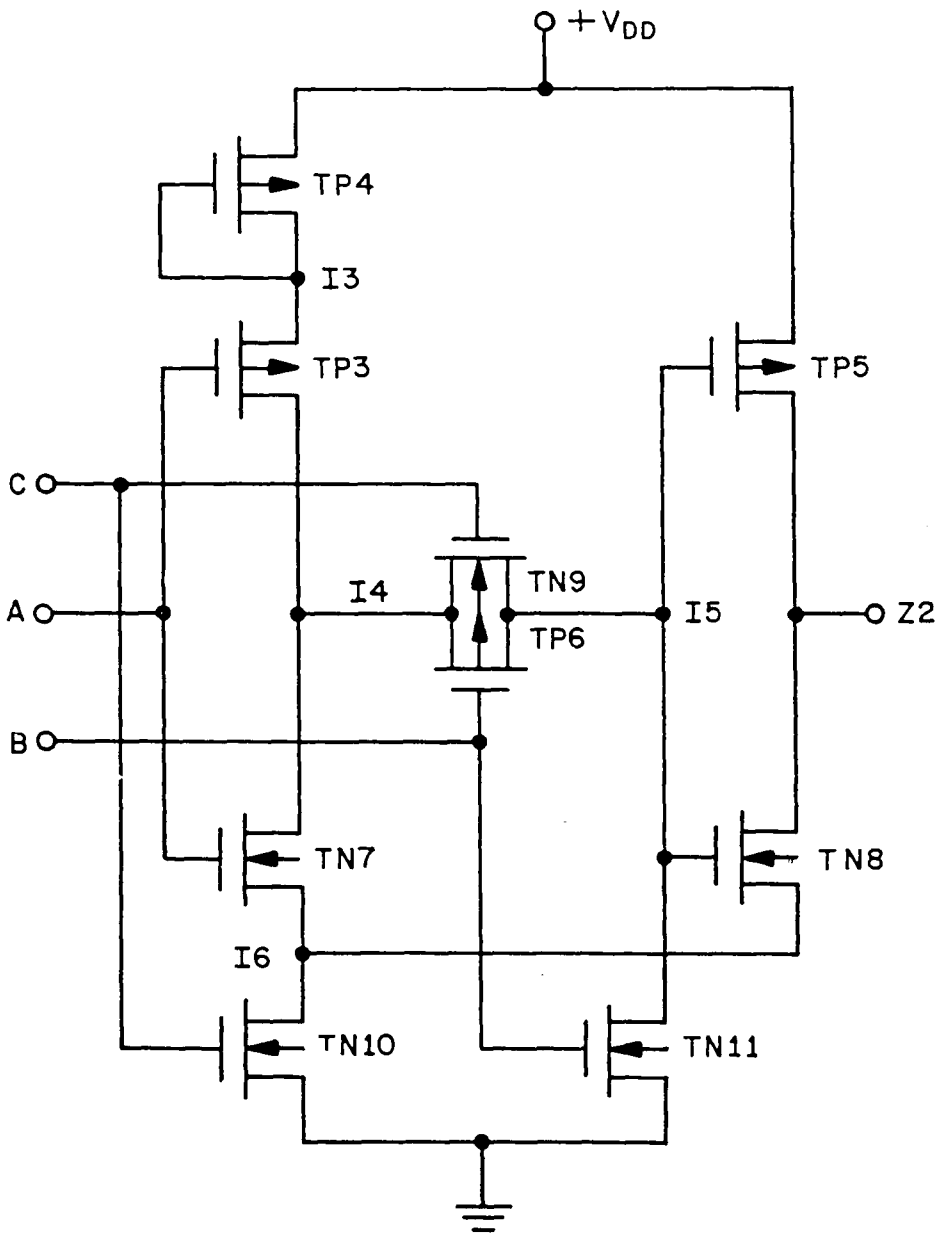
COMPOSITE RTL BUFFER WITH SELECTION

FIGURE 6



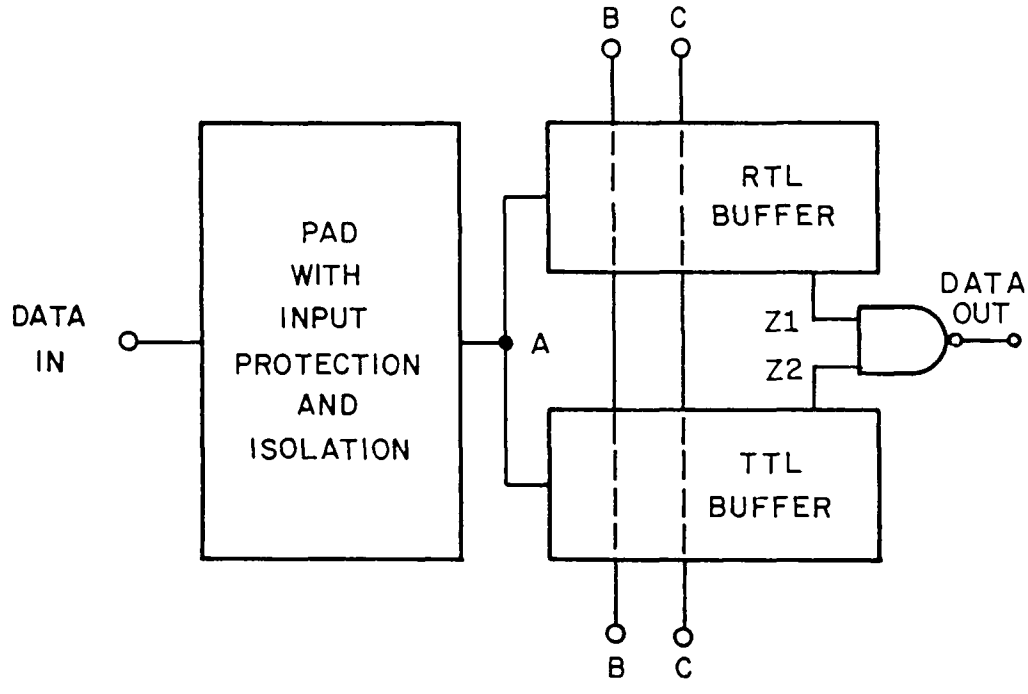
BASIC TTL INPUT BUFFER
WITHOUT SELECTION OR ISOLATION

FIGURE 7



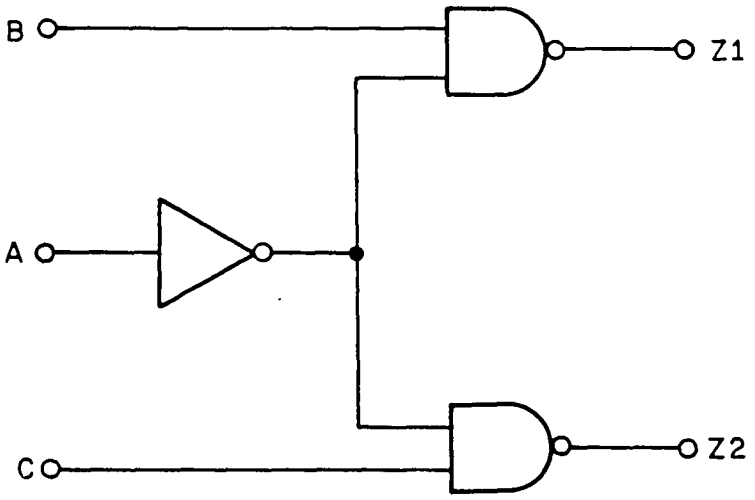
COMPOSITE TTL BUFFER WITH SELECTION

FIGURE 8



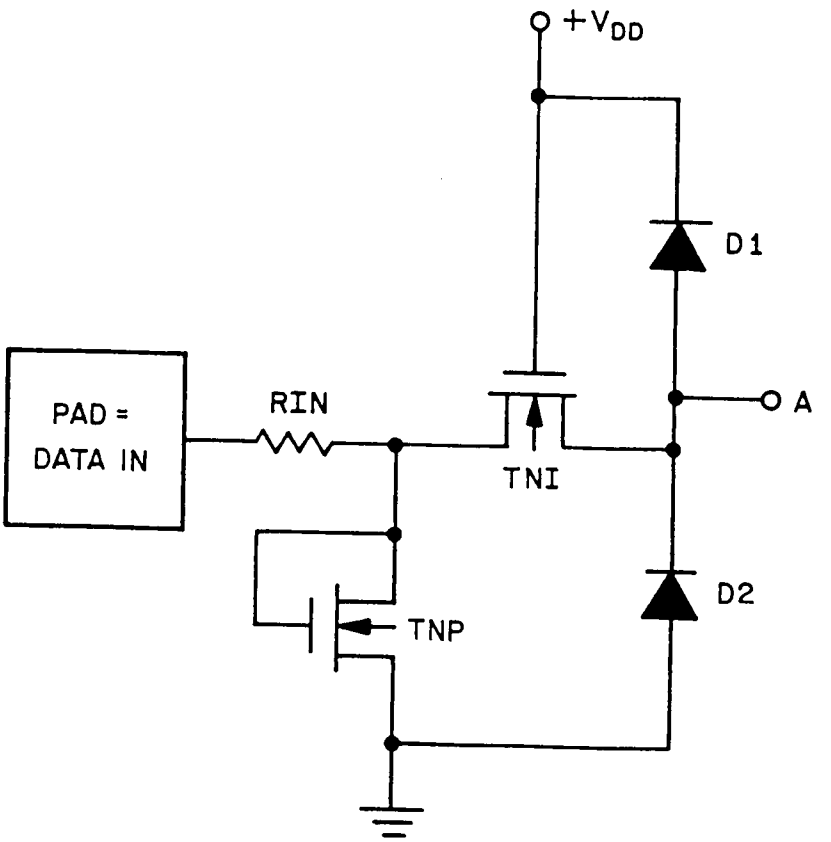
BLOCK DIAGRAM OF COMPOSITE BUFFER

FIGURE 9



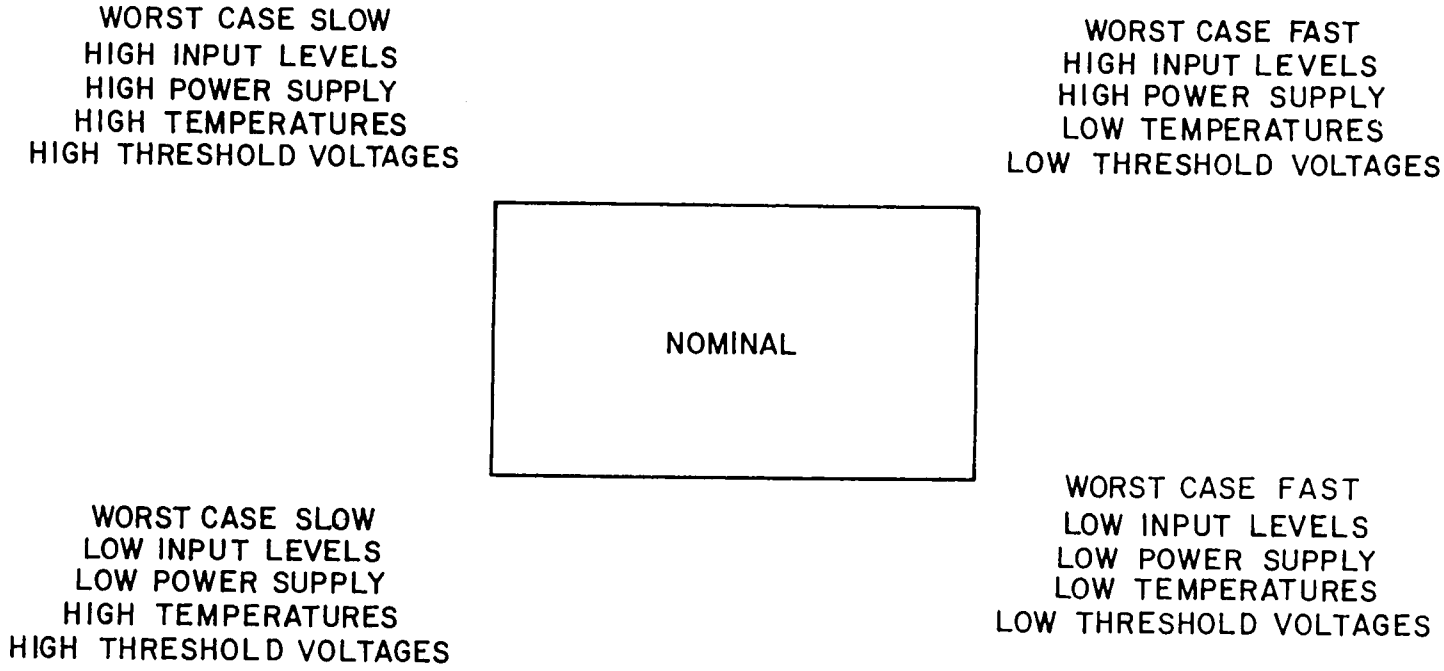
LOGICAL EQUIVALENT
OF RTL/TTL BUFFER

FIGURE 10

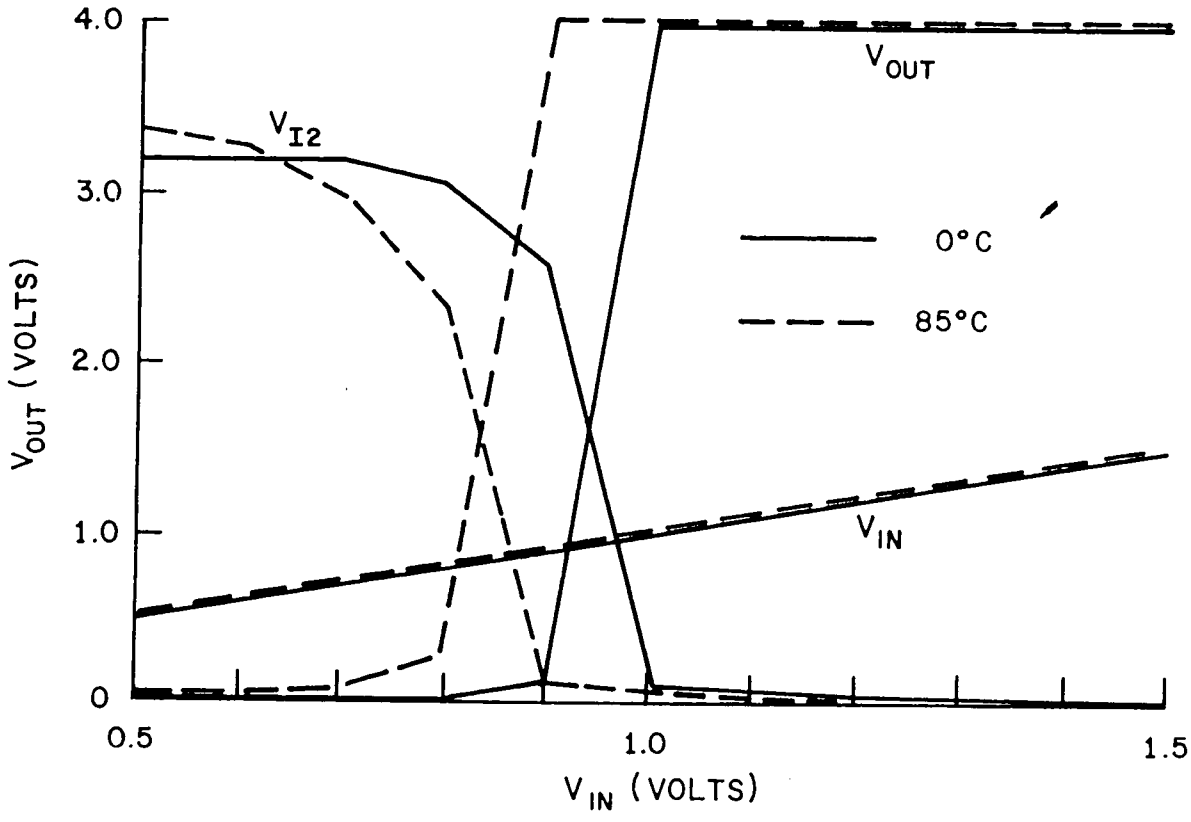


INPUT PAD
WITH ISOLATION AND PROTECTION

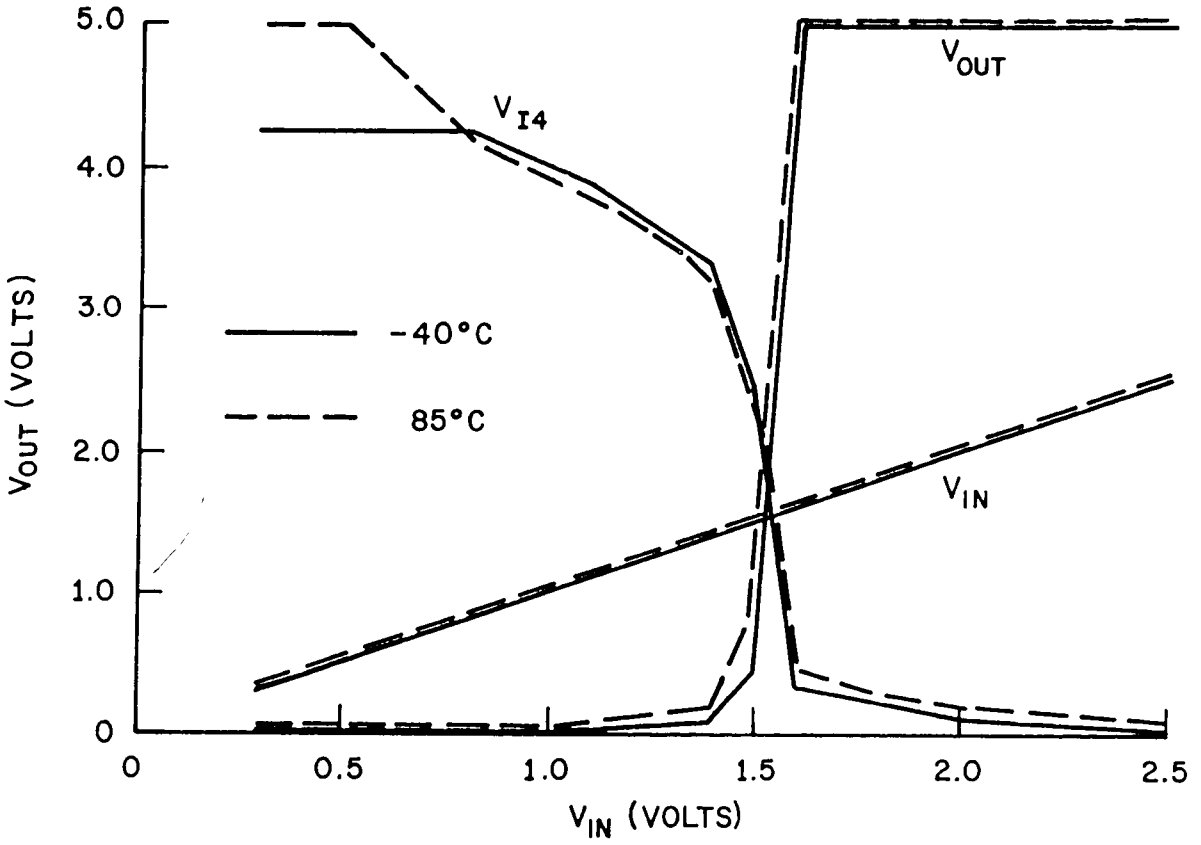
FIGURE 11



DESIGN AND SIMULATION WINDOW
FIGURE 12

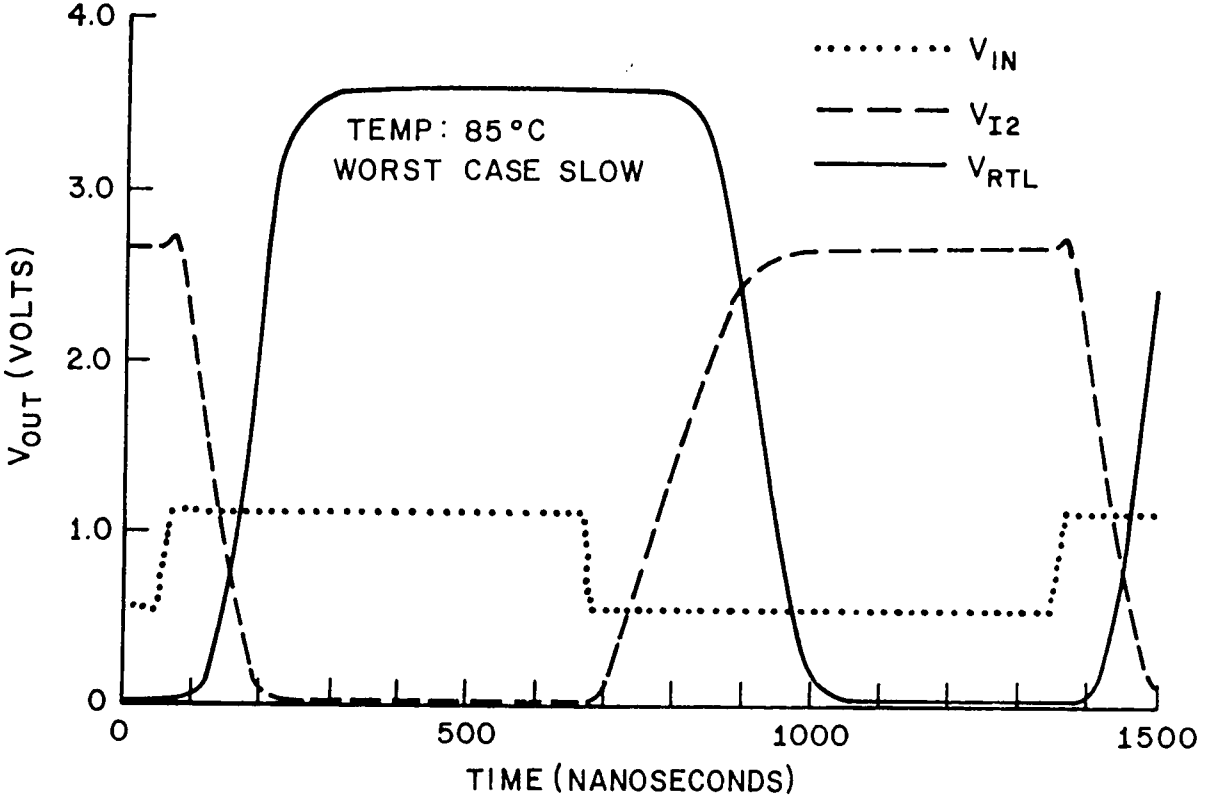


RTL BUFFER DC TRANSFER CURVE
NOMINAL PROCESSING, $V_{DD} = 4.0V$
FIGURE 13

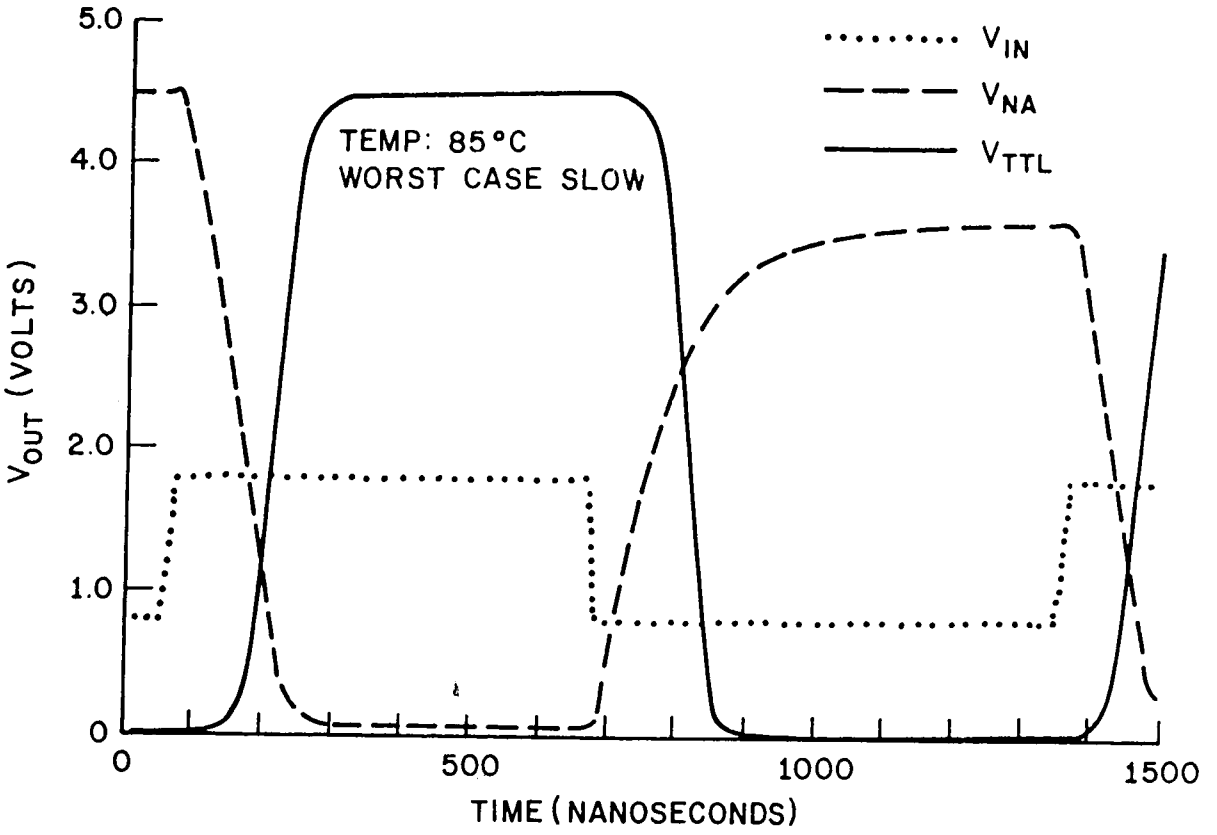


TTL BUFFER DC TRANSFER CURVE
NOMINAL PROCESSING $V_{DD} = 5.0$ V

FIGURE 14



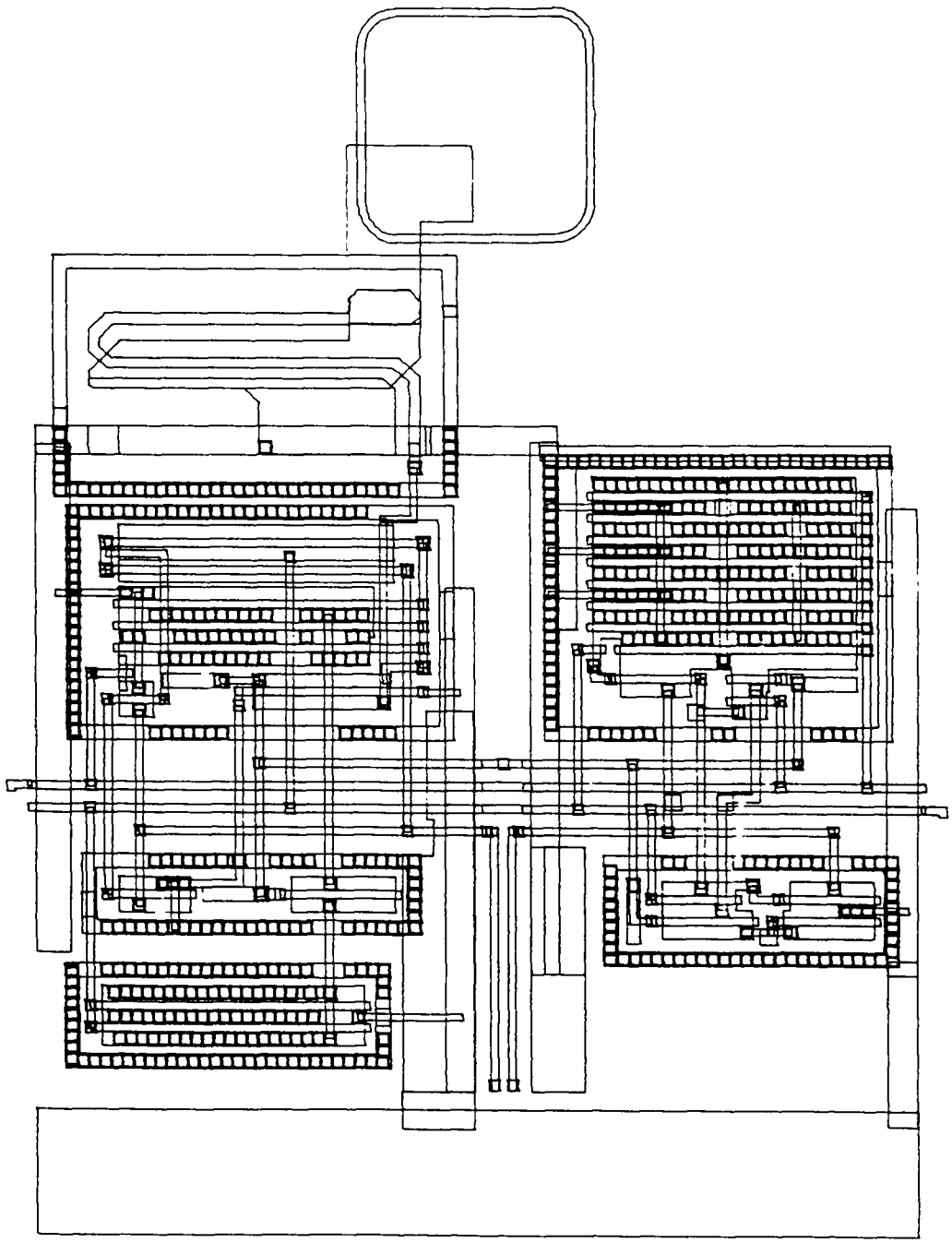
RTL TRANSIENT RESPONSE
HIGH THRESHOLD PROCESSING, V_{DD} = 3.6 V
FIGURE 15



TTL TRANSIENT RESPONSE

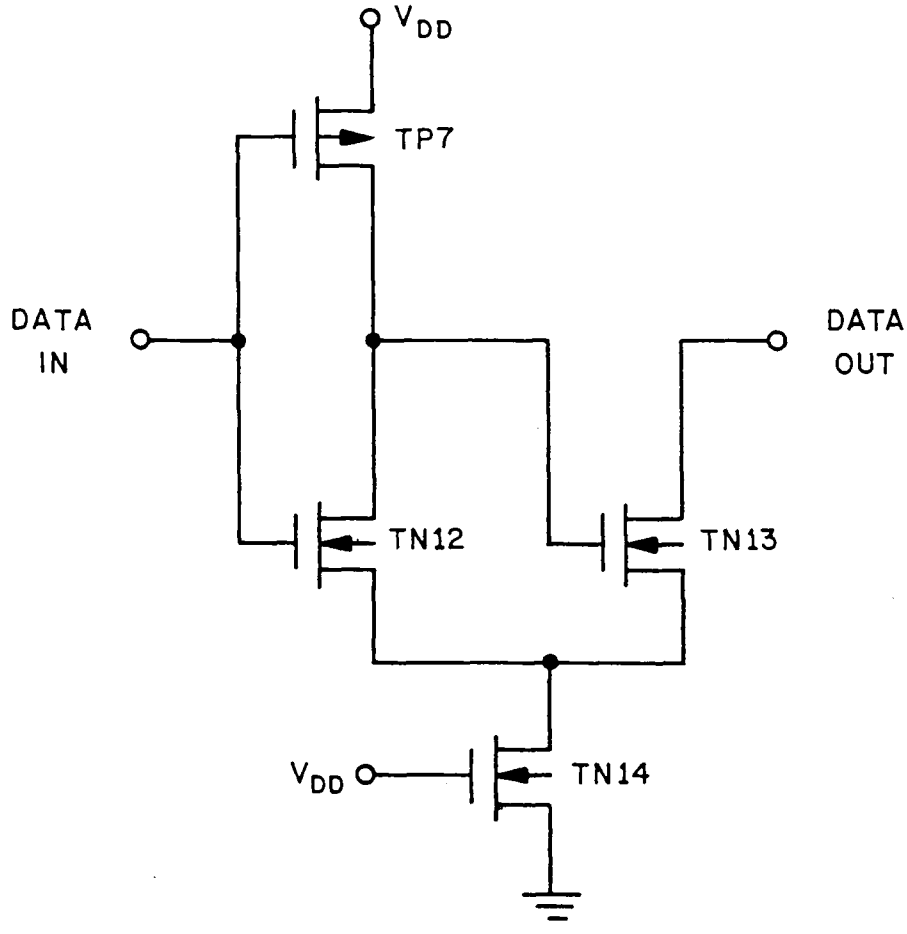
HIGH THRESHOLD PROCESSING, $V_{DD} = 4.5$ V

FIGURE 16



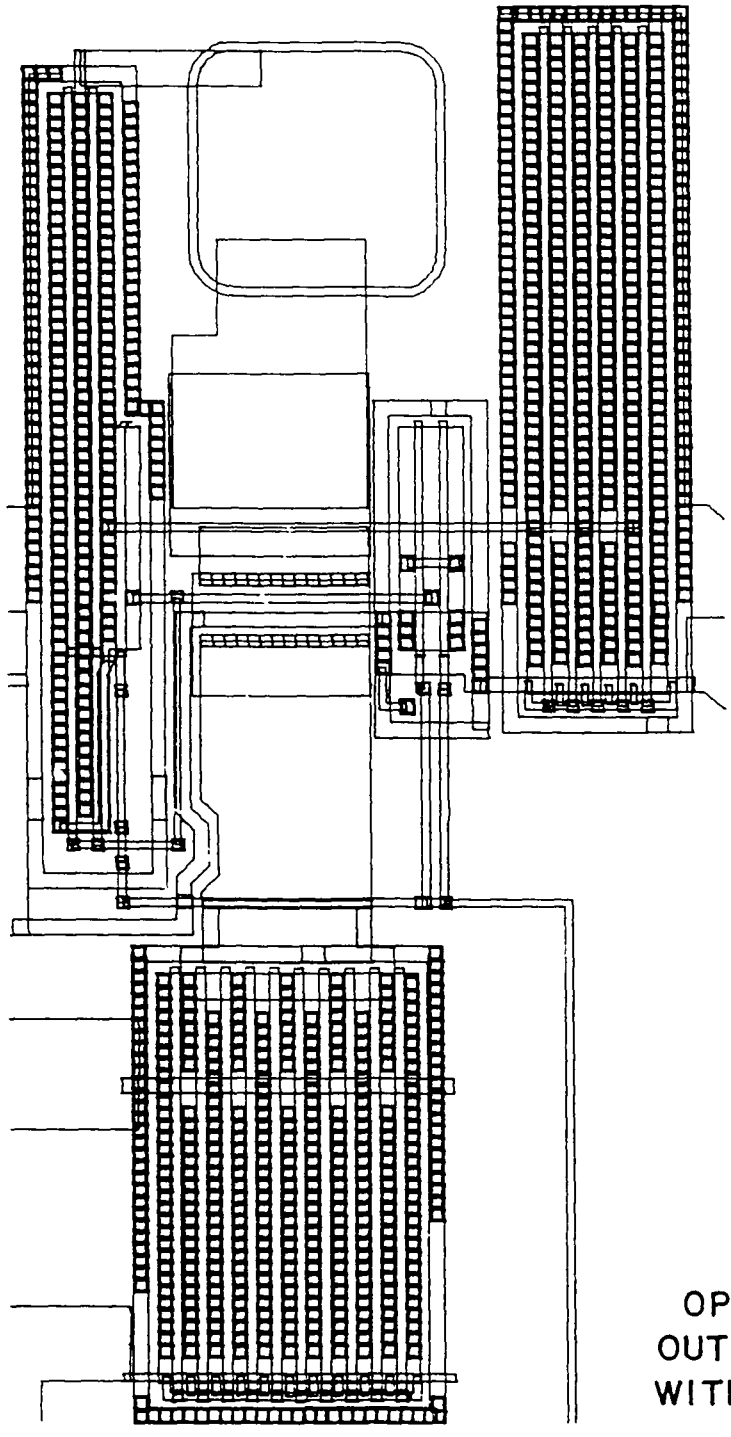
RTL/TTL INPUT BUFFER

FIGURE 17



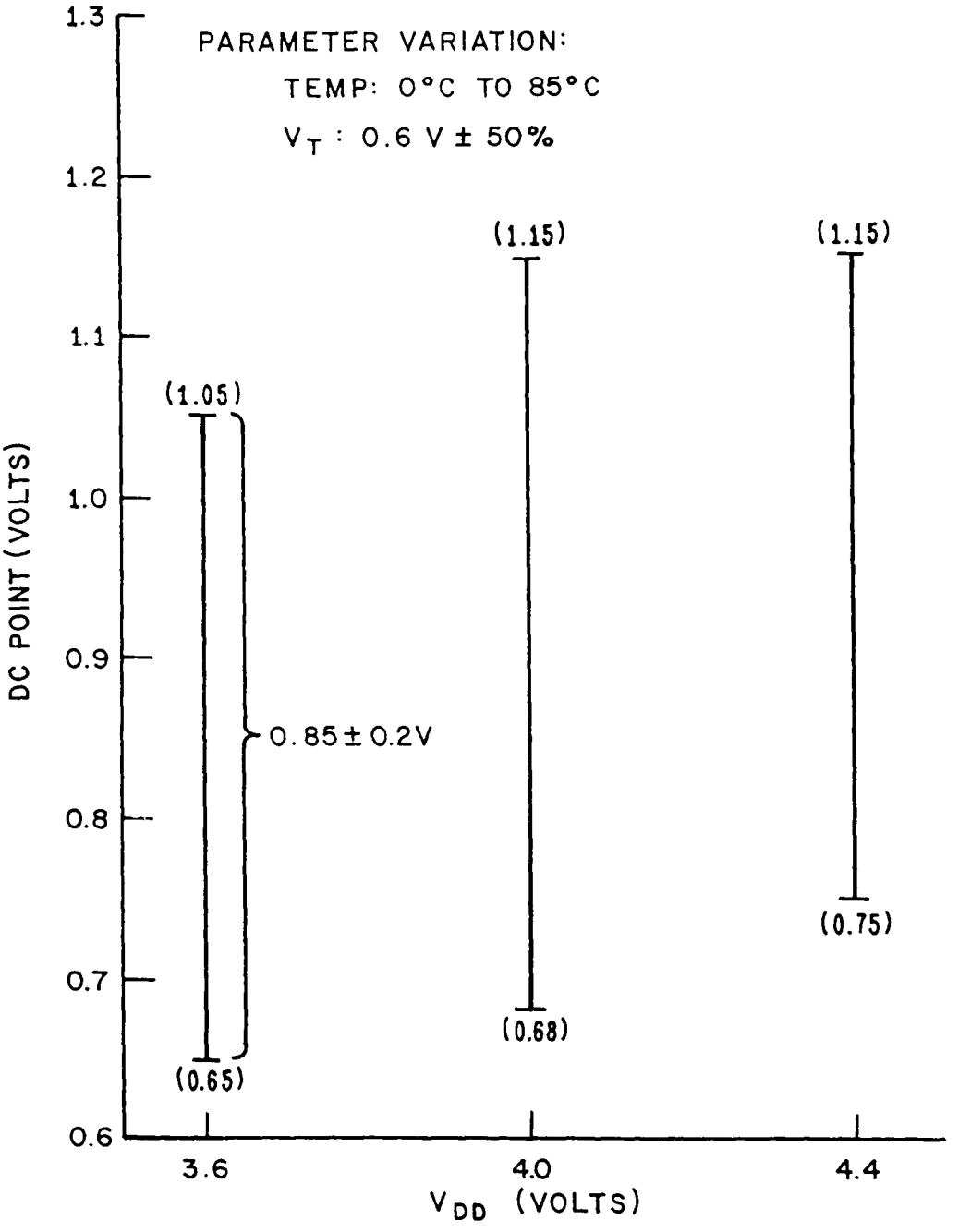
OPEN DRAIN OUTPUT BUFFER WITH ISOLATION

FIGURE 18

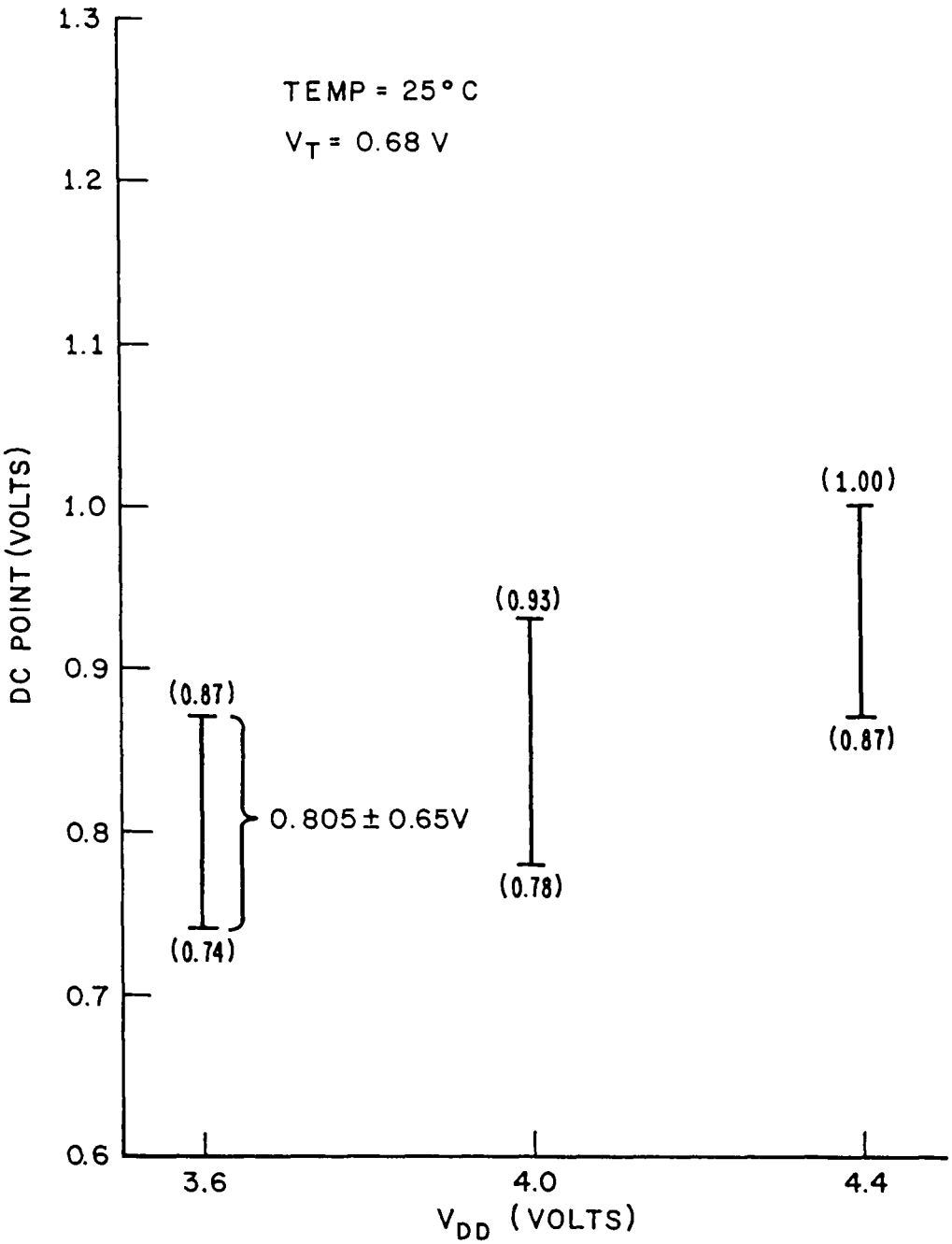


OPEN DRAIN
OUTPUT BUFFER
WITH ISOLATION

FIGURE 19

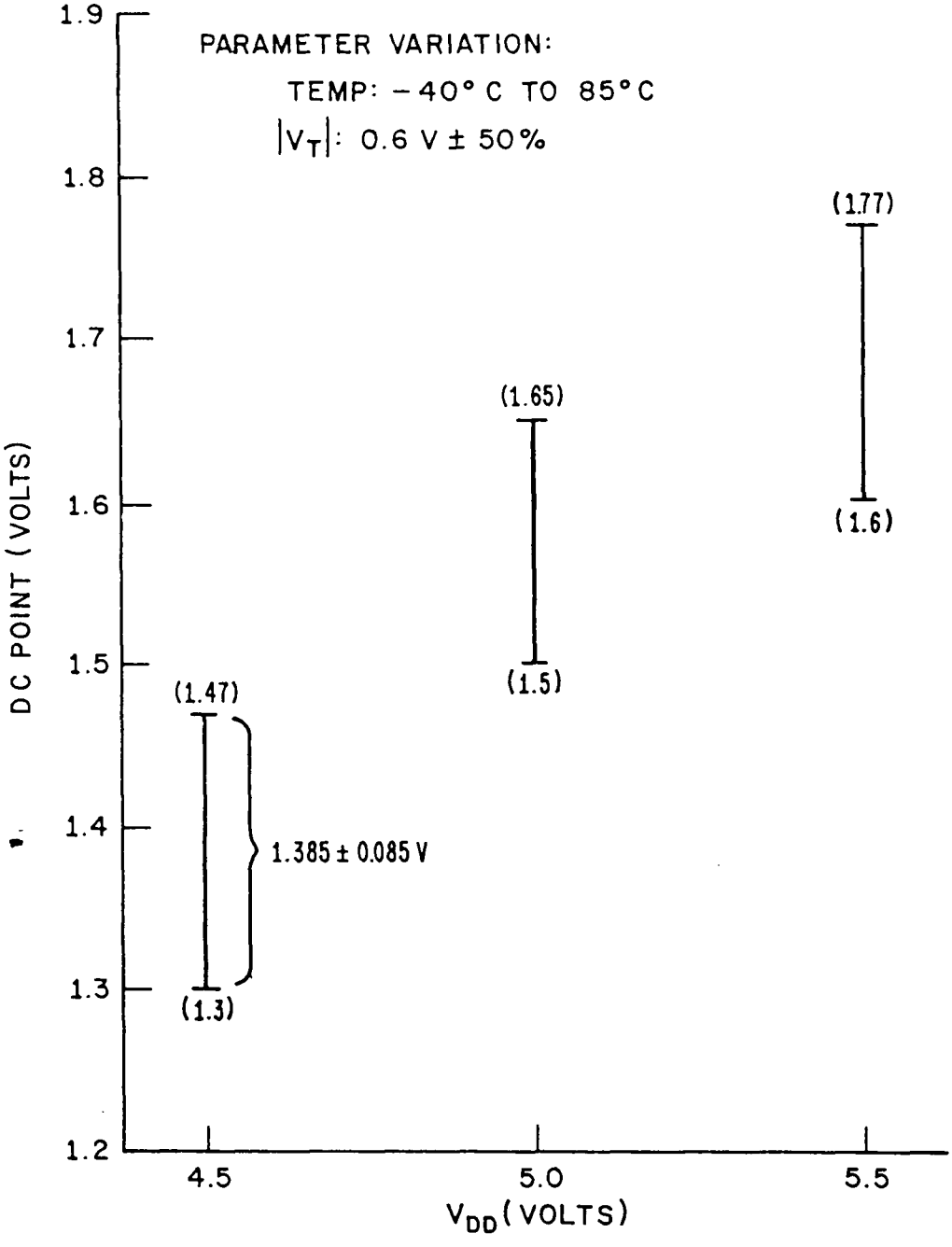


RTL SIMULATION
VARIATION OF DC OPERATING POINT
AS A FUNCTION OF PARAMETER VARIATION
FIGURE 20

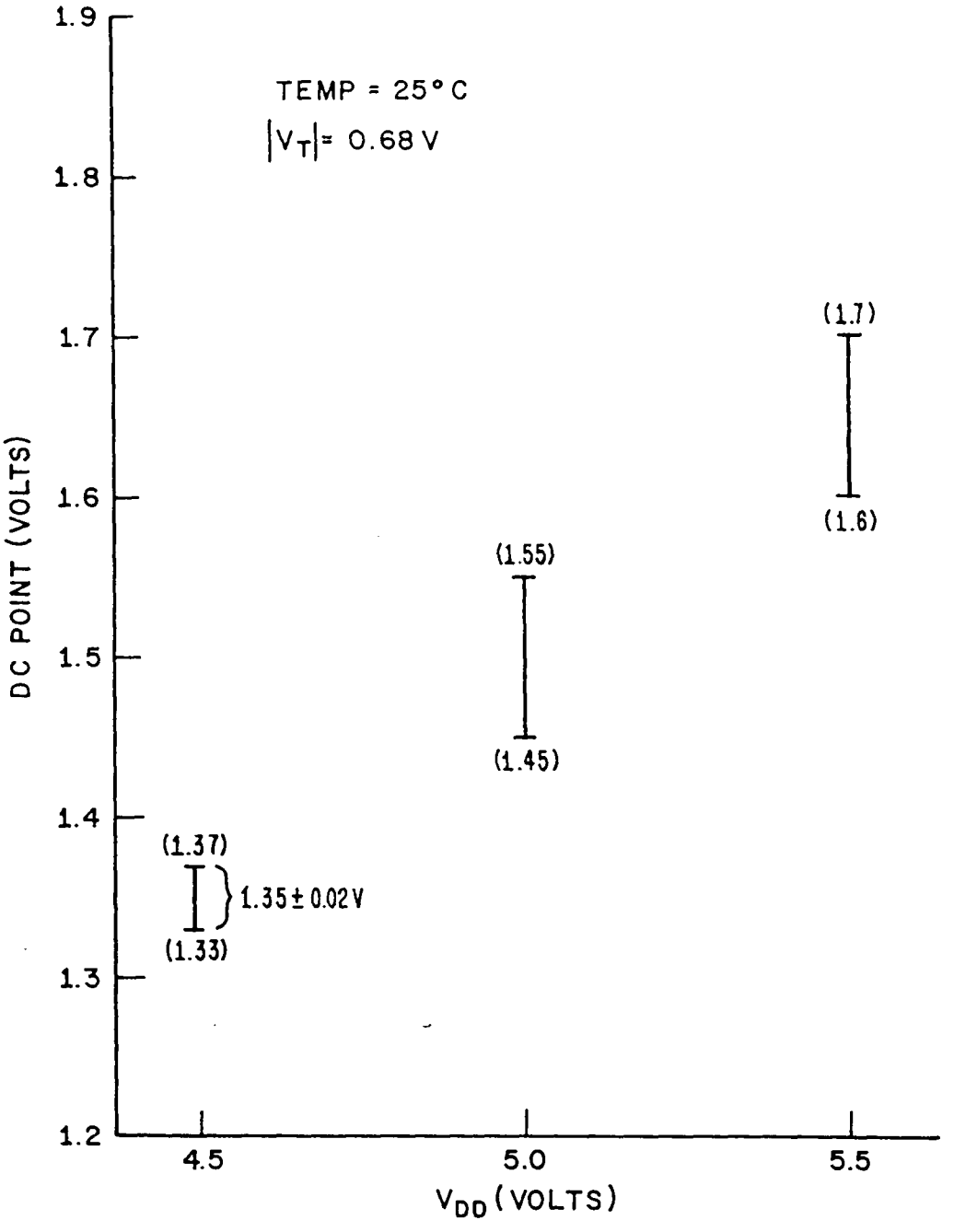


RTL MEASUREMENT
VARIATION OF DC OPERATING POINT
AS A FUNCTION OF BIAS VARIATION

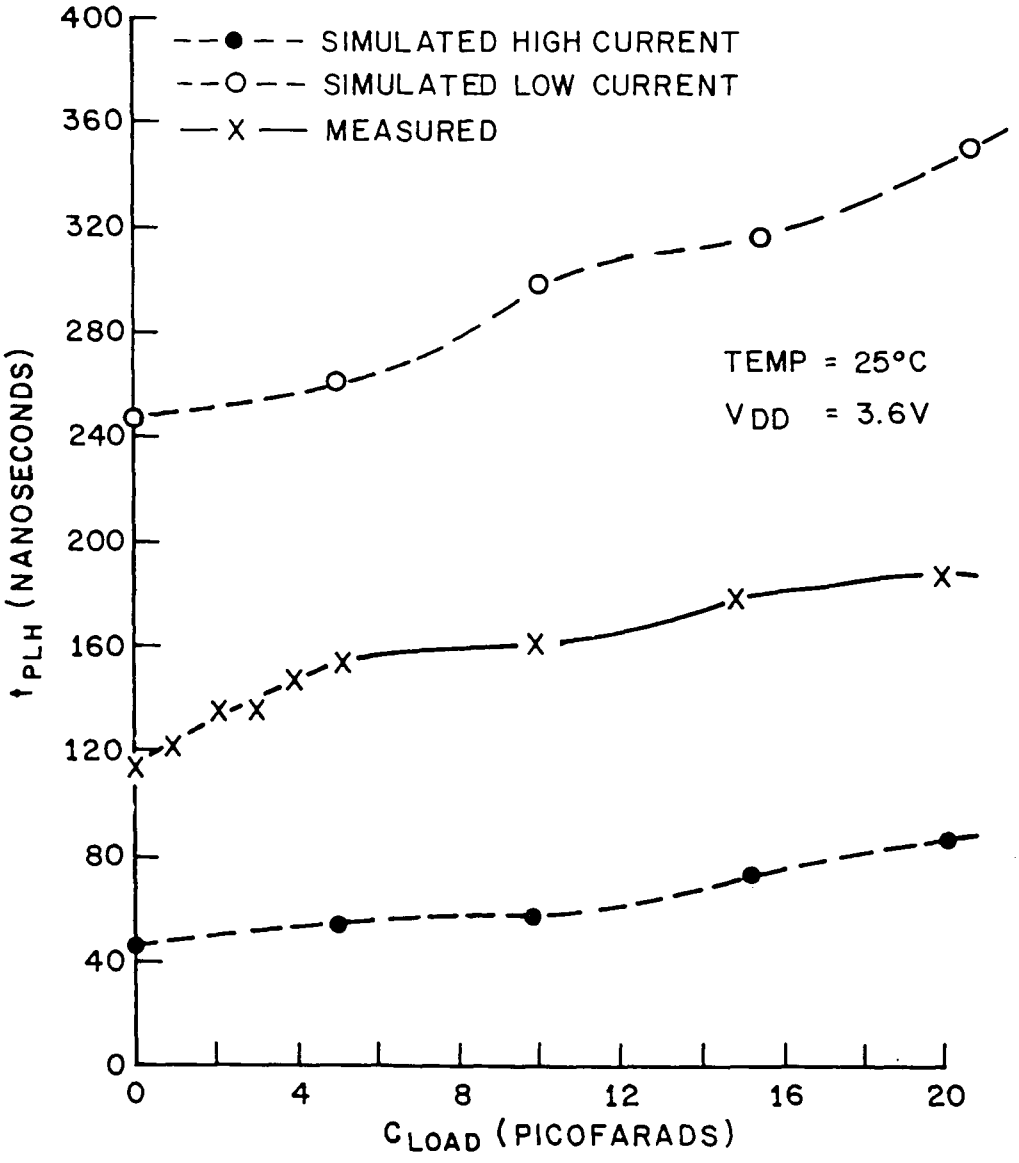
FIGURE 21



TTL SIMULATION
VARIATION OF DC OPERATING POINT
AS A FUNCTION OF PARAMETER VARIATION
FIGURE 22

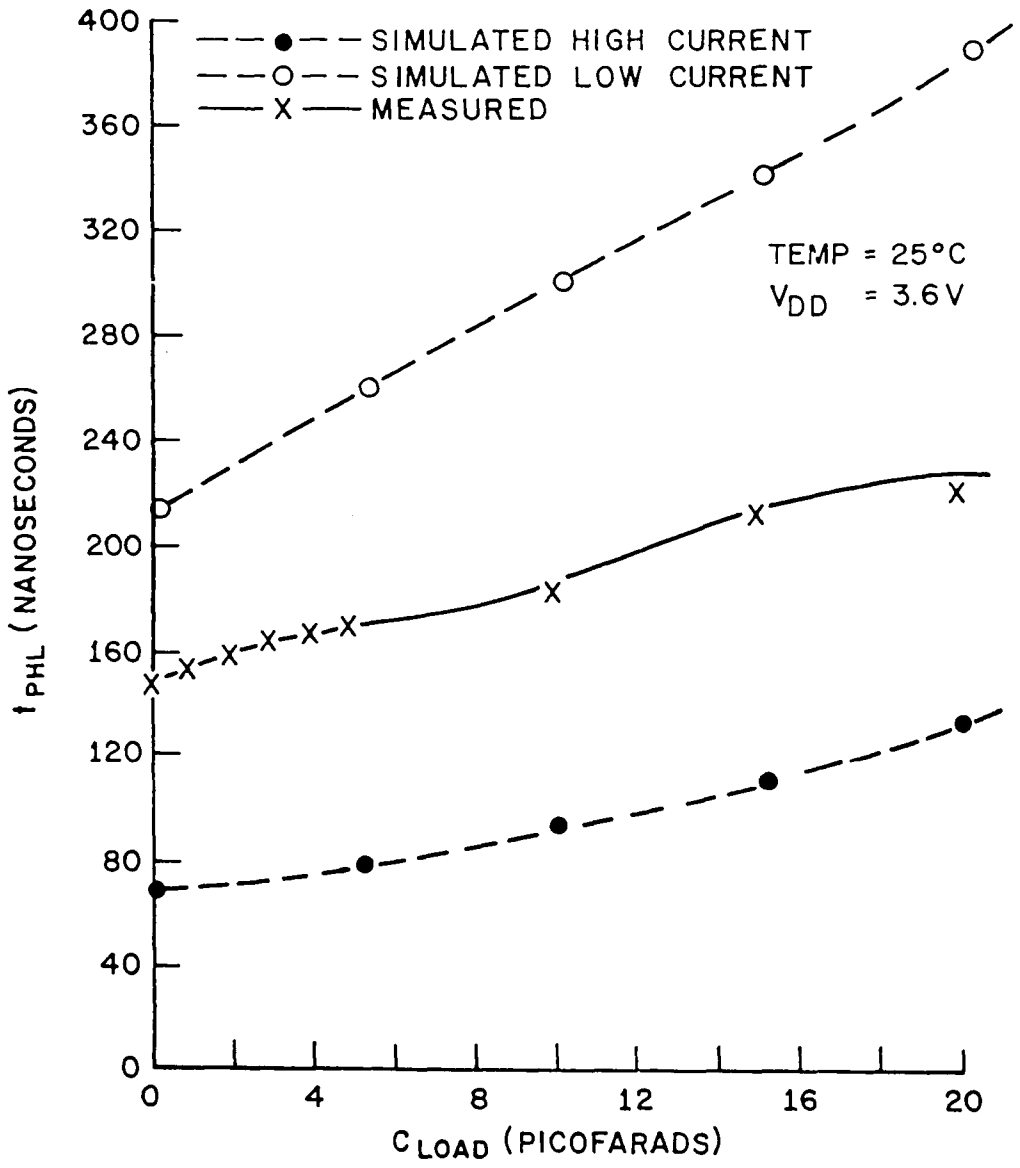


TTL MEASUREMENTS
VARIATION OF D C OPERATING POINT
AS A FUNCTION OF BIAS VARIATION
FIGURE 23



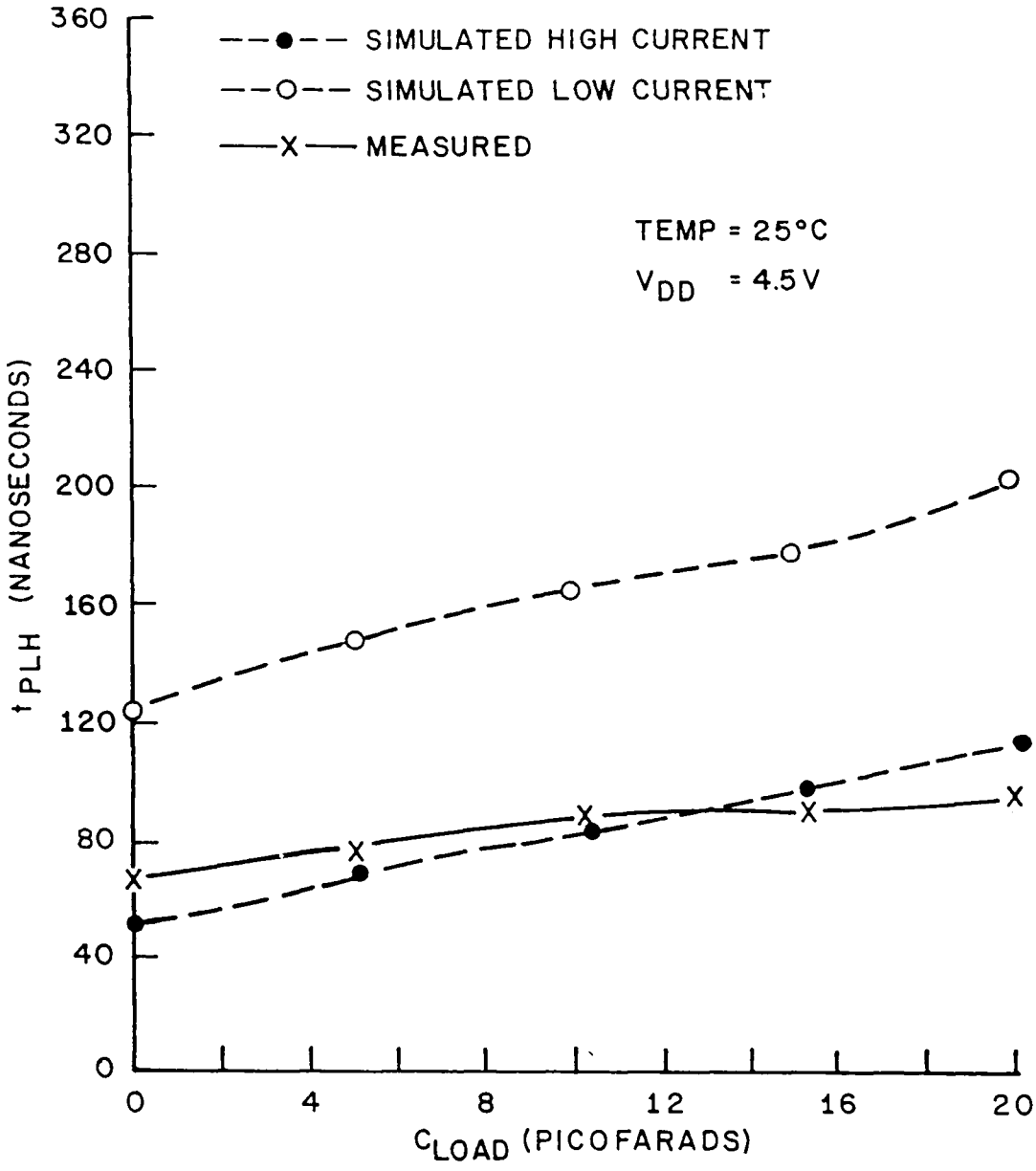
RTL t_{PLH} VS CAPACITIVE LOADING

FIGURE 24



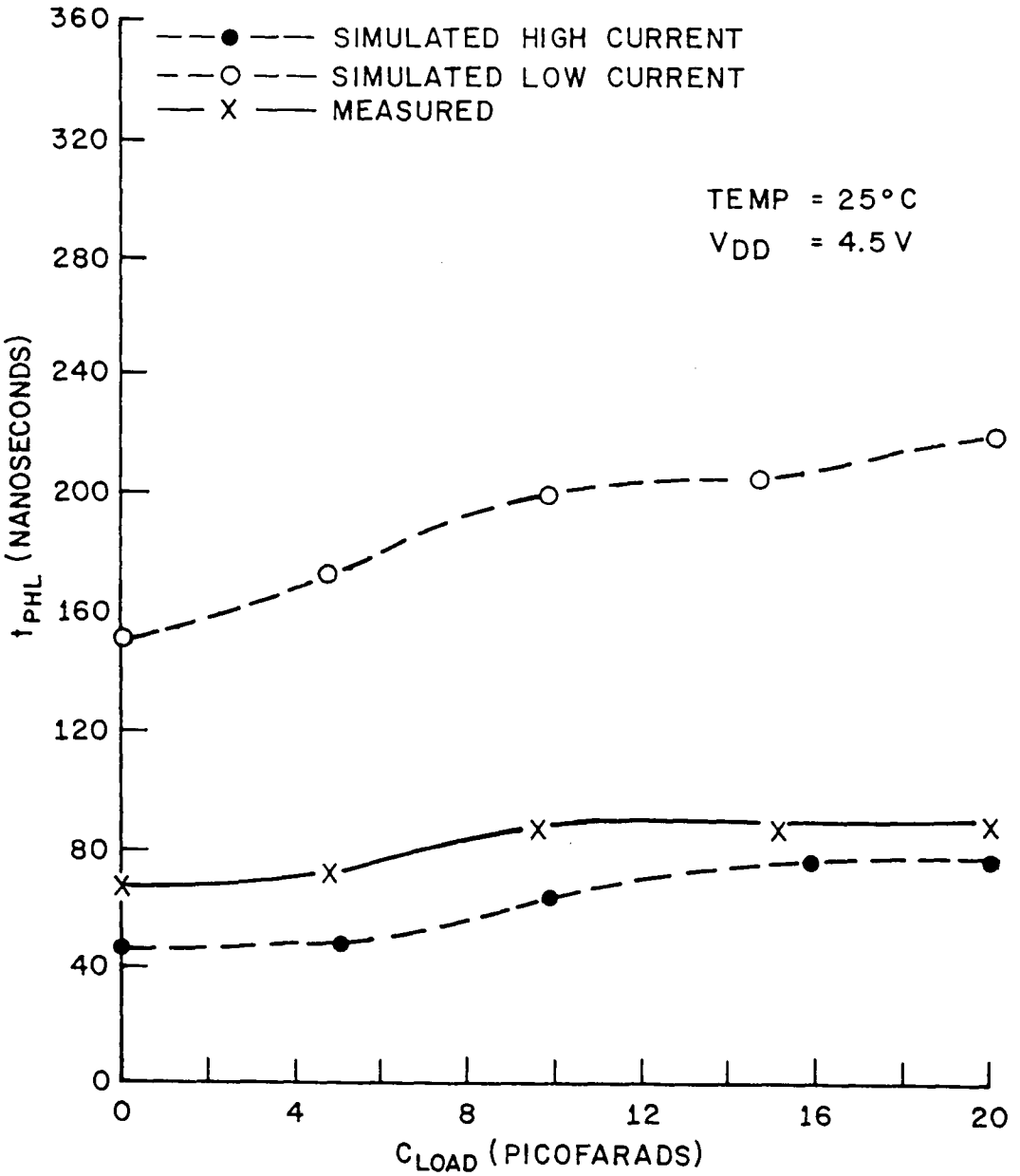
RTL t_{PHL} VS CAPACITIVE LOADING

FIGURE 25



TTL t_{PLH} VS CAPACITIVE LOADING

FIGURE 26



TTL t_{PHL} VS CAPACITIVE LOADING

FIGURE 27

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VITA

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