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A SUBSTRATE-BIAS GENERATOR

By

Dimitris C. Pantelakis

A Thesis

Presented to the Graduate Committee

of Lehigh University

In candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

1980

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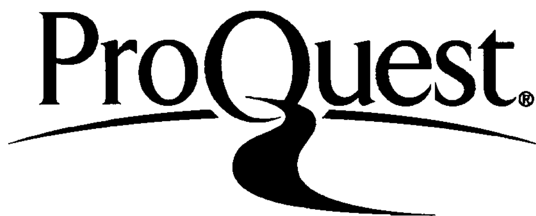

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November 11, 1980
(date)

Professor in Charge

Chairman of the Department

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ABSTRACT

An on chip substrate-bias generator to provide substrate reverse bias in MOSFET's has been designed and developed. The design utilizes four threshold voltages (high enhancement, low enhancement, depletion, zero). If only three thresholds are desirable, a slight modification is necessary.

An analysis of the circuit is presented, as well as circuit simulations and experimental results. The results of this investigation demonstrate that the desired substrate-bias of $-V_{CC} + V_T$ and oscillation frequency of 5MHz at 25°C is achieved. This generator is being used on a 2K x 8 static RAM.

I. INTRODUCTION

The desire to require only a single 5 volts power supply[1] on static RAMs engendered the decision to provide substrate-bias on chip. Reverse biasing the substrate modulates the channel conductance of a MOSFET. This effect is known as the back-gate effect or substrate effect, and plays an important role in the operation of MOS/LSI circuitry. The parasitic capacitance of pn junctions (source to substrate and drain to substrate) is reduced, the change in threshold voltage due to source follower action is minimized and the effects of carrier injection into the substrate are suppressed.[2]

Figure 1 is a block diagram of a substrate-bias generator used on both 4K x 1 and 1K x 4 static RAMs. Three inverters and two RC networks are connected to form a ring oscillator which drives a simple depletion-load inverter push-pull. The capacitor is alternatively charged to near V_{CC} ($V_{CC} = 5 \pm 0.5$ volts) and then discharged into the substrate causing it to be driven negative. The minimum substrate-bias that can be achieved is $-V_{CC} + 2V_T$. The capacitance diode network operates as follows. Capacitor C1 is charged up to V_{CC} when the input signal at node 1 is high through diode D1. This puts node 4 at one threshold voltage above ground. As soon as the signal at node 1 swings down (putting node 1 at ground level), $-V_{CC} + V_T$ is seen at node 4 and node 3 is thus at $-V_{CC} + 2\ V_T$ below

ground. Figure 2 shows the I-V characteristics.

A survey of potential systems customers showed that a 2K x 8 organization was needed. A substrate-bias generator with a more negative swing than the one used on the 4K parts was desirable because the change in threshold voltage is minimized. Substituting a driven device for MOS diode D1 would discard one of the two thresholds giving $-V_{CC} + V_T$.

A circuit that provides these performance advantages is presented. A discussion of the various parameters affecting the MOS device and how their effect is reduced by the circuit design is presented. Characterization of the circuit is also accomplished.

II. CIRCUIT DESCRIPTION

Figure 3 is the ring oscillator section of the substrate bias generator which is used for timing purposes. Figure 4 is the driver/pump section. The oscillator and driver are merged into Figure 5. The oscillator consists of 11 stages when nodes 1214 and 1228 are high and 7 stages when node 1206 goes high. To slow the oscillation to a nominal 5MHz for pumping efficiency, inverters 1201, 1203 and 1212 need low gain high capacitance transistors. The next inverter 1213 has high gain transistors and is used to amplify signal 1212. The required timing signals 1205 through 1228 are able to achieve full MOS levels.

The substrate is connected to the terminal labeled V_{BB}. The requirement is to charge the gate of capacitor M1229 to V_{cc} with the aid of transistors M1217 and M1232 and to be able to discharge it into the substrate through MOS diode M1230. We therefore have to insure that node 1210 gets up to V_{cc} and node 1211 is held at ground and the discharge is only into the substrate.

The operation of the driver/pump can be described by starting with node 1206 going high. This puts node 1228 at ground and transistor M1247 (Enhancement type) is turned on. There is essentially zero charge on capacitor M1248. As soon as node 1205 goes up the gate of transistor M1214 self-bootstraps which allows capacitor

M1227 to charge up to V_{cc}. The pull down of node 1219 is delayed by the aid of transistors M1245, M1234 and M1244. Node 1210 goes up to one threshold below V_{cc}. As this occurs node 1226 (driven push-pull) rises causing node 1215 to rise while capacitor M1228 is charging through M1233. Node 1215 gets high enough to turn on M1232 (this is the driven device that replaced MOS diode D1 of Figure 1) so that node 1211 is held near ground. After three inverter delays (1207, 1208 & 1214) node 1214 rises causing node 1209 to rise above V_{cc} and node 1210 to V_{cc}. After a further two inverter delays (1204, 1228) node 1228 rises causing node 1226 to rise further and raising node 1215 further up so that M1232 can be turned on long enough allowing capacitor M1229 to charge to V_{cc}. Devices M1255 and M1254 which make up an inverter are necessary to avoid slowing down signal 1207 due to loading from M1246.

Discharge of capacitor M1229 into the substrate begins when node 1206 goes high which causes node 1226 to return to ground and node 1215 to go negative until M1228 discharges into the substrate through diode M1235. A negative gate to source voltage is applied to M1232 assuring that it is turned off. After two inverter delays (1207, 1208) node 1208 goes high pulling node 1210 to ground. Capacitor M1229 discharges into the substrate through diode M1230.

A. Layout

The circuit layout was done assuming a scanning projection printer operating in the near ultraviolet. The layout rules, as characterized by an average half-pitch were 2.8 μm.

B. Processing

The fabrication process is a single level poly silicon (selectively doped)/multiple threshold NMOS-process.

III. EFFECT UPON THRESHOLD

When a bias voltage is applied between substrate and source there is a change in transistor characteristics. This is referred to as body effect.[3] Due to the substrate being reverse biased with respect to the source the depletion region between the channel and substrate widens and contains more charge; consequently, the gate electric field necessary to form a channel is increased. The apparent threshold voltage of the transistor is thus increased. MOS transistors can be connected in series to perform gating functions. This results in an increase in source-to-substrate voltage as the signal proceeds along the series chain. It also results in an increase in effective threshold voltage of devices whose source potential is higher than the substrate potential.

The total threshold voltage is the algebraic sum of the intrinsic threshold voltage (of which a derivation is shown in the Appendix) and that due to surface states.

$$V_{th} = V_{Ith} + V_{ss}$$

$$V_{th} = -K_1 \sqrt{\phi_s} + V_{ss}$$

where $K_1 = \pm (t_{ox}/\varepsilon_{ox}) \sqrt{2q\varepsilon_s N}$

(minus for N-channel)

$$\phi_s = 2\ \phi_F$$

$$V_{ss} = -\ Q_{ss} \frac{t_{ox}}{\varepsilon_{ox}}$$

It is often convenient to express V_{th} in terms of a fixed value ($V_{BB} = 0$) plus a variable term, ΔV_{th} which is a function of V_{BB}.

$$V_{th}(V_{BB}) = V_{ss} - K_1 \sqrt{-(2\ \phi_F + V_{BB})}$$

$$V_{th}(V_{BB}) = V_{ss} - K_1 \sqrt{-2\ \phi_F} + K_1 \sqrt{-2\ \phi_F} - K_1 \sqrt{-(2\ \phi_F + V_{BB})}$$

$$V_{th}(V_{BB}) = V_{th} + \Delta V_{th}$$

$$\Delta V_{th} = -K_1 [\ \sqrt{-(2\ \phi_F + V_{BB})} - \sqrt{-2\ \phi_F}\ ] \quad ....3.1$$

where V_{BB} is the substrate-bias voltage

IV. EFFECT UPON CURRENT

The magnitude of the substrate-bias and the substrate resistivity will affect the I-V curves of a MOSFET.[4] Applying a negative substrate-bias to an N-channel device decreases the drain-to-source conductance in the linear resistance and in the saturated-current region for all gate voltages. This decrease in current is due to the drain-substrate and channel substrate diodes increasing in reverse voltage due to the substrate-bias. The depletion region widens and spreads into the channel decreasing the drain-to-source conductance. As a result pinch-off will occur at a lower drain voltage for a fixed gate-to-source voltage and the current will saturate at a lower value.

If the equation for pinch-off voltage is substituted into the expression for drain current at saturation, then an expression is developed which relates I_D to the substrate-bias.

$$I_D = \frac{\beta}{2} (V_G - V_{th})^2 \quad \text{.................. 4.1}$$

$$V_{th} = -K_1 \sqrt{\pm (\phi_s + V_{BB})} + V_{ss}$$

$$I_D = \frac{\beta}{2} (V_G + K_1 \sqrt{\pm (\phi_s + V_{BB})} - V_{ss})^2$$

K_1 is a negative for an n-channel device.

$$I_D = \frac{\beta}{2} [K_1 \sqrt{\pm (\phi_s + V_{BB})} + (V_G - V_{SS})]^2 \quad \ldots\ldots 4.2$$

This equation has the same form as eq. 4.1.

The gain or transconductance due to the back gate is analogous to the front gate transconductance.[5]

The amount of variation in the drain-to-source I-V curves decreases as the resistivity of the substrate increases. Therefore at very high resistivities, the variation is negligible because the depletion region will widen much more into the high resistivity substrate than into the channel.

V. MEASUREMENTS

Measurements were done on wafer BJ568F. Figure 6 shows the frequency as a function of temperature. It verifies that the oscillator is oscillating at approximately 5 MHz. The mobility of the free carriers in the conducting channel will vary as a function of temperature. Electron and hole mobilities in inversion layers have a $T^{-\frac{3}{2}}$ power dependence at higher temperatures.[7] As the temperature increases, the number of electron-lattice collisions per unit time will also increase resulting in a lowering of the average drift velocity of the electrons. Hence a decrease in mobility. The conductivity of the channel is decreased as is the drain current.

Figure 7 shows a typical I-V characteristic of the substrate-bias generator measured at 25°C. From this curve one can determine the open circuit voltage, the short circuit current and the output impedance of the generator. An external connection between the substrate generator pad and the substrate increases the short circuit current by 35.7%. This occurs because of the improved minority carrier collection efficiency.[8] Figure 8 shows how the I-V characteristics vary with temperature. The short circuit current decreases at a rate of 0.7 nA/°C (see figure 9).

A plot of the short circuit current is shown in Figures 9, 10 and 11. Figure 10 indicates that the short-

circuit current is a linear function of the frequency. A plot of leakage current with temperature is shown in Figure 13. I_{sc}/frequency has a small variation at low temperatures (Figure 11).

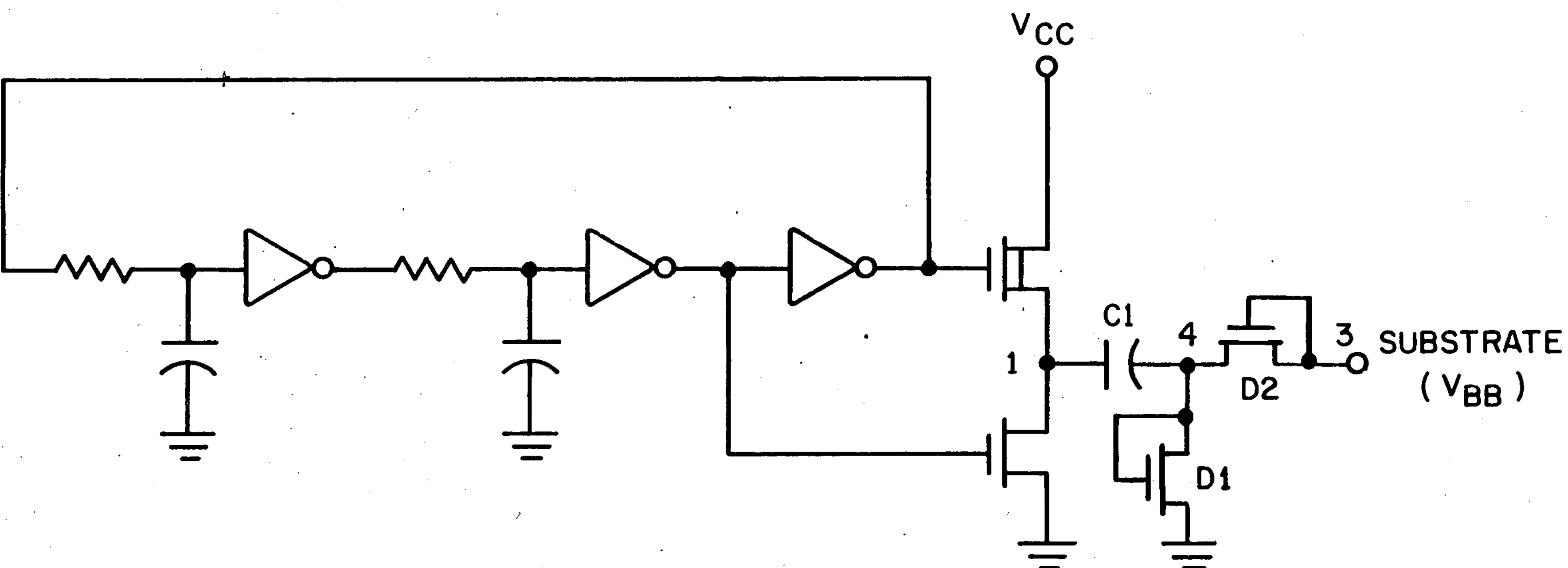
Figure 12 shows the open circuit voltage vs temperature. The measurements indicate that the substrate-bias is $-V_{cc} + V_T$ over a wide temperature range.

Reverse biasing a diode gives rise to reverse currents which is due to electron-hole pairs being generated.[7] Figure 13 shows a plot of reverse current versus substrate-bias. As the temperature is increased the diffusion current will dominate.

VI. CONCLUSION

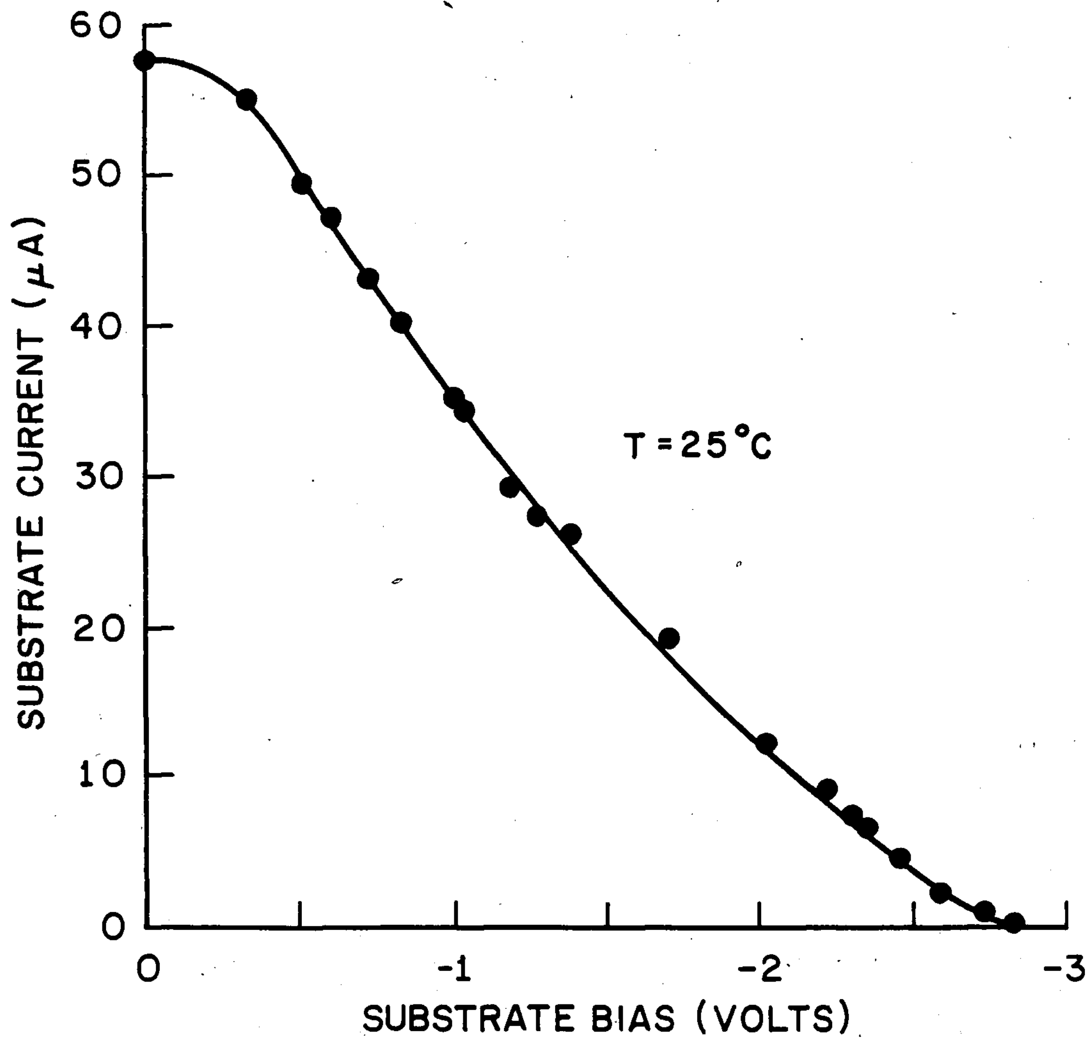
A substrate-bias generator designed to be used in MOS integrated circuits has been developed. It is currently being used on a 2K x 8 static RAM.

Measurements and circuit simulations indicate the substrate is pumped to $-V_{CC}+V_T$ over a wide temperature range. The oscillation frequency is approximatley 5MHz at room temperature. It was observed that the short circuit current decreased with decreasing frequency. It was also observed that at high temperatures leakage current was significant.



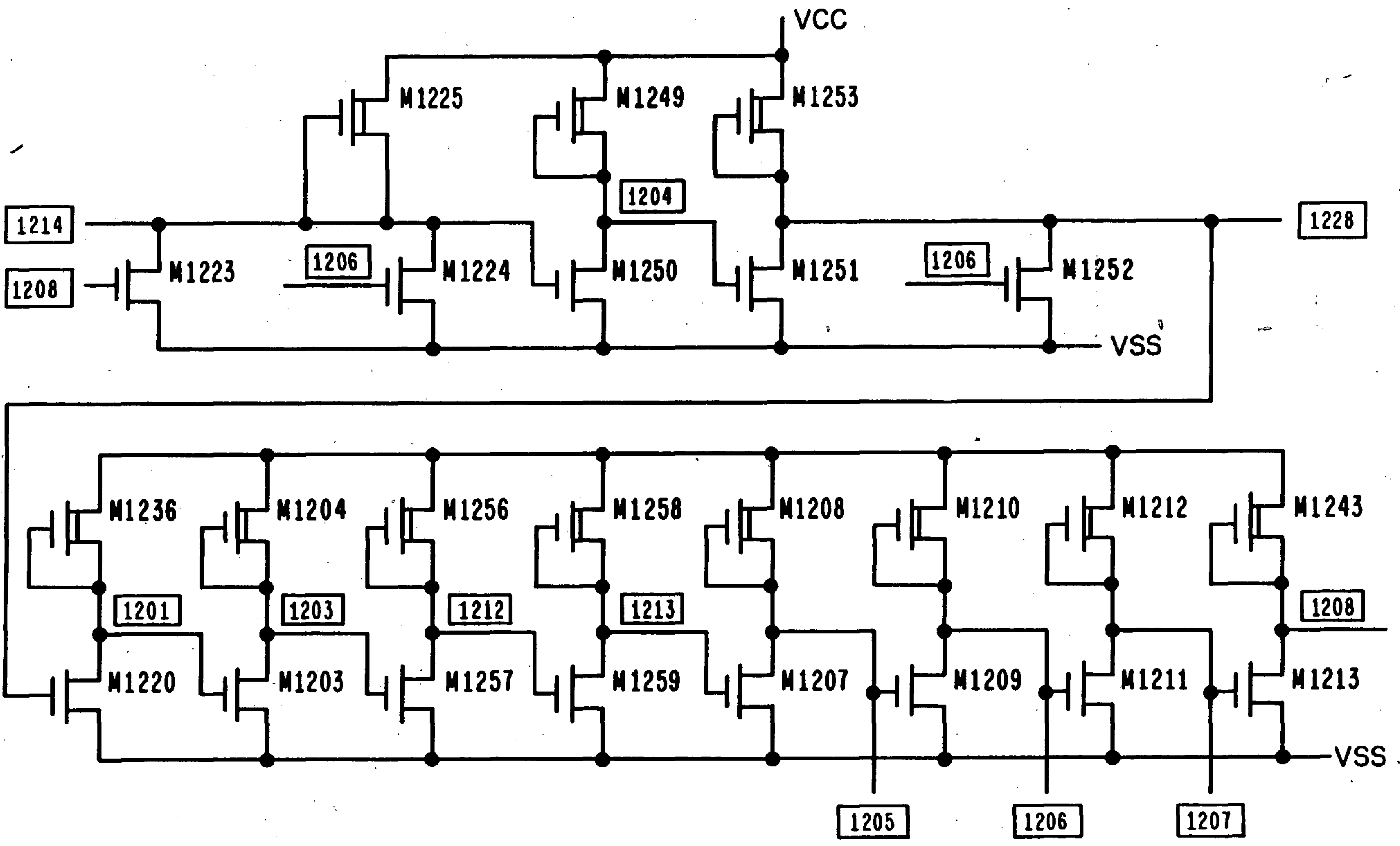
BLOCK DIAGRAM
OF THE SUBSTRATE BIAS GENERATOR

FIGURE 1



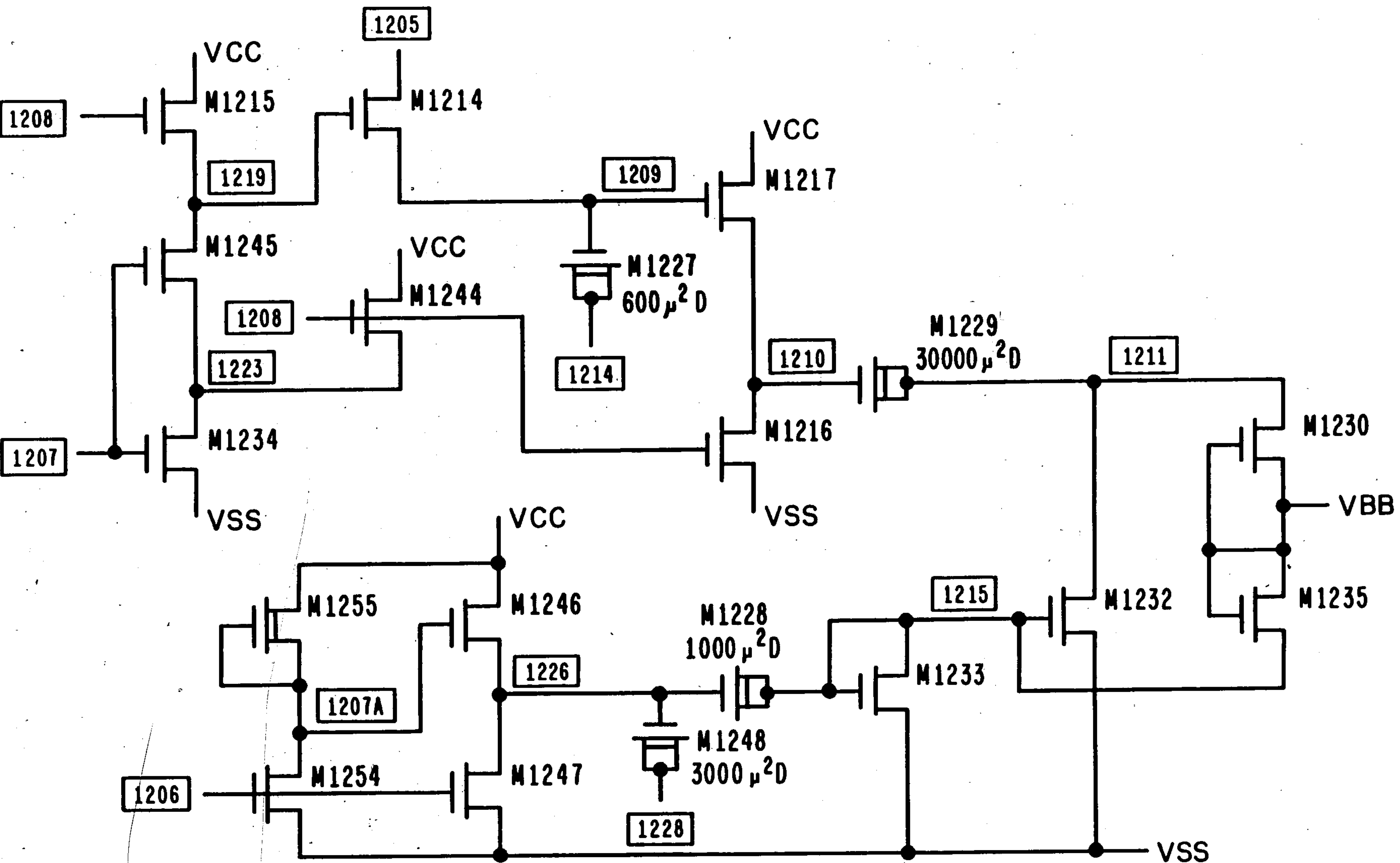
TYPICAL I-V CHARACTERISTIC OF SUBSTRATE BIAS GENERATOR

FIGURE 2



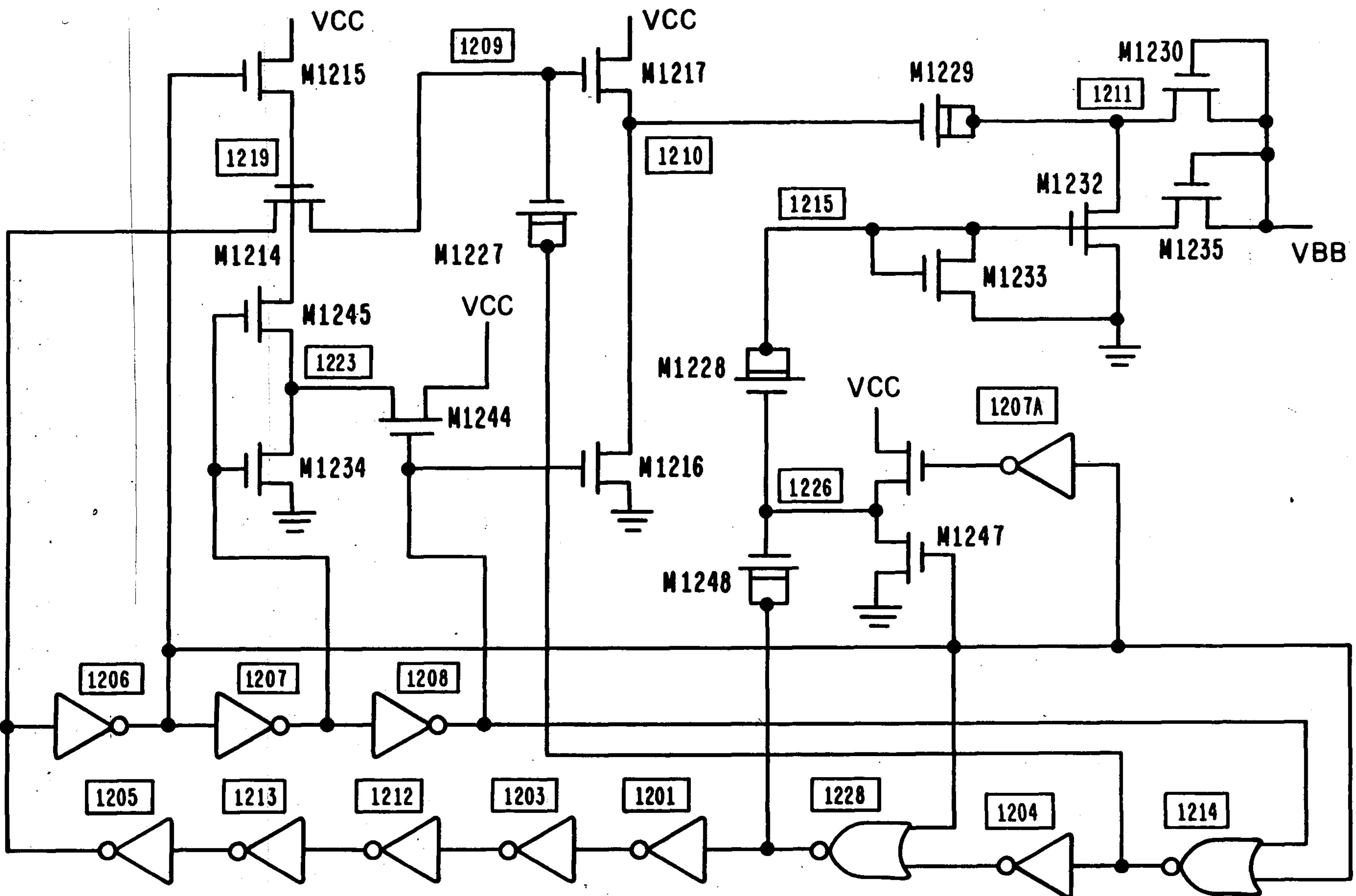
SUBSTRATE BIAS GENERATOR (VBB1)

FIGURE 3

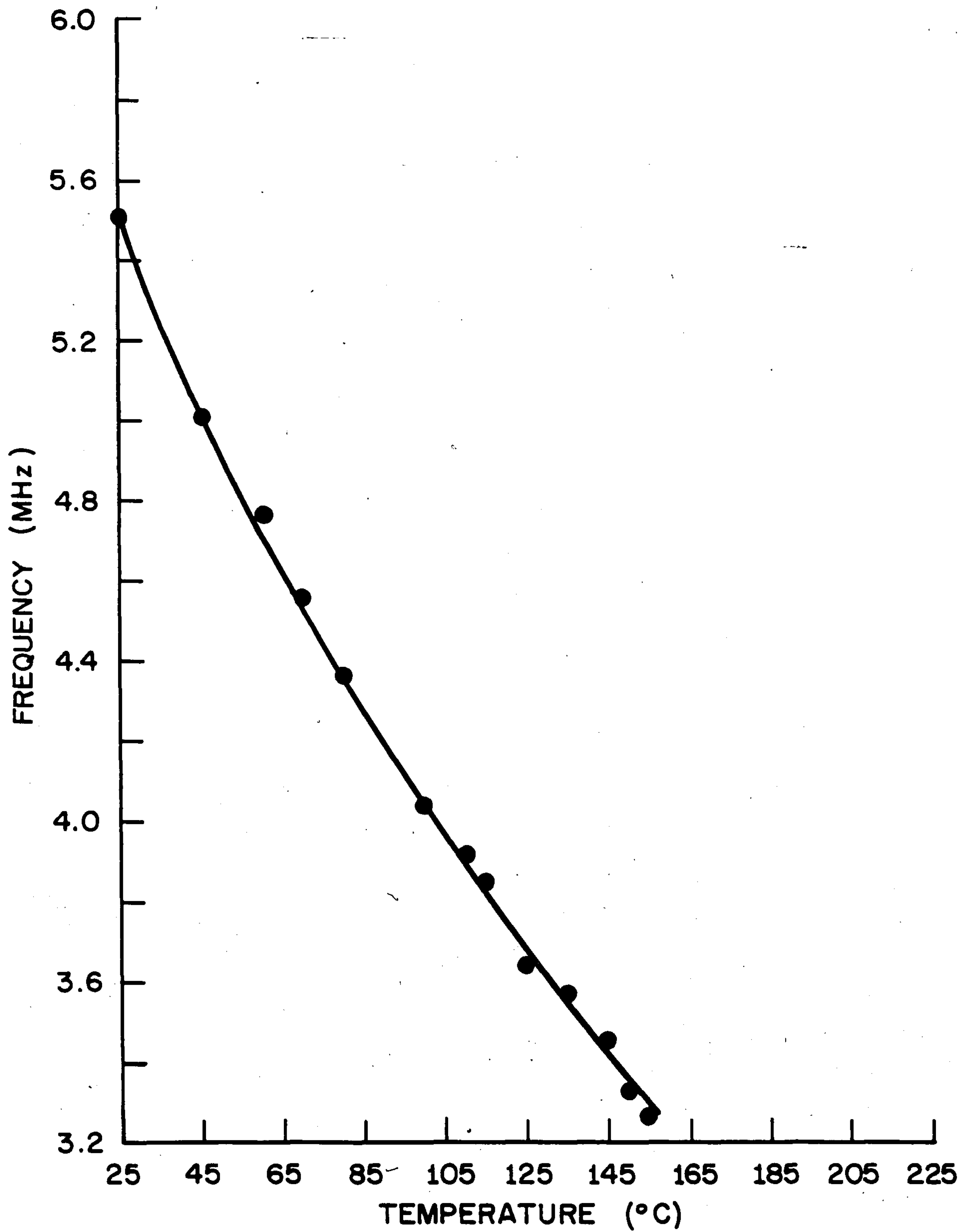


SUBSTRATE BIAS GENERATOR (VBB2)

FIGURE 4

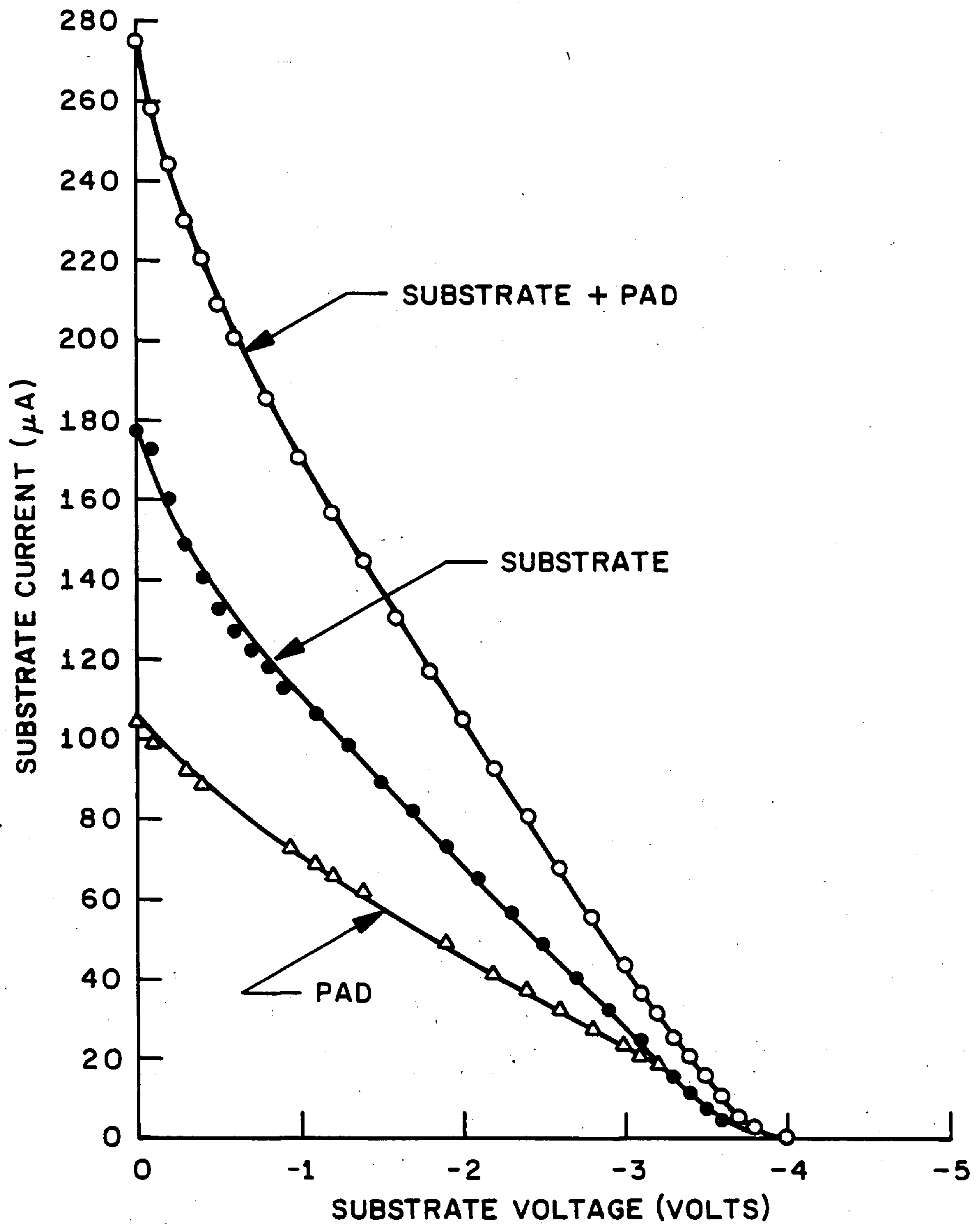


BLOCK DIAGRAM OF SUBSTRATE BIAS GENERATOR ON 2K X8 STATIC RAM
FIGURE 5

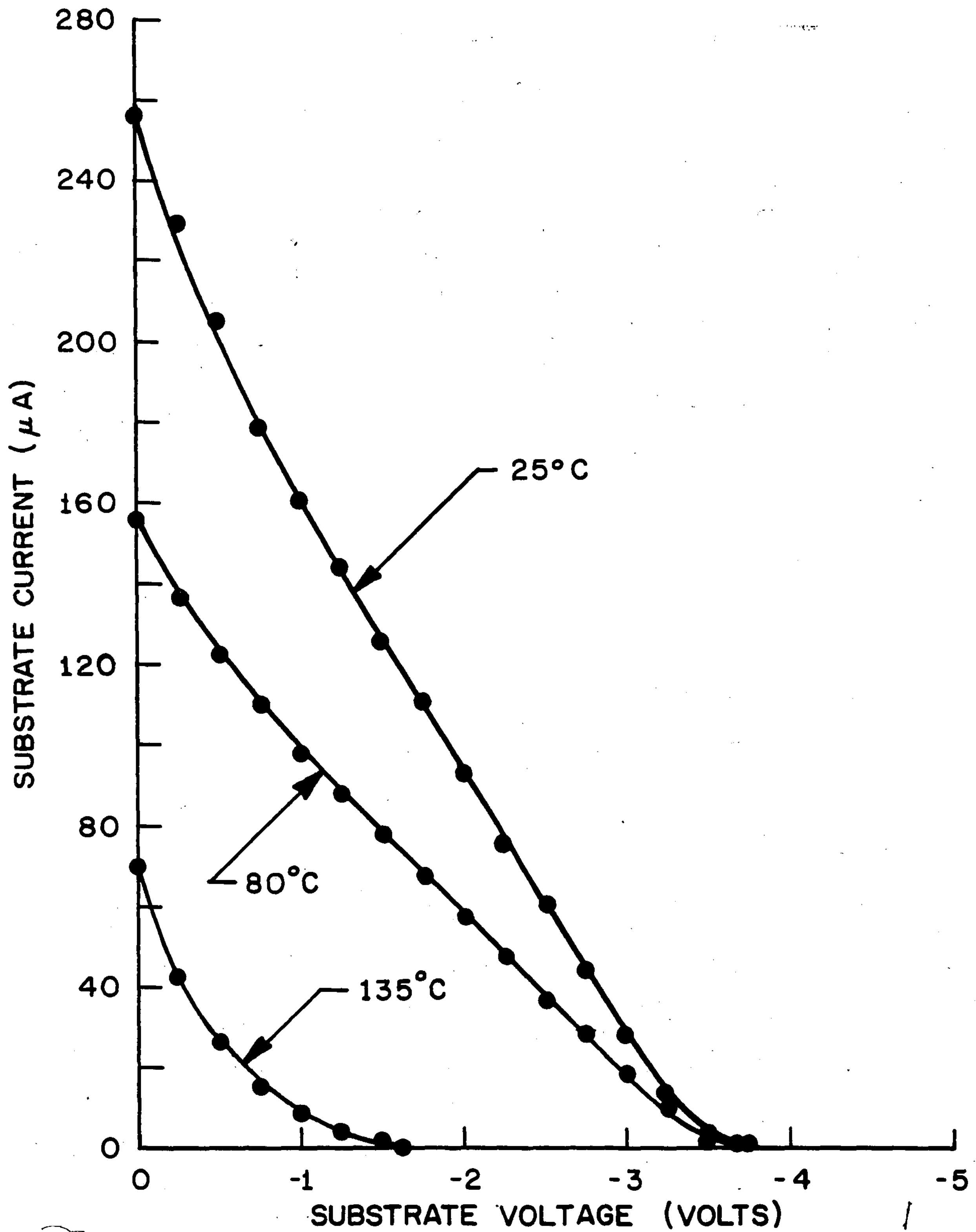


V_{BB} OSCILLATOR FREQUENCY VS TEMPERATURE

FIGURE 6

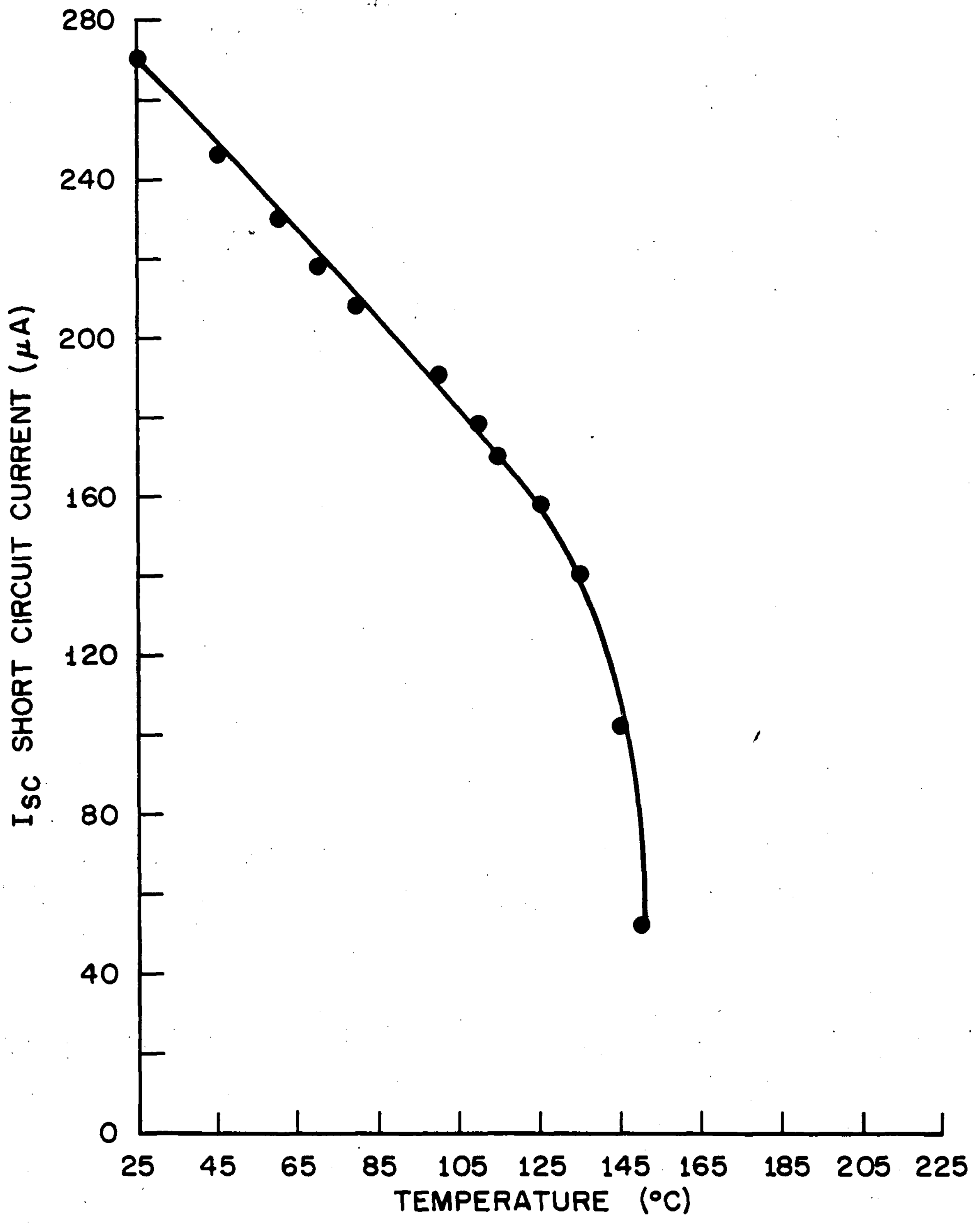


TYPICAL I—V CHARACTERISTICS
OF SUBSTRATE—BIAS GENERATOR
FIGURE 7



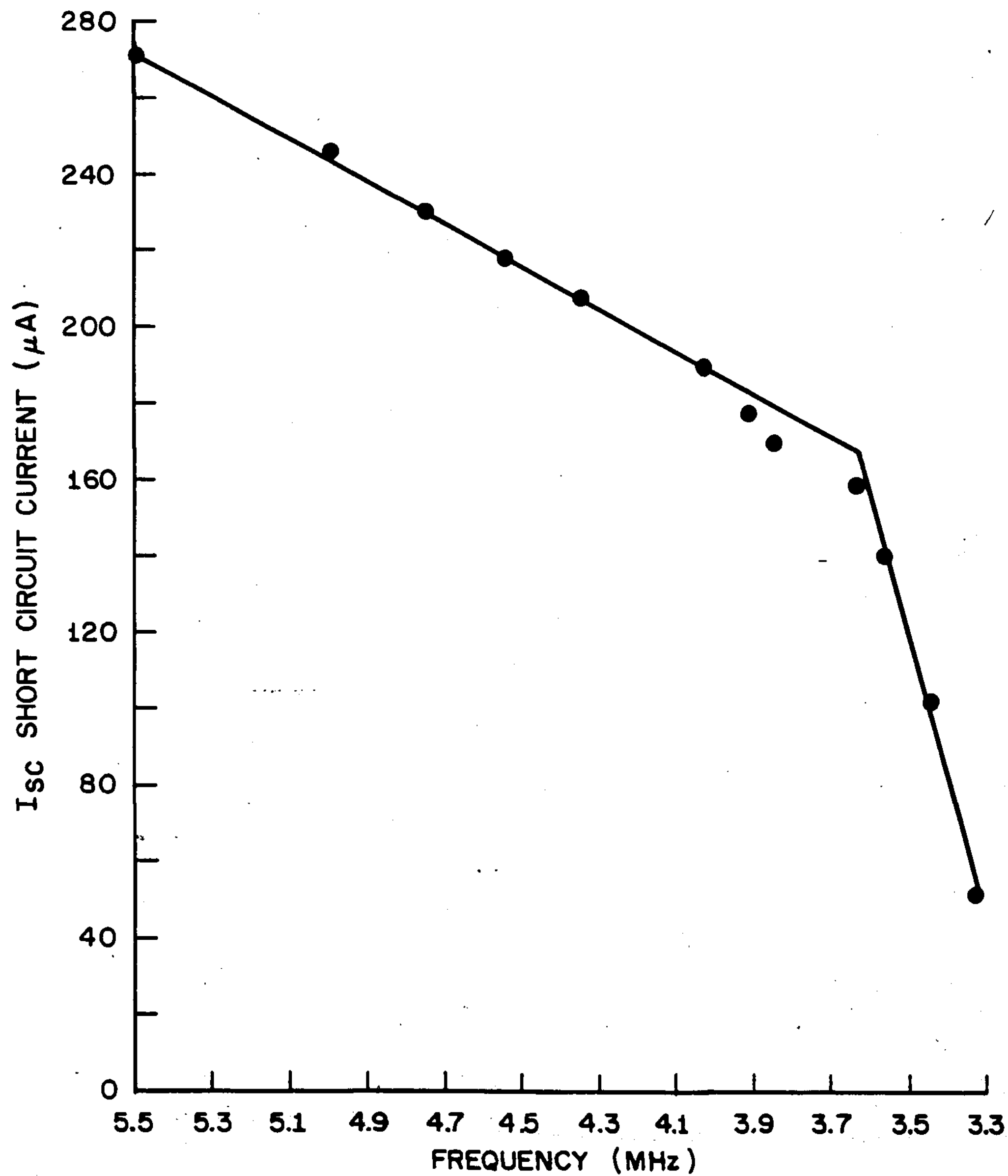
I-V CHARACTERISTICS
AS A FUNCTION OF TEMPERATURE

FIGURE 8



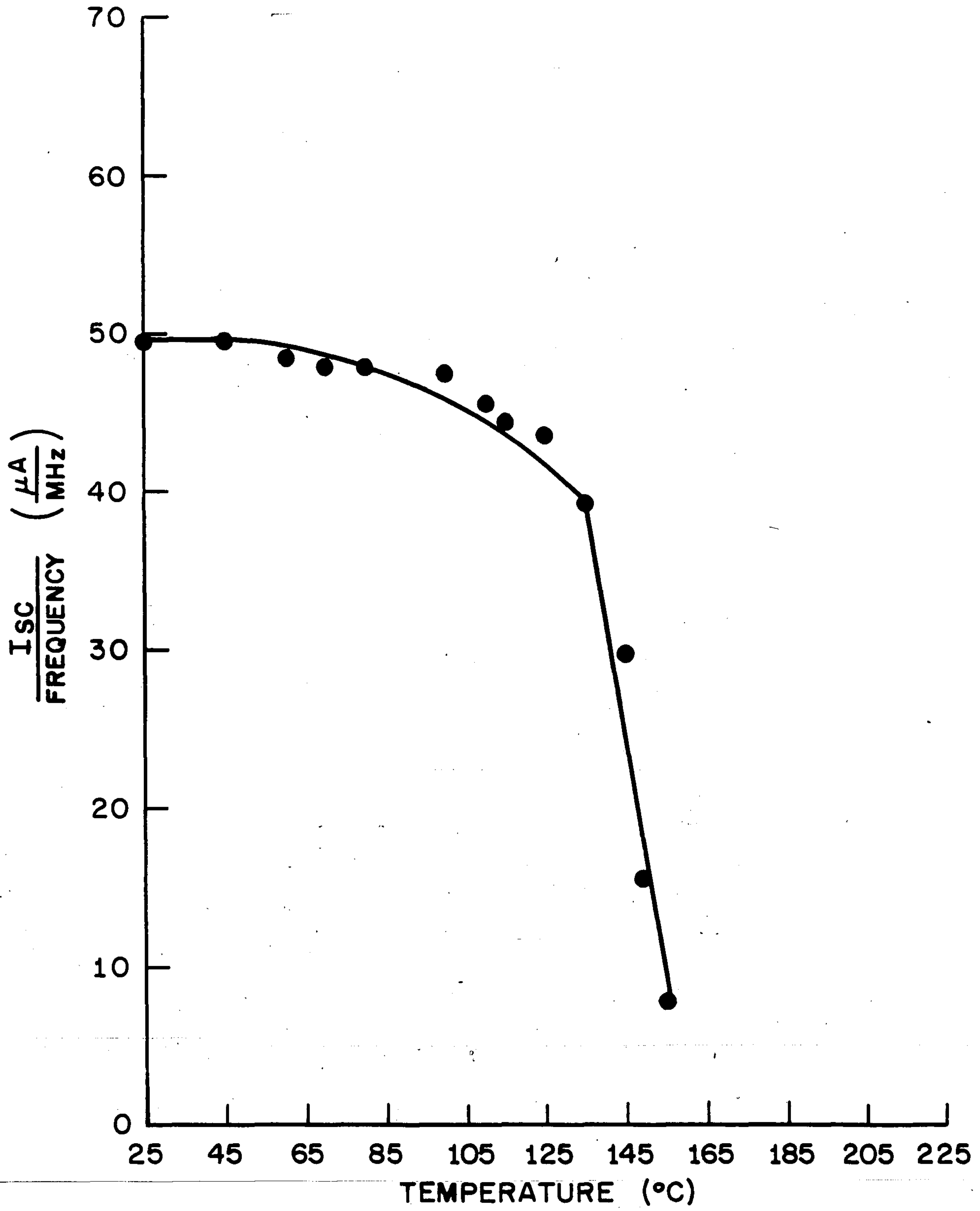
SHORT-CIRCUIT CURRENT VS TEMPERATURE

FIGURE 9



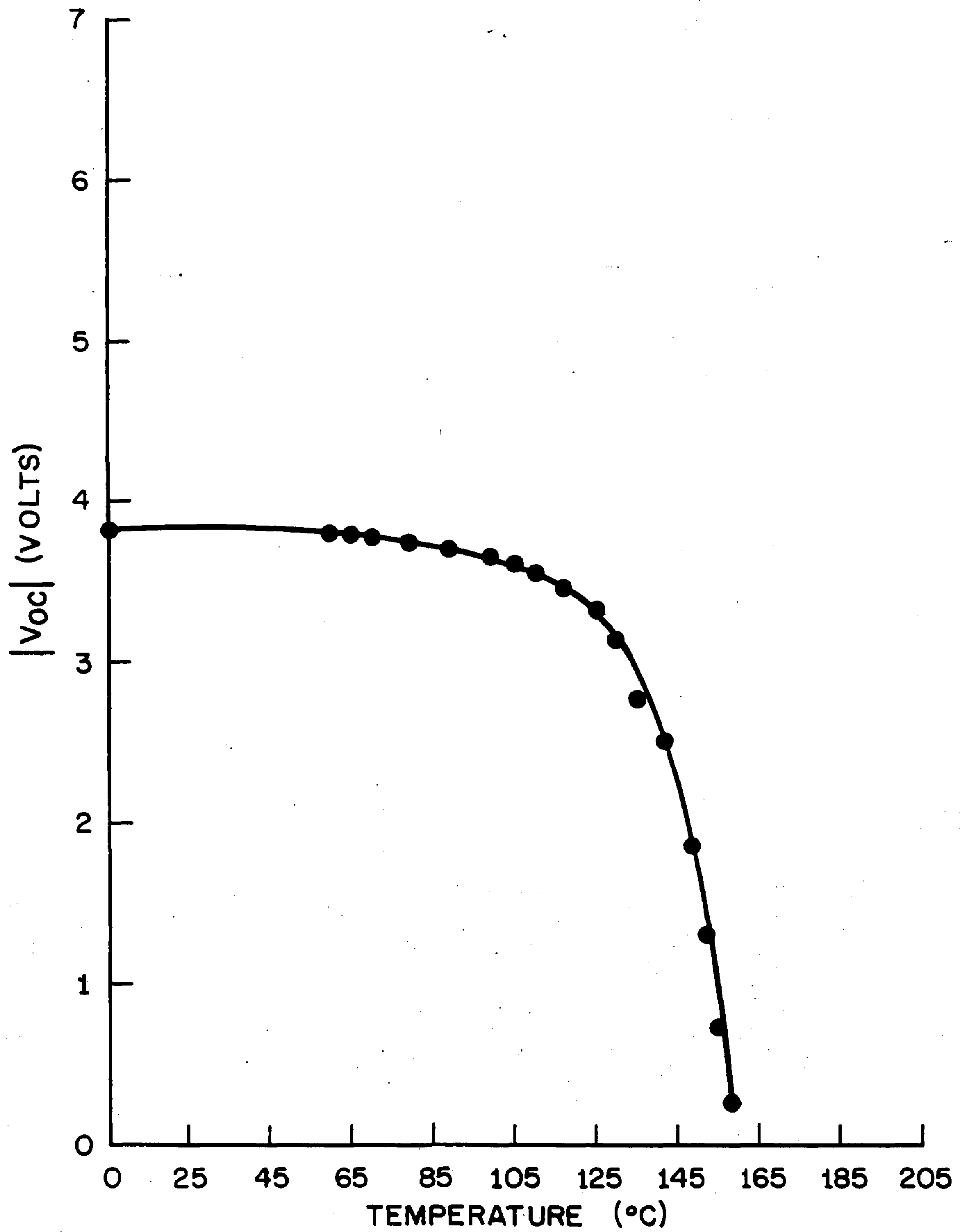
SHORT-CIRCUIT CURRENT VS FREQUENCY

FIGURE 10



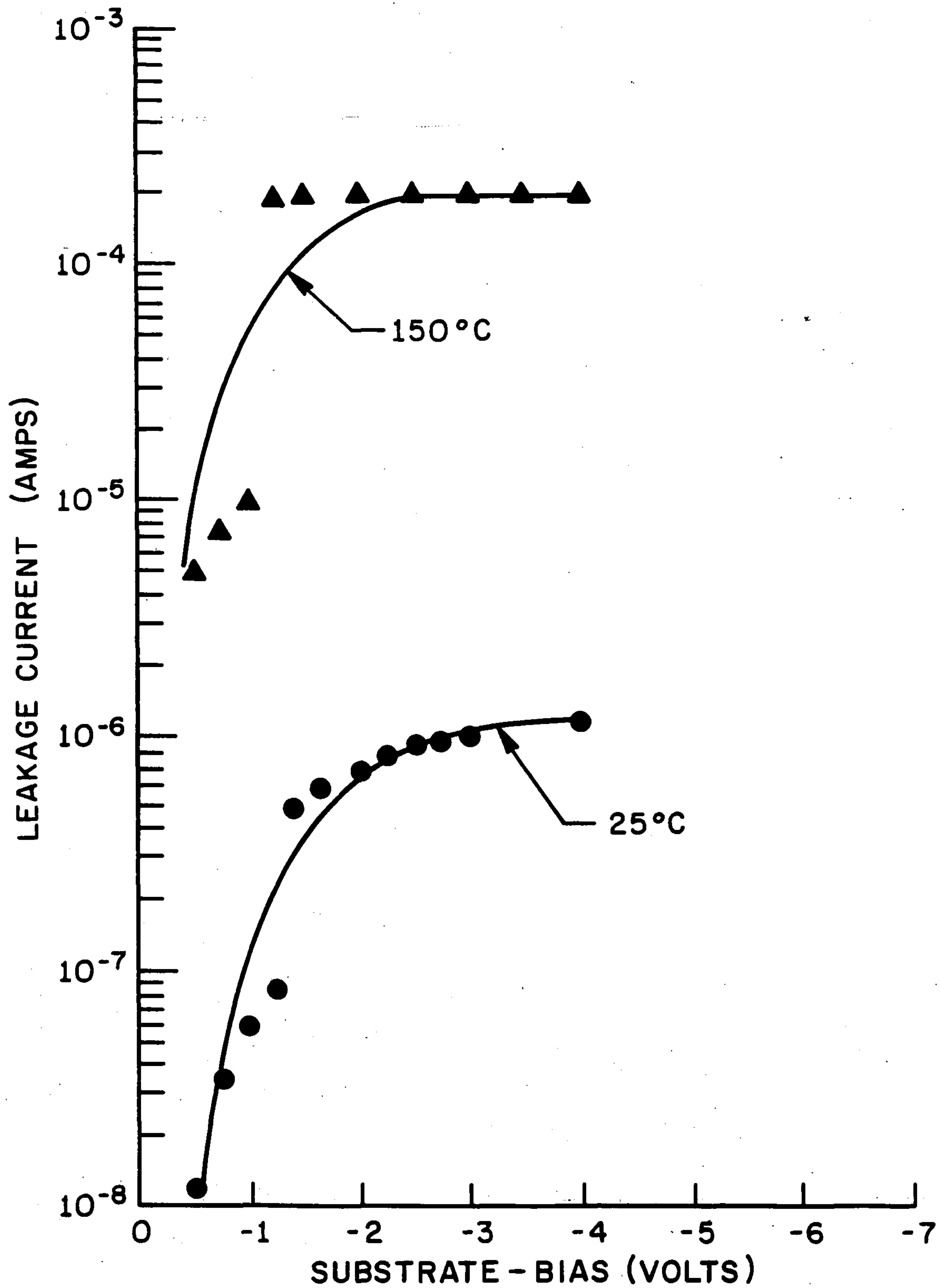
SHORT-CIRCUIT CURRENT / FREQUENCY VS TEMPERATURE

FIGURE 11



OPEN CIRCUIT VOLTAGE VS TEMPERATURE

FIGURE 12



TYPICAL LEAKAGE CURRENT OF THE V_{BB} GENERATOR AS A FUNCTION OF SUBSTRATE-BIAS VOLTAGE

FIGURE 13

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APPENDIX

Threshold Voltage

Threshold voltage can be written as

$$V_{th} = - \frac{Q_{SS} + Q_D}{C}$$

where Q_{SS} = effective surface-state charge density per unit area

Q_D = bulk charge per unit area associated with the channel depletion region

C = capacitance of the gate to channel per unit area

The physical interpretation of the above equation is that V_{th} is the gate voltage required to neutralize, in effect, the immobile charge above and below the channel region. Any additional gate voltage over and above $|V_{th}|$ will produce a gate charge that must be neutralized by an equal amount of mobile channel charge. The charge above the channel is Q_{SS}, while the charge below the channel consists of that within the depletion region located in the bulk (Q_D).

Q_D = depletion region thickness (X_D). Substrate charge density (ρ).

$$Q_D = \sqrt{\frac{2\varepsilon_S \phi_S}{qN}} \; qN \quad \frac{\text{coulomb}}{\text{cm}^2}$$

where $\phi_S = 2\,\phi_F$ and $\phi_F = \dfrac{E_F - E_i}{q}$

$$Q_D = \sqrt{2q\varepsilon_S N} \; \sqrt{2\,\phi_F}$$

where $N = N_D$ for an N-type substrate device

$N = N_A$ for a P-type substrate device.

The voltage on the gate necessary to support this charge is the intrinsic threshold voltage,

$$V_{Ith} \equiv \frac{Q_D}{C} = -K_1 \sqrt{2\,\phi_F}$$

where $K_1 = \pm\,(t_{ox}/\varepsilon_{ox}) \sqrt{2q\varepsilon_S N}$ (+ for P channel, - for N channel).

VITA

Mr. Dimitris C. Pantelakis was born in Kampala, Uganda on October 4, 1951, the son of Mr. and Mrs. Peter Pantelakis. He graduated from Old Kampala High School, Kampala, Uganda in December, 1970. He received an Associate Degree in Electrical Technology from Lehigh County Community College in June, 1976. He graduated with a Bachelor of Technology Degree in Electrical Engineering from Pennsylvania State University in December, 1977. Since December of 1977 he has worked at Bell Telephone Laboratories. He is currently a member of the Memory Design Department designing integrated circuits. He and his wife, the former Neema Nasser of Kampala, Uganda and their two children, Dimitris and Damon, reside in Whitehall, Pennsylvania.