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A STROBED DATA OUTPUT BUFFER FOR A 2K X 8 STATIC NMOS RANDOM ACCESS MEMORY

by

Michael V. DePaolis, Jr.

A Thesis

Presented to the Graduate Committee

Of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

1980

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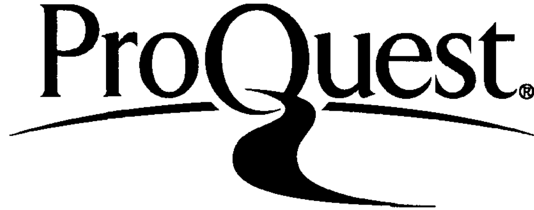

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This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

Nov. 20, 1980
Date

Professor in Charge

Chairman of the Department

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ABSTRACT

A Strobed Data Output Buffer for a 2K X 8 Static NMOS RAM has been developed. A novel application of dynamic memory techniques to a static memory design resulted in an overall improvement in the speed-power product. An analysis of the circuit is presented, as well as design considerations, circuit simulations, and experimental results. The output buffer provides valid output data 35 ns maximum after valid data appears on the internal I/O lines over the operating range of the memory. During a deselect mode, the data out circuitry consumes no more than 14 mW of power.

I. INTRODUCTION

Static Random-Access Memories (RAMs) have found increasing use in microprocessor-based operating systems. This application lends itself to an 8 bit byte-wide memory organization. The design and operation of a Strobed Data Output Buffer for a 2K x 8 Static NMOS RAM will be discussed. A block diagram of the memory is shown in Figure 1.

Data output from eight 2048 x 1 bit memory arrays must be buffered to off-chip circuitry. The requirements of the Data Output Buffer are that it should be able to drive the input of a low power TTL gate and 50 pf of capacitance. It must do this over the required range of system voltage, temperature, and processing variations. The circuit should also consume minimum power since eight buffers are required. A Data Output Buffer that meets these requirements is presented.

The complete Data Output Circuitry consists of a Data Output Strobe Circuit and a Data Output Buffer. The Data Output Strobe is a novel application of dynamic memory techniques to a static memory design. A design concept called "address transition activation"[1] allowed the use of strobed/dynamic circuitry while making the part look static to the user. Any address transition initiates a new cycle. The transition is detected and generates a signal which sets off a series of clock pulses. The series

of pulses are combined to provide a timing edge from which the data output strobe signal can be generated. A retriggerable monostable multivibrator guarantees a minimum duration precharge period before generating the strobe signal. This precharge period is used for charging dynamic nodes in the Data Output Circuit which are then "bootstrapped"[(2)] when the data output strobe signal is generated. The enhanced drive capability provided by the "bootstrapping" allows smaller size devices to be used than would have been possible using strictly static circuits. The result is circuitry that requires both less power and less area. All eight Data Output Buffers are controlled by a single Data Output Strobe Circuit. The Data Output Strobe Circuit contains all the control logic for the Data Output Buffers.

The results obtained can be applied to larger static memory designs where area, speed, and power are even more critical. The reduced area requirements and improved speed-power product of the Strobed Data Output Buffer would be valuable assets to a larger scale design.

II. THE MOS-BIPOLAR INTERFACE

The output buffer source and sink current design goals are:

Output "1" Level:

2.4V min @ 1mA

Output "0" Level:

0.4V max @ 3mA

The above figures represent the input level requirements for a low power TTL circuit. From a design standpoint the TTL requirements are the most stringent. MOS circuits require essentially no current source or sink capability from the output buffer. The actual design has included a 0.1V margin on both the "1" and "0" levels. For design, simulation, and testing purposes an equivalent resistive load network can replace the actual TTL input circuit. Two driver transistors are required in the output buffer, one driver to source current and one to provide a current sink. An effective on-resistance for each device can be calculated from the required currents and voltages. The system power supply specification is 5V ± 10% plus an additional ± 0.1V for end of life degradation. The V_{cc} minimum voltage is then 4.4V.

A basic TTL inverter circuit and a equivalent resistive circuit are shown in Figure 2. Note that when the sink driver is on the source driver is off and conversely. The

effective on-resistances are as follows:

$$R3 = \frac{4.4V - 2.5V}{(1 \times 10^{-3})A} = 1900\ \Omega$$

$$R4 = \frac{0.3V}{(3 \times 10^{-3})A} = 100\ \Omega$$

The equivalent source and sink current-voltage relations can be developed from the circuits shown in Figure 3. The equations describing the equivalent source and sink currents are:

Sink: $I_1 = 3 \times 10^{-3}A + I_2$

$$\frac{4.4V - .3V}{R1} = 3 \times 10^{-3}A + \frac{.3V}{R2}$$

Source: $I_4 = 1 \times 10^{-3}A + I_3$

$$\frac{2.5V}{R2} = 1 \times 10^{-3}A + \frac{4.4V - 2.5V}{R1}$$

Solve the simultaneous equations for R1 and R2. The results are:

$$R1 = 1{,}240\ \Omega$$

$$R2 = 980\ \Omega$$

Adding an external capacitance of 50 pf, results in the final equivalent circuit of a TTL input shown in Figure 4. The 50 pf of load capacitance is an industry standard to represent package, fixture and device capacitive loading. This circuit was used for all design and simulation work.

A Thevenin equivalent resistive circuit was included in a bench test set used for testing the 2K x 8 RAM. The Thevenin equivalent resistance is simply R1 in parallel with R2 or 547 ohms. The Thevenin voltage source is determined by the following expression:

$$V_{Thevenin} = V_{cc} \times \frac{980}{980 + 1240}$$

If $V_{cc} = 4.4V$:

$$V_{Thevenin} = 1.94V$$

The resulting circuit is only a single resistor in series with a voltage source. One side of the resistor is tied to a RAM data in/data out lead.

III. LOGIC FUNCTIONS OF DATA OUT CIRCUIT

The 2K x 8 Static RAM uses eight common Input/Output (I/O) lines. That is, data both inputs and outputs on the same lead for each I/O section. It is, therefore, necessary to control the states of the data out buffer into three catagories:

1) Pull-up transistor on; Pull-down transistor off; Reading a "1".
2) Pull-up transistor off; Pull-down transistor on; Reading a "0".
3) Both pull-up and pull-down transistors off. Output tri-stated.

In the tri-state mode the data input being applied will only encounter a reverse biased P-N junction instead of active devices pulling high or low. The state of the output buffer is directly controlled by the following three circuit functions:

1) CEB ($\overline{\text{Chip Enable}}$) - This function deselects the entire memory, except the array, resulting in a power savings in standby condition. The output buffer must be tri-stated in this mode.
2) CS (Chip Select) - The chip select function keeps the output buffer tri-stated and prevents writing of the memory. Fast access is available upon reselection.

3) OEB ($\overline{\text{Output Enable}}$) - This function provides fast access and keeps the output buffer tri-stated.

Figure 5 shows the logic diagram of a basic output buffer and the corresponding truth table.

IV. DESIGN CONSIDERATIONS

A. Driver Device Sizes

The 2K x 8 memory organization requires eight data output buffers. The current and voltage drive specification for the output drivers requires them to be rather large. From the following equations[3] for MOS transistors drain current, the minimum size driver transistors can be calculated to meet the quiescent I-V specifications:

1. $$I_D = \beta[(V_{GS} - V_T)\ (V_{DS}) - V_{DS}^2/2]$$

For $|V_{GS} - V_T| > |V_{DS}|$

2. $$I_D = \frac{\beta}{2}[V_{GS} - V_T]^2$$

For $|V_{GS} - V_T| \leq |V_{DS}|$

and: $$V_T = V_{FB} + 2\phi_f + \frac{Q_g}{C_{ox}}$$

where V_{FB} is the flat band voltage, $2\phi_f$ is the total band bending, and Q_g/C_{ox} is the bulk voltage due to depletion and fixed charge, and:

$$\beta = \frac{\mu\ C_{ox}\ W}{L}$$

where μ is the electron mobility in the channel, C_{ox} is the gate capacitance per unit area, W is the channel width,

and L is the effective channel length.

By considering temperature variations (0°C→ 85°C), and process variations, the minimum size pull down transistor can be calculated as follows:

I_{DS} = 3 mA @ 0.3V (guard banded)

V_{DS} = 0.3V

V_{GS} = 4.4V (V_{cc} minimum)

V_T = 1.3V (maximum)

$$|V_{GS} - V_T| > |V_{DS}|$$

$$I_D = \beta[(V_{GS} - V_T)\ (V_{DS}) - V_{DS}^2\ /2]$$

$$3 \times 10^{-3}A = \beta[(4.4V - 1.3V)\ (0.3V) - \frac{(0.3V)^2}{2}]$$

β min. = 3,300 μmho/V

If $\mu\ C_{ox}$ = 15.2 μmho/V (@ 85°C) and L = 2.4 μm (max.)

then:

$$W = \frac{(3300)\ (2.4)}{15.2} = 521\ \mu m$$

If we assume that the actual process technology requires a photo-lithographic channel length of 3 μm printed

for an effective 2 μm nominal channel, then the minimum device gate area will be:

$$A_{gate}\ (min) = (3\ \mu m)\ (521\ \mu m)$$
$$= 1563\ \mu m^2$$

The calculated gate area corresponds to an approximate gate capacitance of 1 pf. The driver gate capacitance is important since it is reflected back to the preceding control logic circuitry. The control logic circuitry must charge and discharge this capacitance within the timing specifications.

B. Timing and Power

The design goal for data output buffer timing was to provide valid output data 35 ns after valid data appeared on the internal I/O lines. This timing specification had to be met at V_{CC} = 4.4V, Temp. = 85°C, and worst case processing.

Another design restriction was that, during a deselect mode, all data out circuitry consume no more than 14 mW of power. The power specification had to be met at V_{CC} = 5.6V, Temp. = 0°C, and best case processing. This combination of parameters represents the worst case power condition for the RAM. The low power consumption requirement dictated the need for consolidation of data output logic control functions. Obviously repeating the output control logic

circuitry eight times would greatly increase the power consumption. It was decided that a single central logic control circuit could be used to control eight simplified data output circuits.

The data output circuit only accepts the internal I/O line information and a control signal from the one logic control circuit. As discussed in the introduction, the transition activated circuitry used in this memory provided a convenient timing reference for controlling the output logic. Implementing the data out circuitry with purely static techniques would require large devices with high power dissipation to drive the capacitive loading of the output drivers. The timing reference pulse allowed dynamic memory circuit techniques to be used which improved the speed-power product in the active mode and minimized the standby power.

C. Process Technology

The fabrication process is basically a single level polysilicon gate, n-channel technology. Ion implantation techniques are used to control device thresholds (V_T), field region thresholds, and source/drain doping. The single level polysilicon is selectively doped to produce both high resistivity load resistors in the memory cells plus low resistivity runners and gates. The integrated circuits were fabricated on the Western Electric - Allentown MOS process line.

V. STROBED DATA OUTPUT BUFFER

A. Memory Read Operation

A brief description of a read operation is necessary to the understanding of the data output buffer circuitry. Refer to the system block diagram Figure 1. Binary row and column address information is decoded. The decoded address signals select data from eight 2048 x 1 bit memory arrays. Transition detection circuitry provides a series of internal clocks which are used to:

1) Recover the bit lines to one threshold below V_{cc}.
2) Precharge and strobe the bit and word decoders.
3) Strobe the sense amplifiers.
4) Strobe the data output circuits.

When a row or column address transition is detected, a retriggerable monostable multivibrator provides a guaranteed delayed strobe pulse to the sense amplifier and data output circuits.

The sense amplifier is a depletion-load cross-coupled flip-flop which is connected directly across each pair of internal I/O lines. The sense amplifiers are enabled by the Sense Amplifier Strobe (SASTR) signal. The SASTR signal is only generated after a fixed delay which is timed from a valid row and column selection. During the delay period, the internal I/O lines are recovered to V_{cc} potential

through the sense amplifier depletion loads and the selected data is impressed on the I/O lines. After the fixed delay the sense amplifiers are strobed "on" and full MOS signals are developed on the I/O lines. The data on the eight pairs of I/O lines is routed to its respective Data Output Buffer.

B. Data Output Circuitry

The complete circuitry required for the data output function is composed of a Data Output Strobe Circuit and eight Data Output Buffers. A block diagram of the output circuitry is shown in Figure 6. Note that the Data Output Strobe Circuit (DOSTR) receives control signals from the sense amplifier strobe, CEB, OEB, and CS. The DOSTR signal is a function of all these controls. That is, the memory must be:

1) Enabled (CEB low)
2) Selected (CS high)
3) Output Enabled (OEB low)
4) Sense amplifier must be strobed (high) - read mode.

before a DOSTR signal is generated. DQ0 through DQ7 are the common I/O lines in and out of the integrated circuit.

C. Data Output Strobe Circuit

The Data Output Strobe Circuit is shown in Figure 7. Five control signals are applied to this circuit. Complementary signals CE3 and CE3B are used for powering down the

circuit when the memory is not selected. Devices Q1, Q8, and Q10 are special lightly implanted depletion type devices which are only slightly conducting when their gates are at V_{SS} potential. They improve the overall speed-power product of the memory. Driver transistors Q4 and Q13 assure that critical gate nodes are held low so that standby current is minimized. The SASTR signal is applied to the gate of device Q3. The SASTR signal inhibits the DOSTR signal until a valid read condition occurs.

A normal MOS level discriminating inverter such as depletion load device Q2 and enhancement driver device Q3 have a beta (β) ratio of 4. That is:

$$\frac{\beta_D}{\beta_L} = 4$$

Power down device Q1 has a β of twice that of Q2's.

The $\overline{\text{Output Enable}}$ (OEB) signal originates directly from external circuits which may be TTL or MOS levels. A ten to one beta ratio inverter consisting of Q6 and Q9 transforms OEB TTL levels to full MOS levels at Node 4.

The $\overline{\text{Chip Select}}$ (CSB) signal is a full MOS level signal generated at the CS buffer. The CSB signal is applied to the gate of Q7 in the DOSTR circuit. Enhancement driver devices Q5, Q6, and Q7 along with depletion load device Q9 provide a logical NOR function. Both OEB and CSB must be logic "0"'s to allow the DOSTR signal to occur.

Power staging is performed with enhancement devices Q12 and Q13 together with depletion load devices Q11 and Q14. The device sizes were chosen to drive the runner and gate capacitance of eight Data Output Buffers. Device Q16 is an enhancement driver device with its gate driven by Node 2. The reason for this is to provide fast pull down of the DOSTR signal when SASTR goes low.

A Data Out Tri-State (DOTS) signal is generated along with the DOSTR signal. The purpose of the DOTS signal is to keep the data output drivers tri-stated (high Z) until a DOSTR signal is generated. DOTS is the complement of DOSTR.

D. <u>Data Output Buffer</u>

A schematic of one of the eight Data Output Buffer (DOBUF) circuits is shown in Figure 8. The DOSTR signal is connected to the common source (drain) node of devices Q26 and Q27. A DOBUF is connected directly across each pair of internal I/O lines (IO and IOB). During a read cycle either the I/O or the I/O bar line will go low (both are normally high). Either Node 7 or 8 will remain high, depending on the data. The transition detection circuitry always insures that both of the I/O lines stay high long enough to precharge Nodes 7 and 8 through low gain devices Q19 and Q20.

The DOSTR signal remains low until a valid read condition occurs and the SASTR signal is developed. The DOSTR

signal then goes high and is capacitively coupled to Node 7 or 8 through the gate overlap capacitance of device Q26 or Q27. The node that was high (7 or 8) will be "bootstrapped" to a voltage higher than Vcc for a time period determined by the sub-threshold leakage of device Q19 or Q20 and the node capacitance of Node 7 or 8. The junction leakage of Node 7 or 8 also contributes to the loss of charge. The total voltage can be expressed by:

Assume Node 7 was high -

$$\text{Original voltage} = V_{CC} - V_T = V_7$$

$$\text{or } V_{CC} - V_T = \frac{Q_7}{C_7}$$

$$\text{New voltage} = \frac{Q_7 + \Delta Q}{C_7}$$

where Q_7 is the charge at Node 7, C_7 is the capacitance at Node 7, and ΔQ is "bootstrapped" charge. A nominal "bootstrapped" node voltage is about 7.5 V (V_{CC} = 5V). Device Q26 or Q27 is turned on hard; which, in turn, raises the gate voltage of either Q31 or Q32 to the DOSTR level (V_{CC}). The added "bootstrapping" effect allows the large size output driver devices, Q31 and Q32, to be turned on within the required response time using relatively small driver transistors.

The "bootstrapped" node voltage eventually decreases to $V_{CC} - V_T$. At this time small depletion load devices,

Q23 or Q29, hold the driver gate potential at V_{cc}. Enhancement driver devices, Q24 and Q30, are connected in a cross-couple arrangement that keeps the unselected output driver device turned off. Devices Q25 and Q28 keep the output drivers turned off during a write mode when the internal I/O lines are changing levels. Devices Q18, Q21, and Q22 have their gates driven by CE3B. During the deselect mode, CE3B goes high and turns on these enhancement type drivers. They maintain critical nodes at V_{ss} potential to minimize standby power dissipation.

Q32 provides "0" level drive capability of 3mA @ 2.4v and Q31 provides "1" level drive capability of 1mA @ 0.4v.

VI. CIRCUIT PERFORMANCE

A. Design Evaluation

Circuit performance was evaluated by a Bell Laboratories proprietary version of a computer circuit analysis program called SPICE[4]. The circuit was simulated over the operating temperature range of 0°C to 85°C and V_{cc} power supply range of 5V ± 10%. The various processing parameters were also varied over their expected ranges for simulation purposes.

The circuit was optimized, using SPICE, to meet the required design goals before actually laying out the integrated circuit. The predicted performance parameters are listed in Table 1.

The circuit layout was done using an interactive layout design aid. Each device in the circuit was layed out individually to minimize parasitic capacitance on circuit nodes. The output driver devices were placed as close as possible to the bond pads to minimize voltage drops and metal runner widths.

B. Measurements

Actual 2K x 8 Static RAM integrated circuits were fabricated using the Strobed Data Output Buffer circuit. A manual bench test set was used to verify the design. The $\overline{\text{Output Enable}}$ (OEB) signal only goes to the DOSTR circuit and therefore provides a convenient timing reference for evaluating the output circuit performance.

The OEB access time was measured over the operating temperature range and V_{cc} power supply range. The measured OEB access time Vs temperature is shown in Figure 9. Figure 10 shows the OEB access time Vs V_{cc}. A noted increase in OEB access time (Figure 9) can be seen as the temperature is increased. This is due to a reduction in gain of the MOS transistors. As previously shown, the β of a device is a function of the electron mobility (μ). The mobility decreases with temperature in proportion to $T^{-2.5}$.

The equivalent TTL resistive load circuit was used for evaluating the Data Output Buffer "1" and "0" voltage levels. Figure 11 shows the output "1" and "0" levels as a function of V_{cc}. A greater effect of V_{cc} variation can be seen on the "1" level because a "1" is pulled toward the varying voltage. A secondary effect is that the pull-up transistor is always operating in the saturation region ($|V_{GS} - V_T| \leq |V_{DS}|$) where the drain current varies as the square of the gate to source voltage. Figure 12 shows the output "1" level as a function of temperature from 0°C to 85°C. The "0" level variation with temperature is shown over the same range in Figure 13. Both plots were obtained with V_{cc} supply at 4.5 volts. A slight degradation in both output levels can be seen over the temperature range. This effect is due to the mobility reduction associated with increasing temperature.

VIII. CONCLUSIONS

A Strobed Data Output Buffer for a 2K x 8 Static NMOS RAM has been designed and fabricated. Dynamic memory "bootstrapping" techniques were applied to a static design resulting in a fast, low power circuit. Design goals were met over the operating range of the RAM. Integrated circuits, that used this output buffer, were fabricated and characterized.

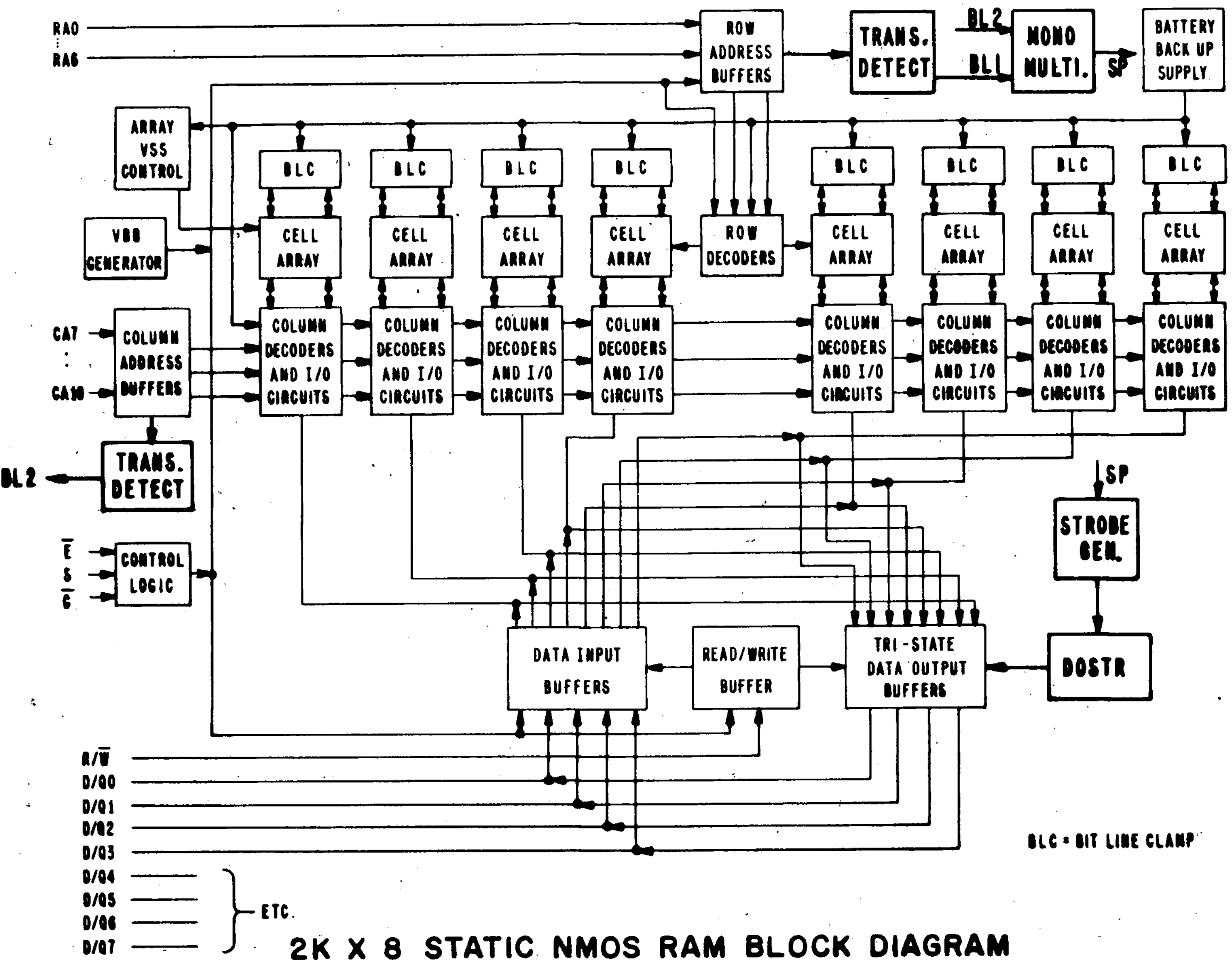
TABLE 1

SIMULATED CIRCUIT PERFORMANCE

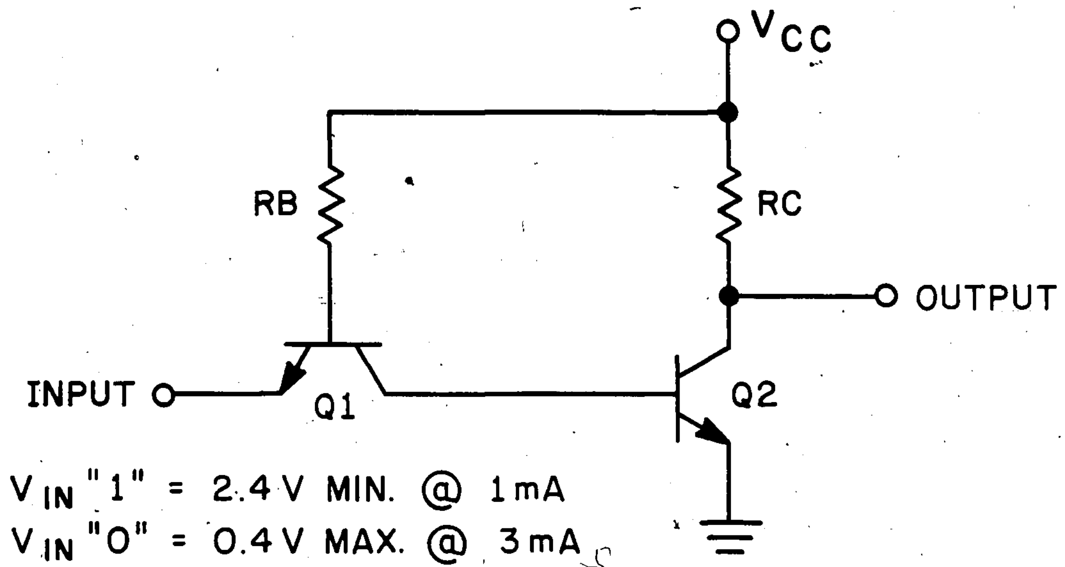
Vcc	Process	Temp.	Simulated Valid Data Time from Internal I/O Change
5.0V	Nominal	25°C	17 nsec
4.4V	Worst	85°C	35 nsec
5.6V	Best	0°C	10 nsec
			Standby Power
5.6V	Best	0°C	7.28 mW

NOTE: Worst Case Processing = High V_T
Low Mobility
Highest Node Capacitance

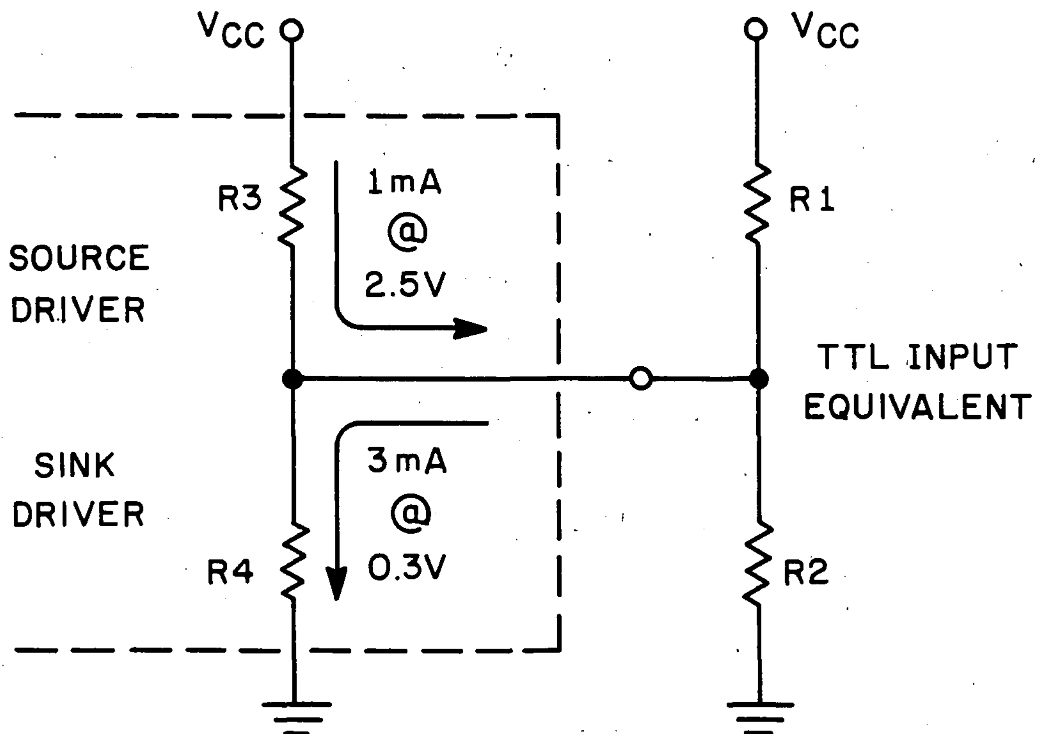
Best Case Processing = Low V_T
High Mobility
Lowest Node Capacitance



2K X 8 STATIC NMOS RAM BLOCK DIAGRAM
FIGURE 1

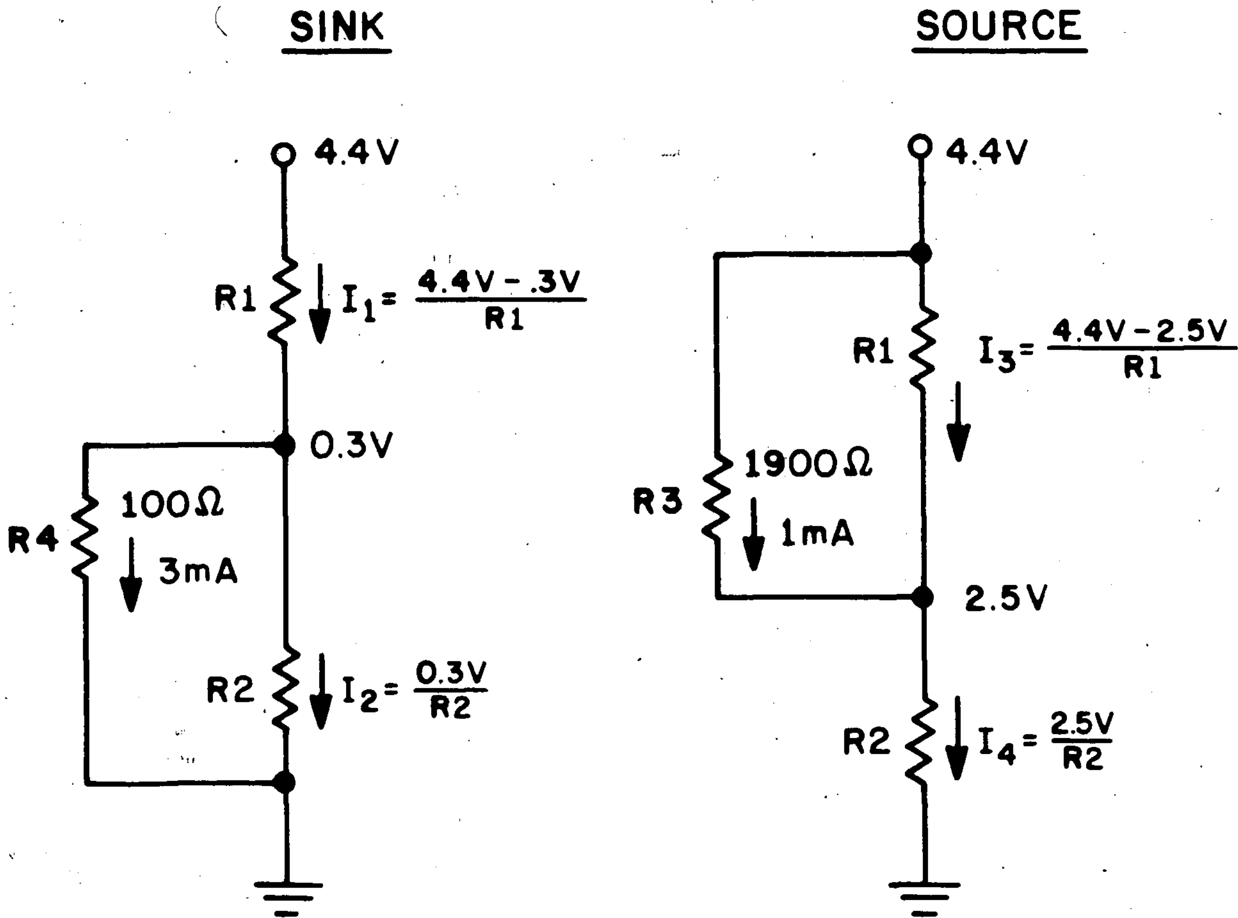


TTL INVERTER



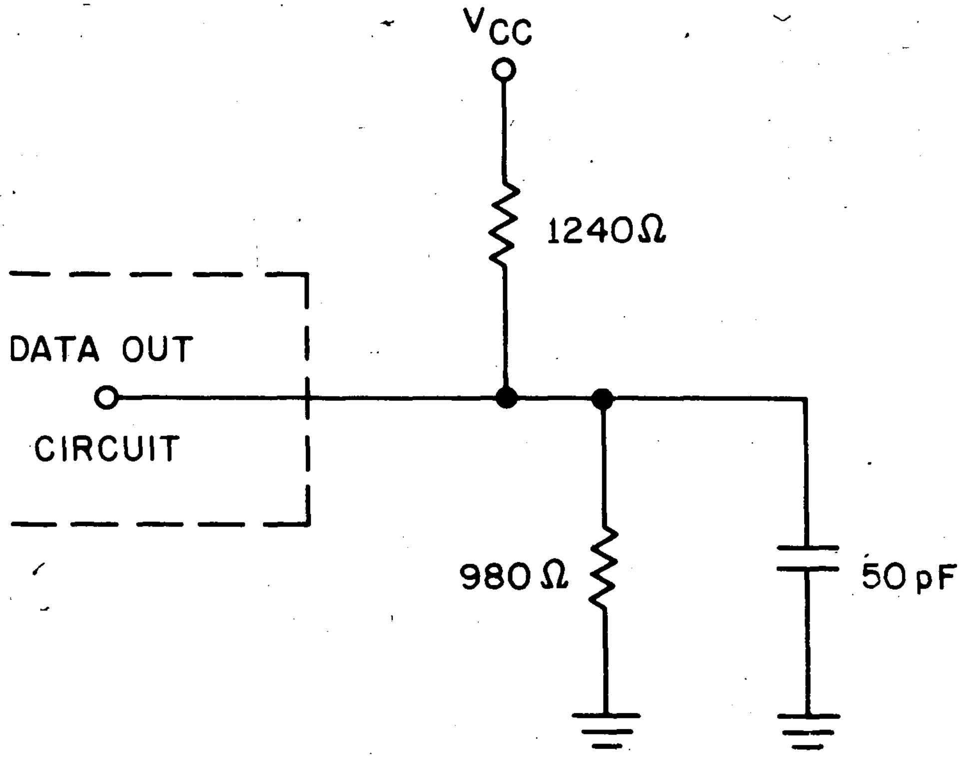
RESISTOR EQUIVALENT CIRCUIT

FIGURE 2



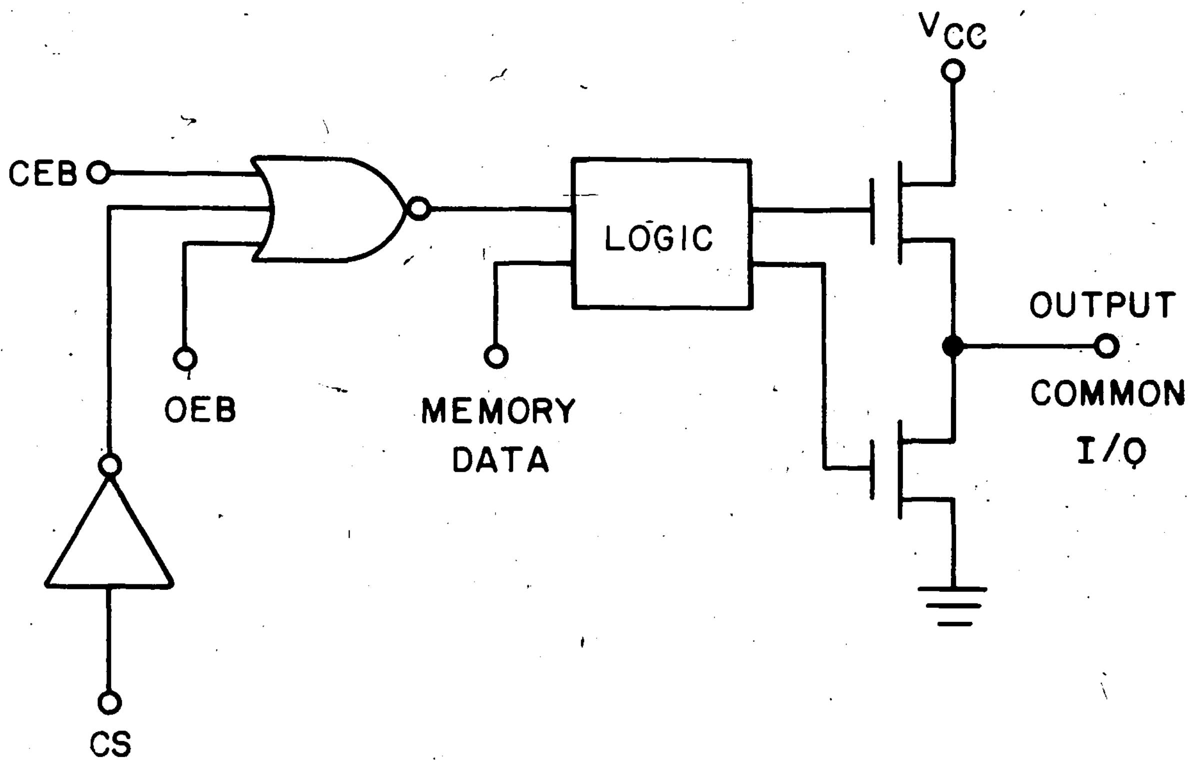
SOURCE AND SINK EQUIVALENT CIRCUITS

FIGURE 3



EQUIVALENT TTL INPUT

FIGURE 4

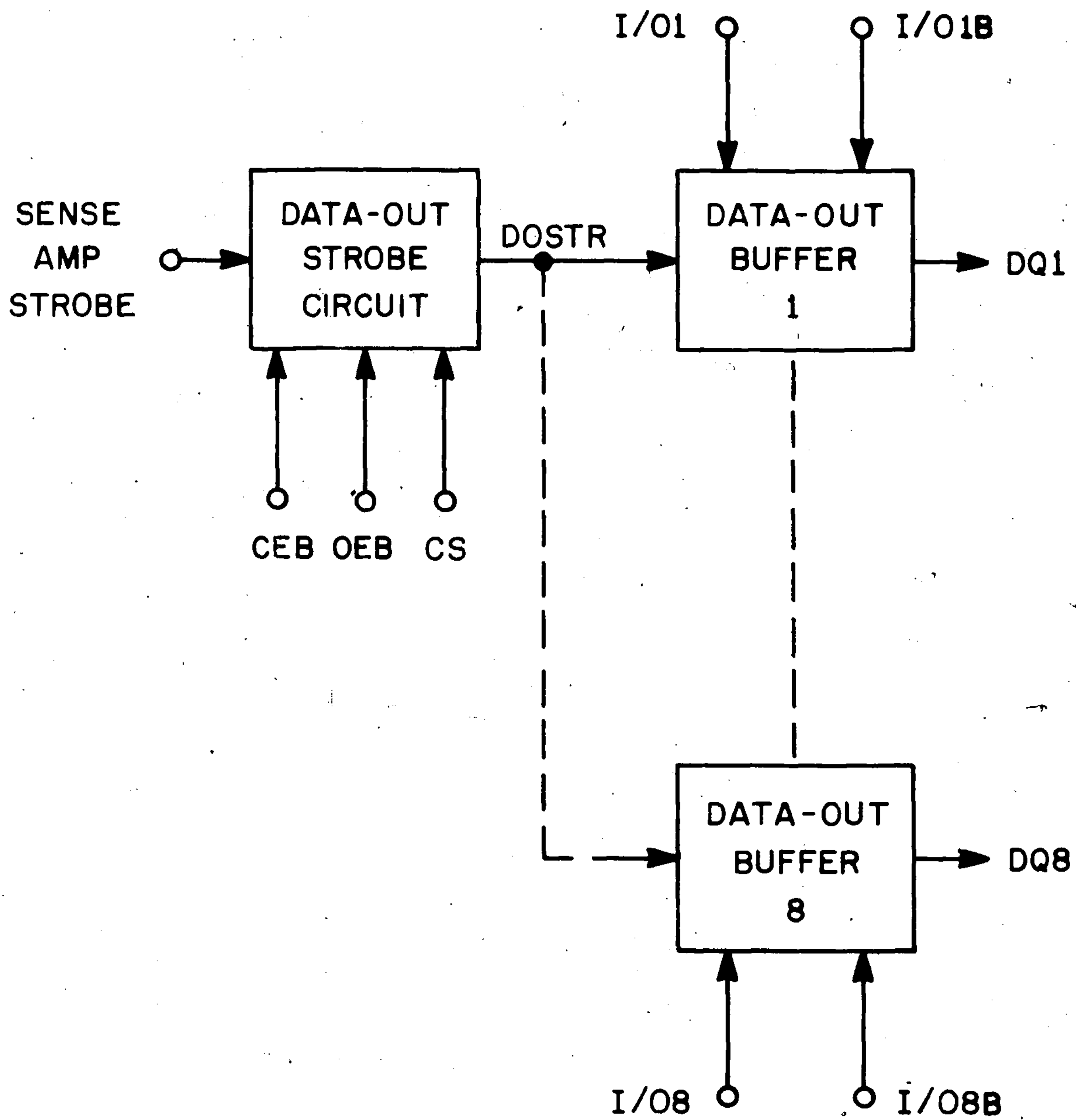


MEMORY DATA	CEB	CS	OEB	OUTPUT
1	0	1	0	1
0	0	1	0	0
X	1	X	X	Hi - Z (TRI STATE)
X	X	0	X	Hi - Z (TRI STATE)
X	X	X	1	Hi - Z (TRI STATE)

(X = DON'T CARE)

OUTPUT BUFFER LOGIC DIAGRAM

FIGURE 5



DATA OUT BUFFER BLOCK DIAGRAM

FIGURE 6

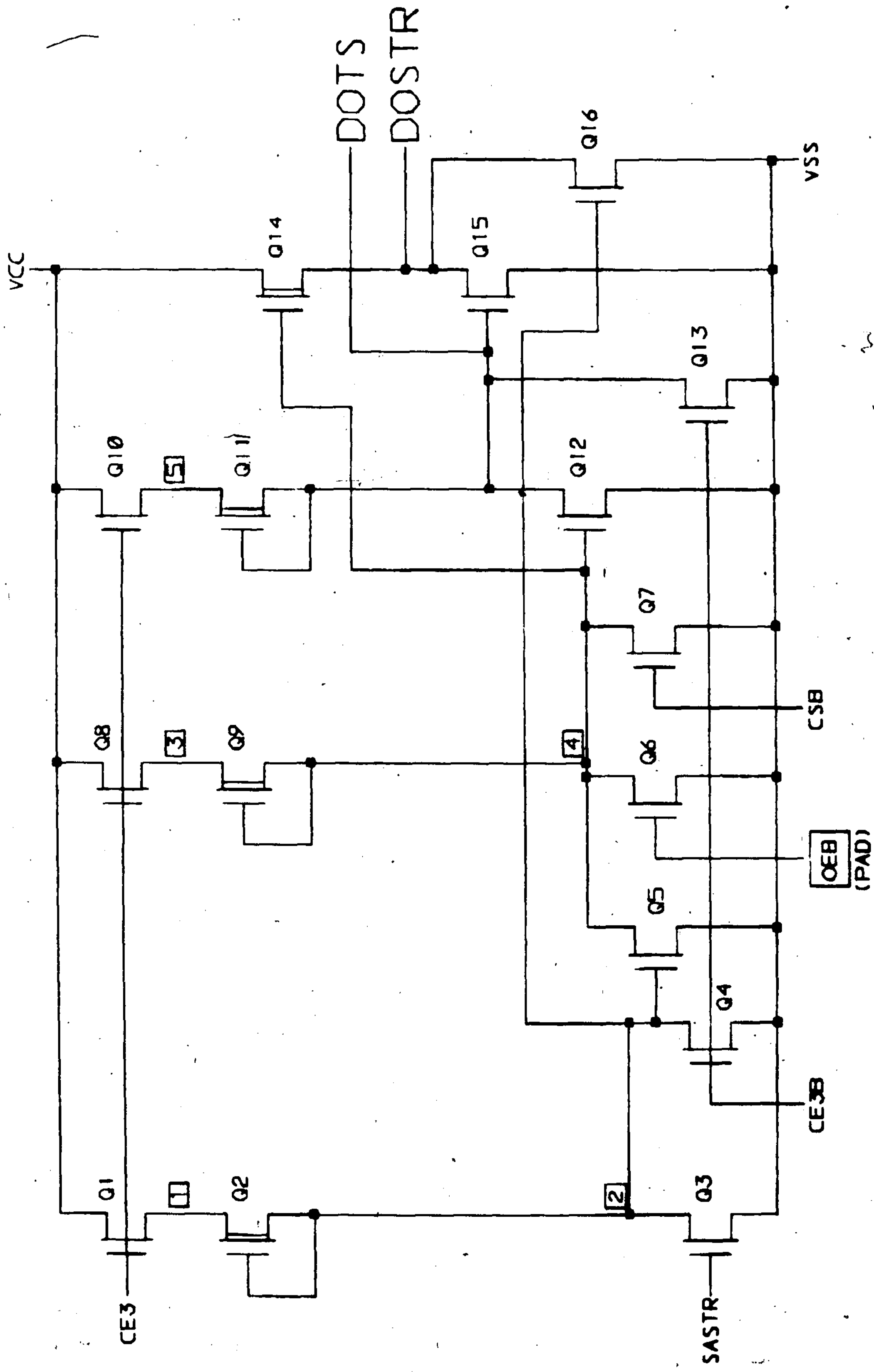


FIGURE 7

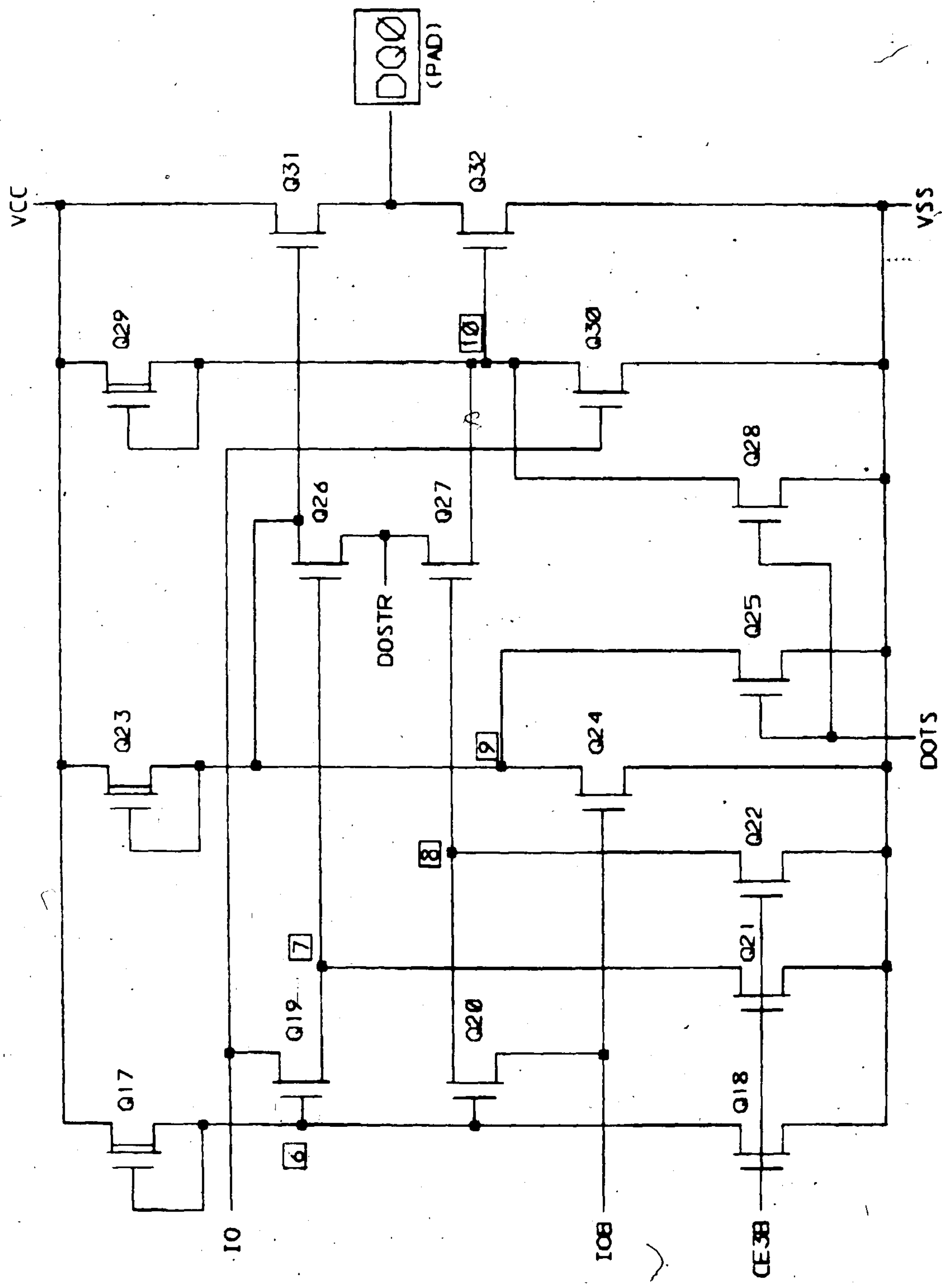
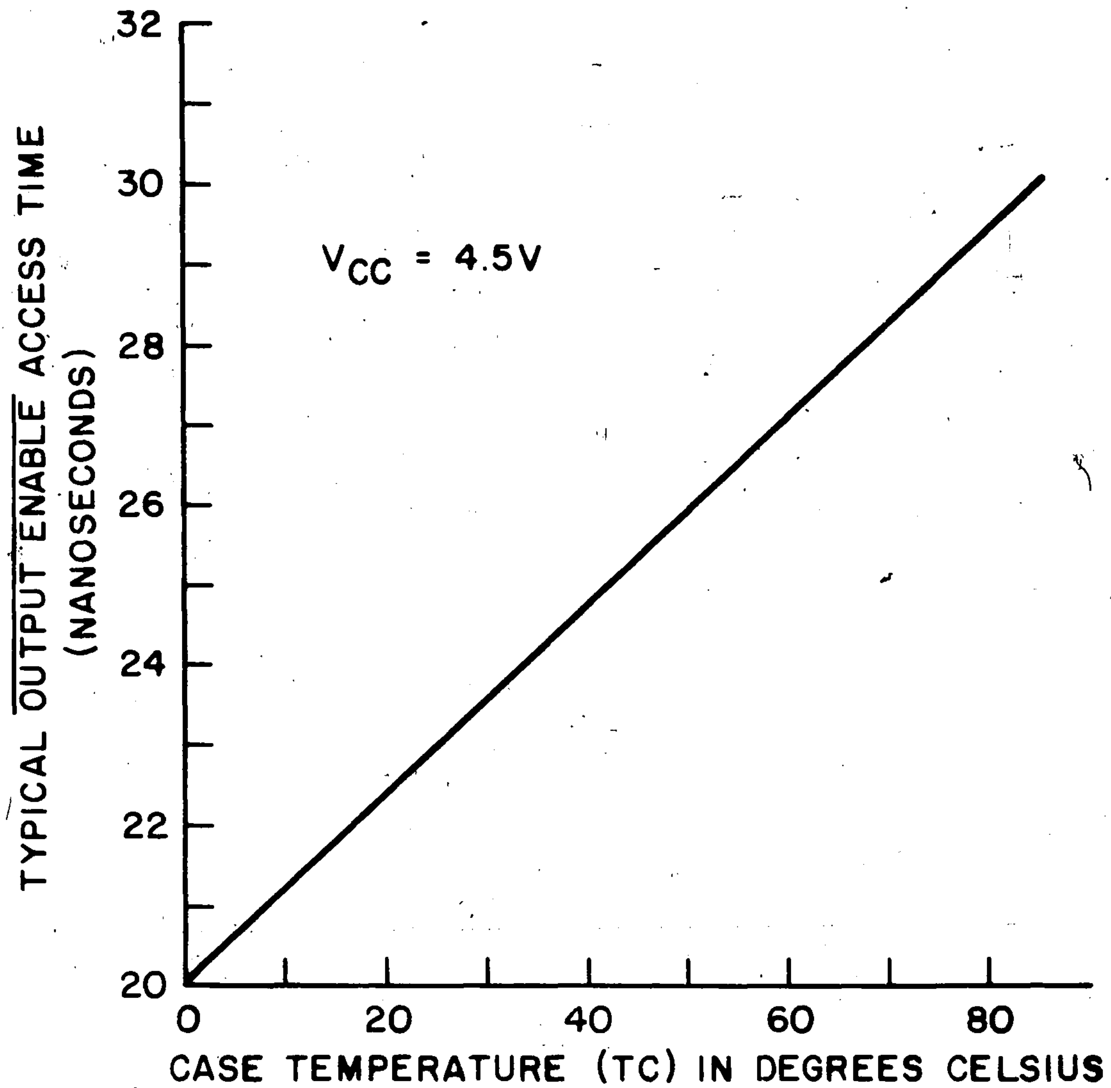
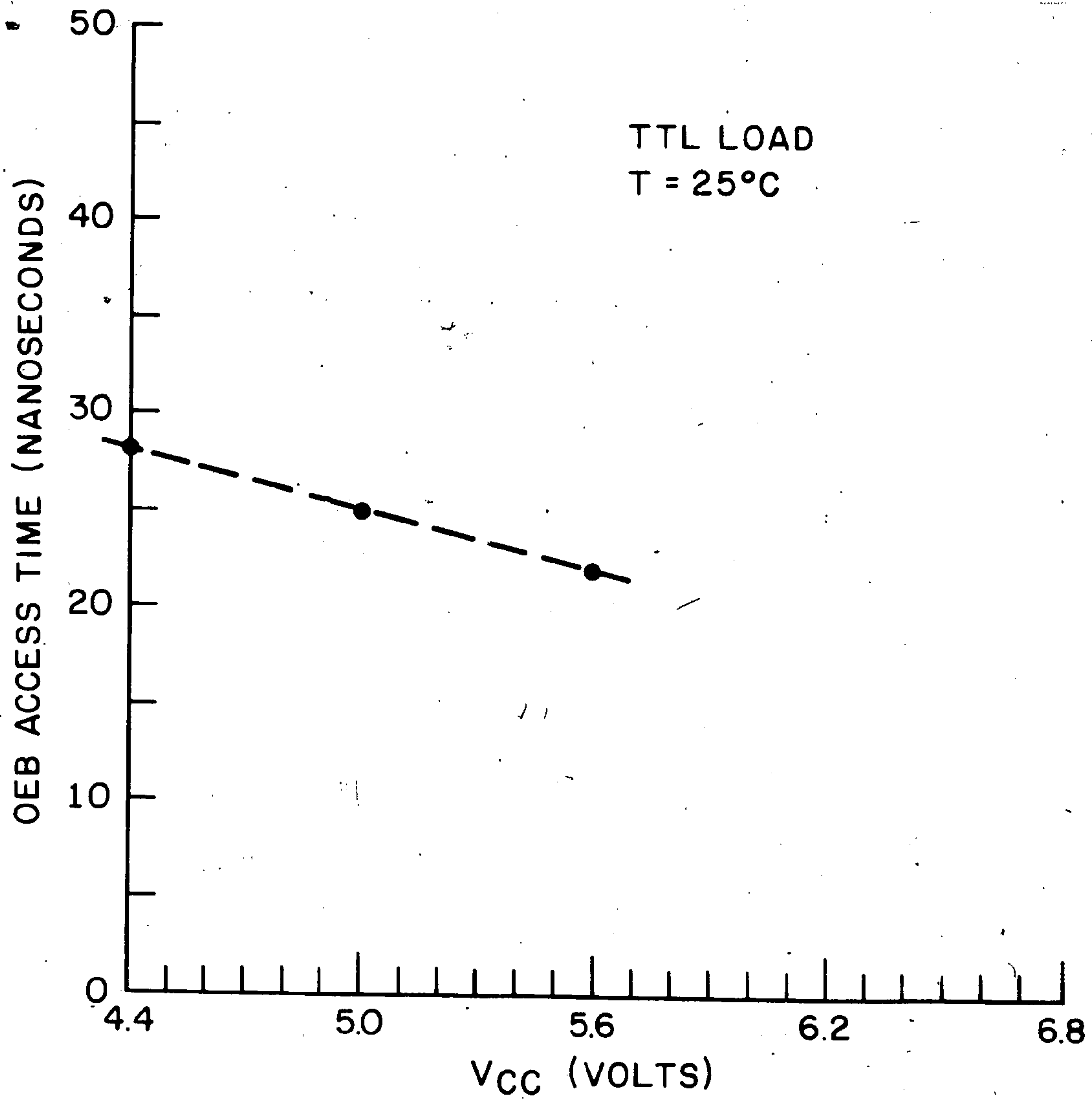


FIGURE 8



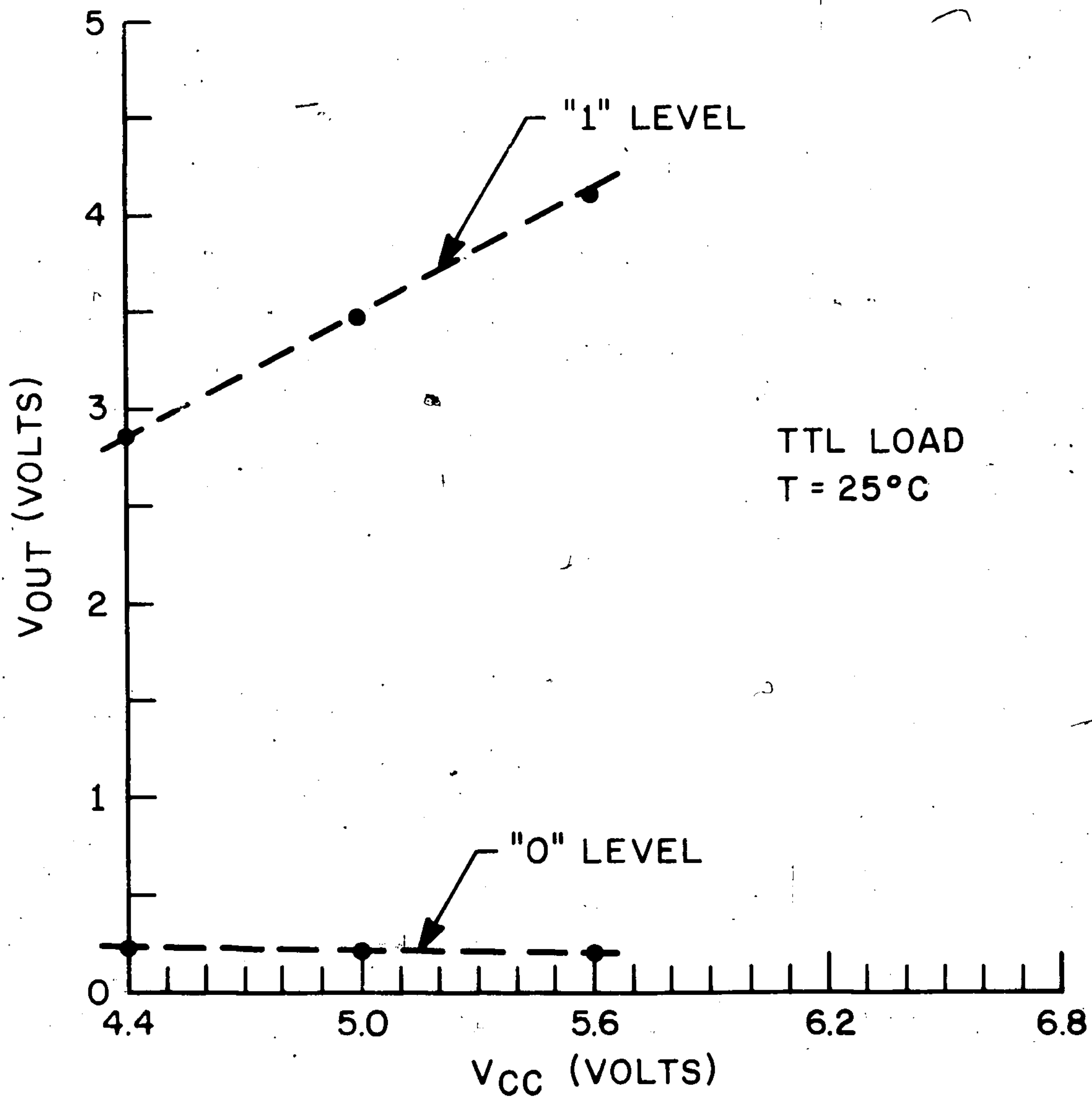
OUTPUT ENABLE ACCESS TIME
VS TEMPERATURE

FIGURE 9



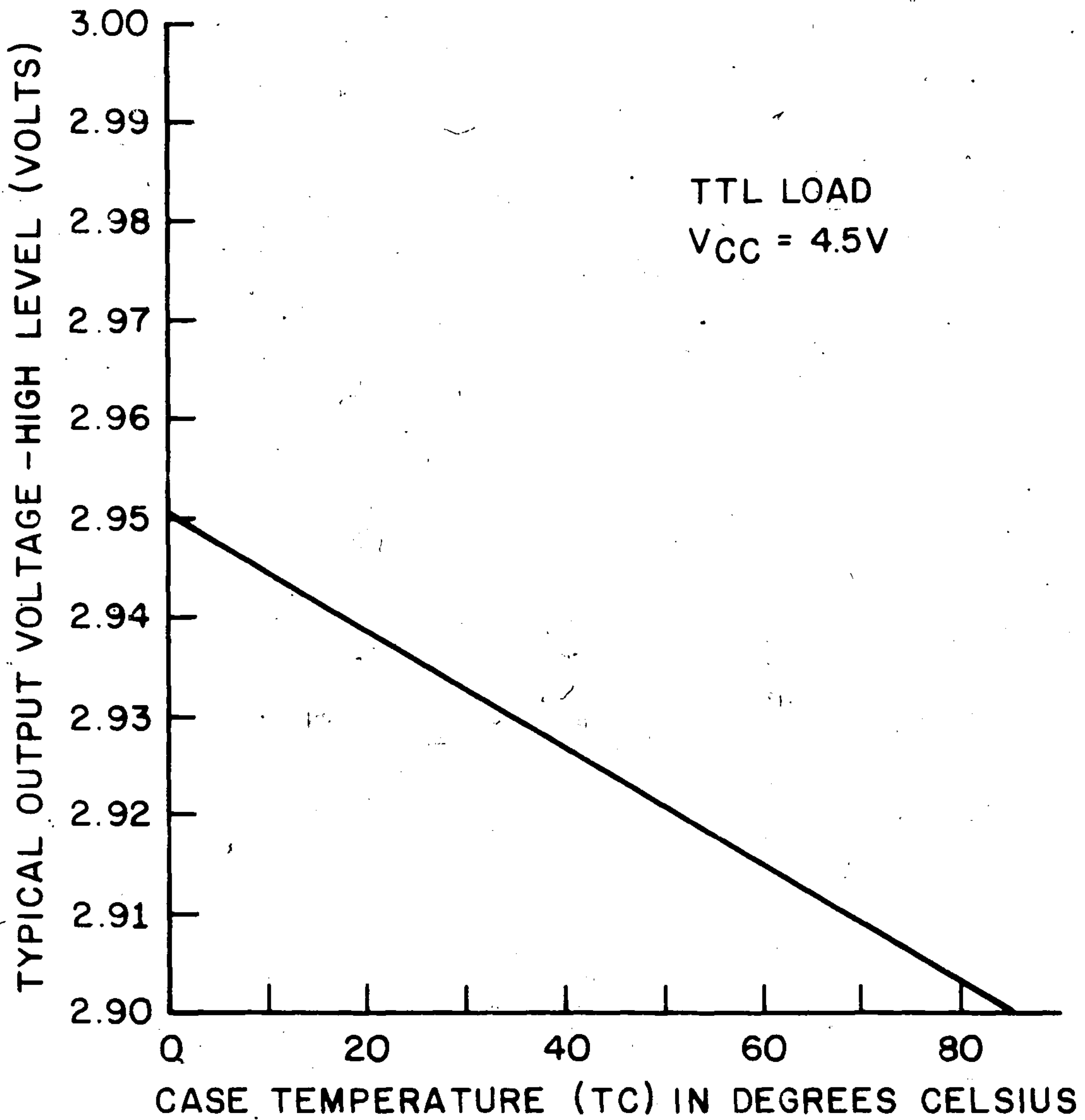
TYPICAL OEB ACCESS TIME VS V_{CC}

FIGURE 10



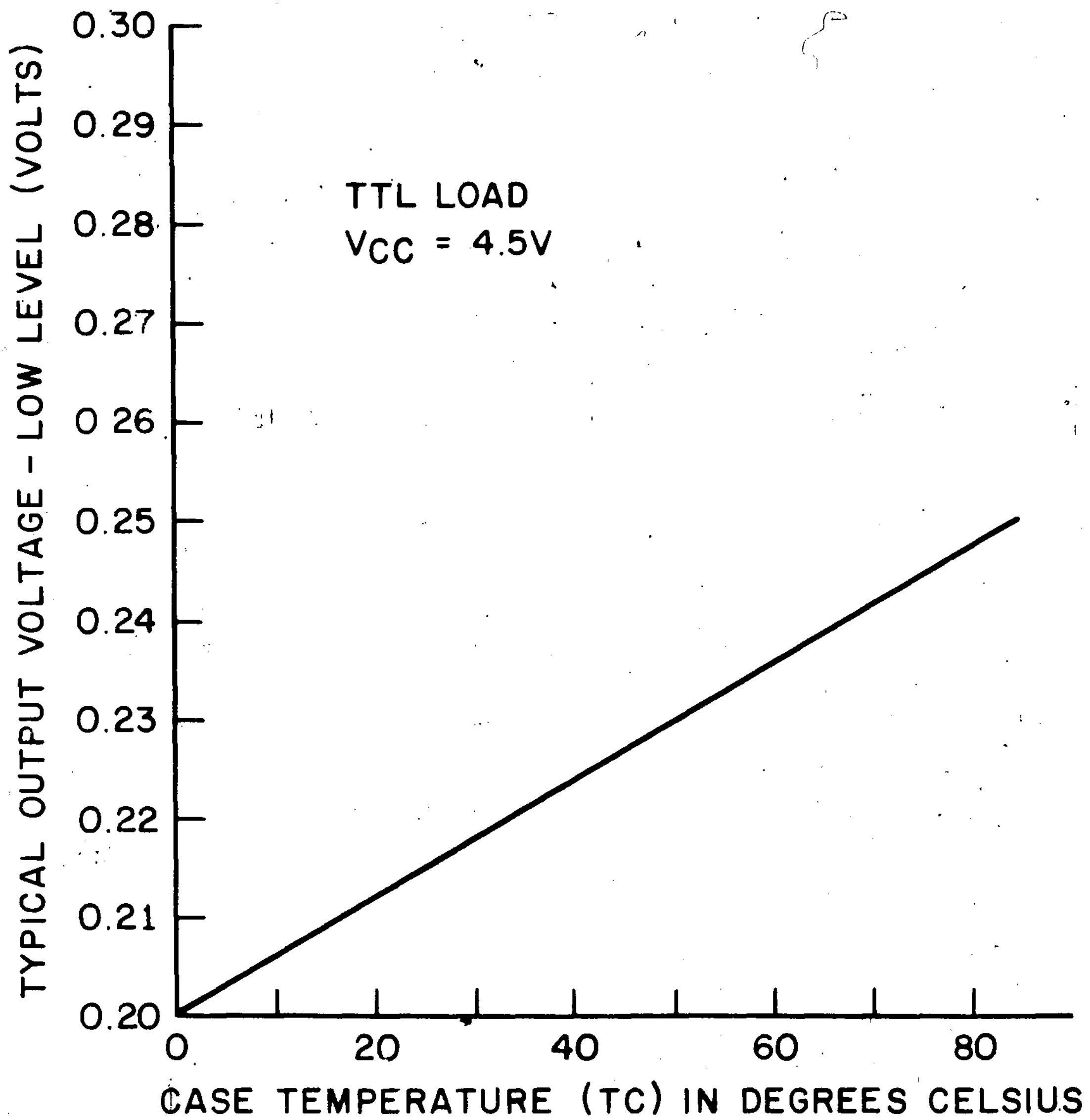
TYPICAL DATA OUTPUT BUFFER
"1" AND "0" LEVELS VS V_{CC}

FIGURE 11



DATA OUTPUT HIGH LEVEL VS TEMPERATURE

FIGURE 12



DATA OUTPUT LOW LEVEL VS TEMPERATURE

FIGURE 13

REFERENCES

1. R. P. Capece, "The Race Heats Up in Fast Static RAMs", ELECTRONICS, Vol. 52, pp. 125-135, April, 1979.

2. W. N. Carr and J. P. Mize, MOS/LSI Design and Application, McGraw-Hill Book Company, 1972.

3. The Engineering Staff of American Micro-System, Inc., MOS Integrated Circuits, Van Nostrand Reinhold Company, 1972.

4. L. W. Nagel and D. O. Pederson, "Simulation Program with Integrated Circuit Emphasis", Proc. Sixteenth Midwest Symposium on Circuit Theory, Waterloo, Canda, April 12, 1973.

VITA

Mr. Michael V. DePaolis, Jr. was born in Allentown, Pennslyvania on October 25, 1944, the son of Mr. and Mrs. Michael V. DePaolis, Sr. He graduated from Lewis E. Dieruff High School, Allentown, Pennsylvania in June, 1962. He graduated with an Associate in Science Degree in Electrical Engineering from the Pennsylvania State University in June, 1964. He joined Bell Laboratories, Murray Hill, New Jersey in 1964 where he worked on electroluminescent device studies. In 1970 he was transferred to Bell Laboratories, Allentown, Pennsylvania where he has been involved in integrated MOS Logic circuit design. He graduated with a Bachelor of Science Degree in Electrical Engineering from Lafayette College in June, 1973. Most recently, he has been involved in the design of CMOS Random-Access Memories. He and his wife, the former Ellen Powell, and their two children reside in Center Valley, Pennsylvania.