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# Digitizing and storing a TV picture frame in computer memory.

Ashutosh Virmani

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DIGITIZING AND STORING  
A TV PICTURE FRAME  
IN COMPUTER MEMORY

by

Ashutosh Virmani

A Thesis

Presented to the Graduate Committee  
of Lehigh University  
in Candidacy for the Degree of  
Master of Science  
in  
Electrical Engineering

Lehigh University

1978

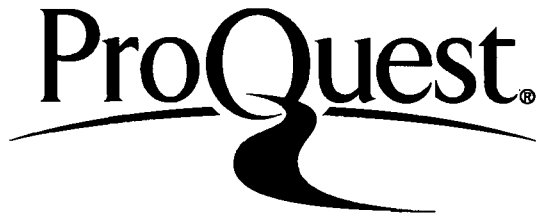
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## TABLE OF CONTENTS

	<b>Page</b>
1. ABSTRACT . . . . .	1
2. INTRODUCTION . . . . .	3
2.1. Statement of Objective . . . . .	3
2.2. Visualizing the Final System . . . . .	4
3. STUDYING THE RESOURCES . . . . .	6
3.1. The Camera and Its Signal. . . . .	6
3.2. HP-1000 Computer System. . . . .	11
3.3. TV Interface Subsystem . . . . .	12
3.4. A/D Interface Subsystem. . . . .	15
4. EVOLVING A GOOD STORING SCHEME . . . . .	18
4.1. Deciding upon Resolution . . . . .	18
4.2. The Sampling Scheme. . . . .	19
4.3. The Memory Management. . . . .	21
4.4. Uncertainty of Sample-and-Hold . . . . .	22
4.5. Design Specifications for Hardware . . . . .	24
5. DESIGN OF THE HARDWARE . . . . .	25
5.1. The Block Schematic. . . . .	25
5.2. Design of Special Circuits . . . . .	28
5.3. Detailed Working of the Hardware . . . . .	33
6. DESIGN OF THE SOFTWARE . . . . .	39
6.1. Program Organization and File Structure. . . . .	39
6.2. Program TVIN . . . . .	42
6.3. Program TVOUT. . . . .	44

7.	THE FINAL PRODUCT	
7.1.	Evaluation of the System and Possible Improvements . . . . .	
8.	BIBLIOGRAPHY	
9.	APPENDICES	
9.1.	Output Specifications of TV Interface Subsystem in Mode I . . . .	
9.2.	Characteristics of S/H703 - Sample and Hold Amplifier . . . . .	
9.3.	Signals on the 44 Pin Connector . .	
10.	VITA	

LIST OF FIGURES

	Page
1. Proposed Layout of the Final System . . . . .	5
2. Fields of TV Scan . . . . .	7
3. The Video Waveform. . . . .	9
4. Horizontal Synchronizing Pulse. . . . .	10
5. Output of TV Interface Card . . . . .	14
6. Addresses of Points in TV Picture . . . . .	14
7. Characteristics of Pacer Pulse. . . . .	16
8. Characteristics of S/H Subsystem. . . . .	16
9. Measured Data Format. . . . .	17
10. The Sampling Scheme . . . . .	20
11. Consequence of S/H Uncertainty. . . . .	23
12. Hardware Block Schematic. . . . .	27
13. Elimination of Bounce . . . . .	30
14. The Complete Circuit. . . . .	37
15. Circuit Waveforms (I) . . . . .	38
16. The File Structure. . . . .	41
17. Flow-Chart of TVIN. . . . .	43
18. Flow-Chart of TVOUT . . . . .	45
19. Display of Stored Picture . . . . .	48



## 1. ABSTRACT

Picture processing is a recent phenomenon in the world of digital computers. As the techniques of picture-enhancement, pattern-recognition, etc., find new directions in the realm of picture processing, the hardware support is also building up in the form of providing a digitized picture as an array in computer memory. Various modules are now available which capture a TV picture, digitize it and store it in computer memory.

Model CD5506, available from De Anza Systems provides the capability of capturing an image with 64 levels of grey scale and 512 x 512 pixel (pixel = picture element) resolution in one TV frame time. Model CD5508, also available from De Anza, will digitize an image to 256 levels. Prices for these models start at \$15,300.

In order to store a large number of picture elements (258,144 elements -- in case of 512 x 512 matrix) in  $\frac{1}{30}$  second, a fast analog-to-digital converter is necessary. Many video A/D converters are now available which can do the conversion at rates up to 20 MHz. Some of them are -- MATV-0811 (8-bit, 11 MHz, \$1150), MATV-0808 (8-bit, 8 MHz, \$995); both from Computer Labs, and ADC-TV (8-bit, 20 MHz, \$1995) from Datel.

However, it is our goal to produce a low-cost digitizer, which sacrifices the time of conversion and

hence will be suitable for storing a still picture.

The objective of the project was set forth to digitize the elements of a TV picture frame and store them in computer memory as inexpensively and in as small a time as possible.

The hardware designed for this purpose was bread-boarded and tested with software written for the HP-1000 computer system. Then the hardware was assembled on a printed circuit board and put in a chassis. This working piece of equipment is now with the Department of Electrical Engineering for future use.

## 2. INTRODUCTION

### 2.1. Statement of the Objective

The project consists of designing the hardware and writing appropriate software for digitizing and storing a TV picture frame in computer memory. The storing time and hardware cost will be minimized.

The following resources have been provided:

1. Panasonic TV Camera model WV-342.
2. A TV-monitor or video display system.
3. HP-1000 Computer System, with
  - a. Analog/Digital conversion subsystem.
  - b. TV display interface subsystem.
  - c. Disk storage.
  - d. Software driver packages.

Each of these resources will be studied in detail.

## 2.2. Visualising the Final System

Figure 1 shows how the final system is visualized to be.

The computer and the digitizing system will be at some distance. Cables will be run from the digitizing system to the computer. The following is how the user will be able to store a TV picture:

The user will run the program TVIN, available in the system library. The program will prompt the user to enter several parameters providing different options, e.g. the file name, the signal channel number, etc. The user will then be prompted to press the 'STORE' key provided on the hardware. The picture storing process will start and an LED will indicate when it has finished.

The user can now run the program TVOUT to display his stored picture on a TV monitor.

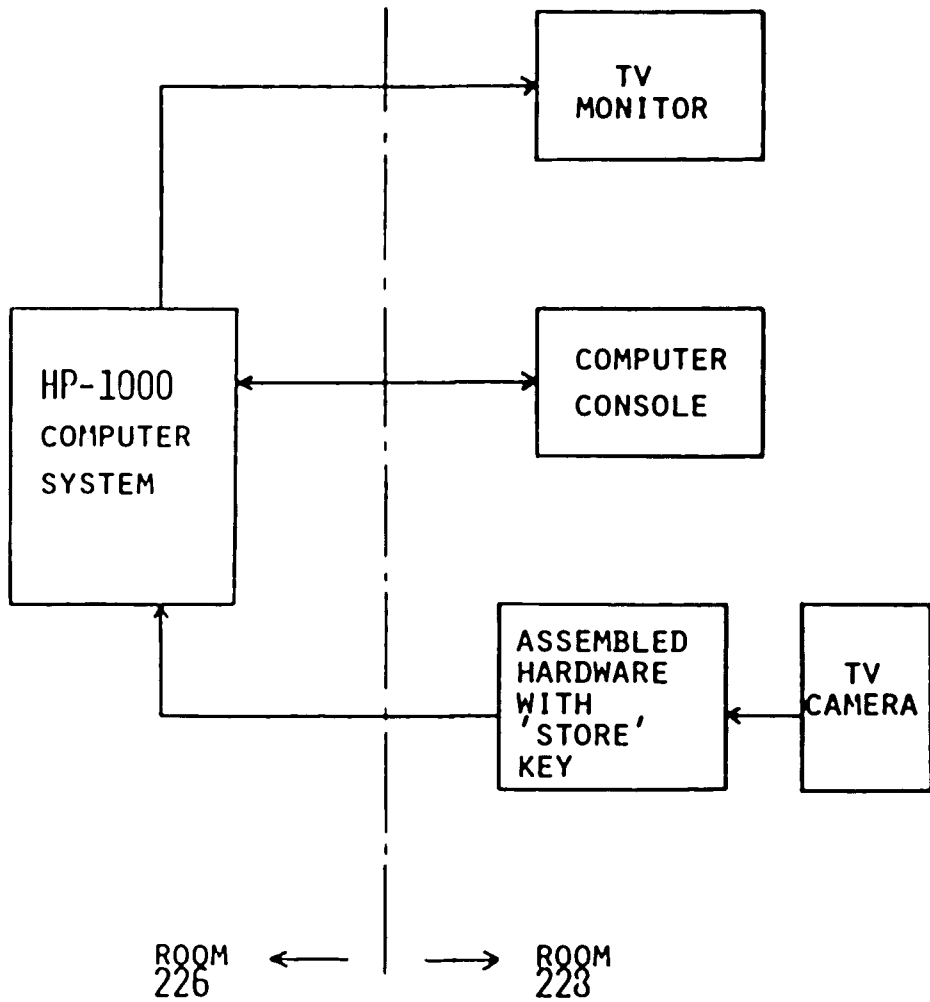


FIG 1. PROPOSED LAYOUT OF THE FINAL SYSTEM.

### 3. STUDYING THE RESOURCES

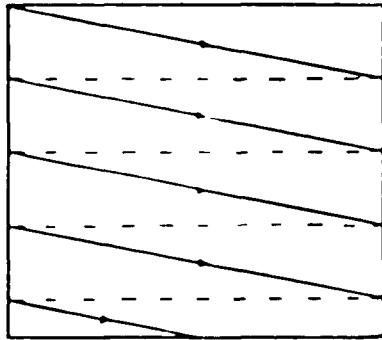
#### 3.1. The Camera and Its Signal

Of prime importance before one can interface a TV camera is to understand the amplitude and timing characteristics of the output waveform from the camera. The output specification for the camera reads as output video IV p-p (75  $\Omega$ ). However, it does not describe the scheme of synchronizing pulses. It was thought that the sync pulses would conform to American TV standards but it turned out that there were some differences in the vertical blanking part of the scans.

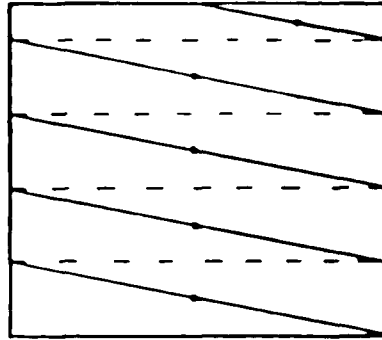
The Video Waveform: According to the American TV standards, a TV camera transmits at the rate of 30 picture frames per second. Each frame of the picture is, however, transmitted twice, there being two fields to a frame. This effectively sets the flicker frequency to be 60 Hz, which is unannoying to the eye. The scan lines corresponding to these fields are interlaced with each other.

The American standard horizontal scan frequency is 15750 Hz (-525 scan lines per frame, 30 frames to a second). Each field has 262.5 lines but only 243.5 contain information. The remaining 19 are blanked out and that time is consumed in the vertical retrace - once every 1/60 second.

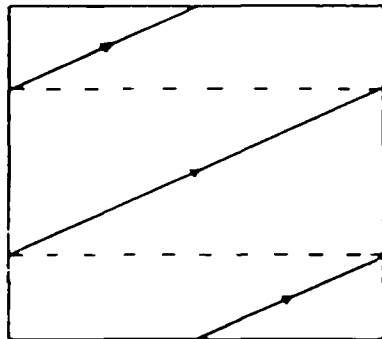
Figure 2 shows the scanning scheme in an American-standard TV.



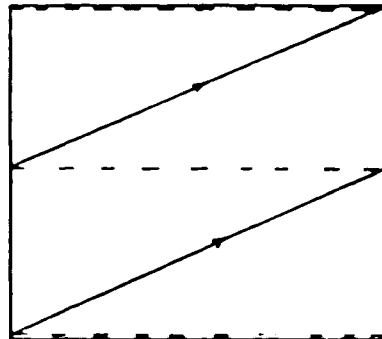
(A) FIELD 1 -  
FORWARD SCAN



(C) FIELD 2 -  
FORWARD SCAN



(B) FIELD 2 -  
VERTICAL RETRACE



(D) FIELD 2 -  
VERTICAL RETRACE

FIG. 2. FIELDS OF TV SCAN.

Each horizontal scan line begins with a synchronizing pulse and carries analog picture information. The voltage level of the sync pulse is much lower than that of the picture portion. Figure 3 shows the horizontal and vertical sync pulses contained in the output of our camera.

The details of one horizontal synchronizing pulse are shown in Figure 4.



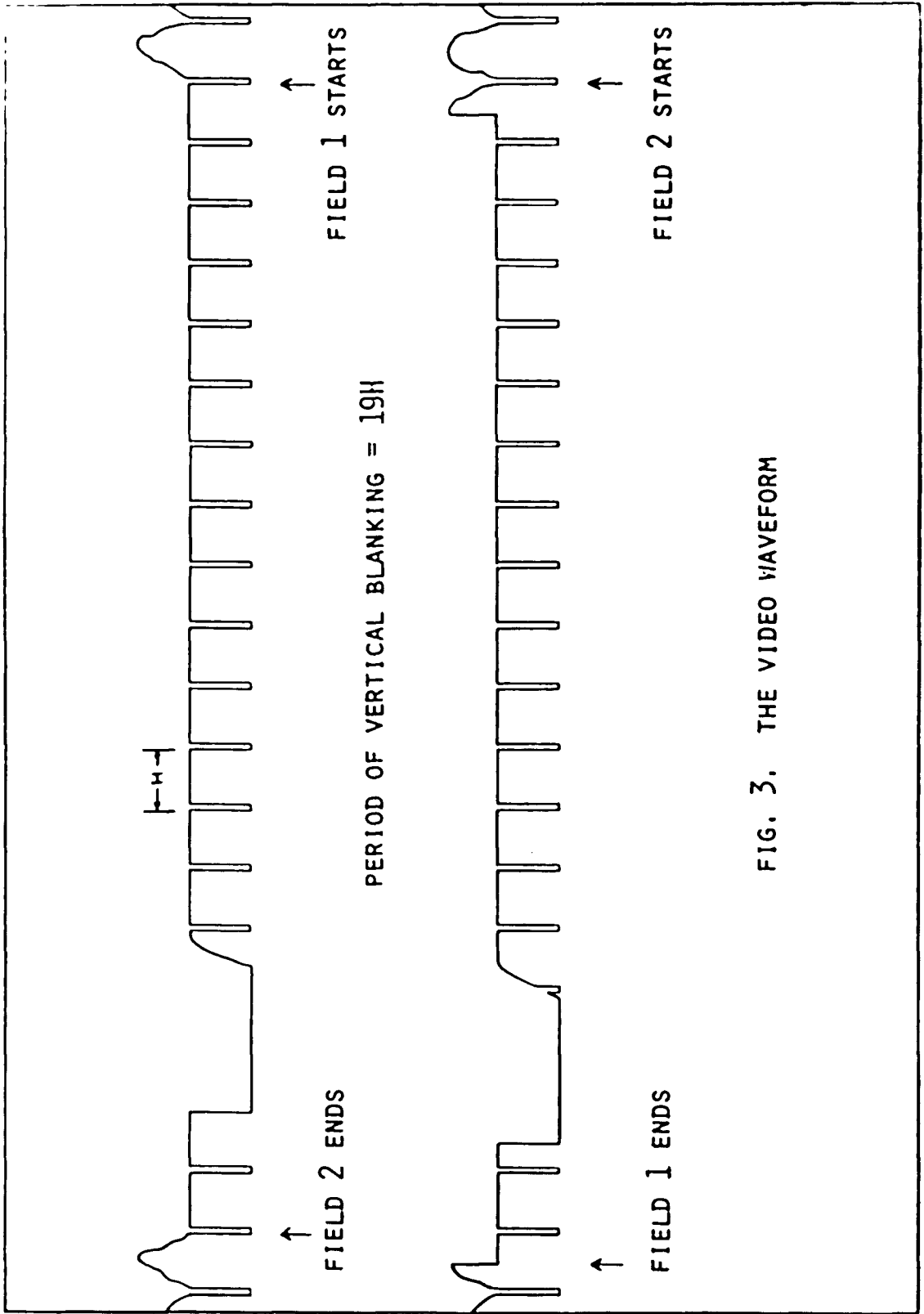
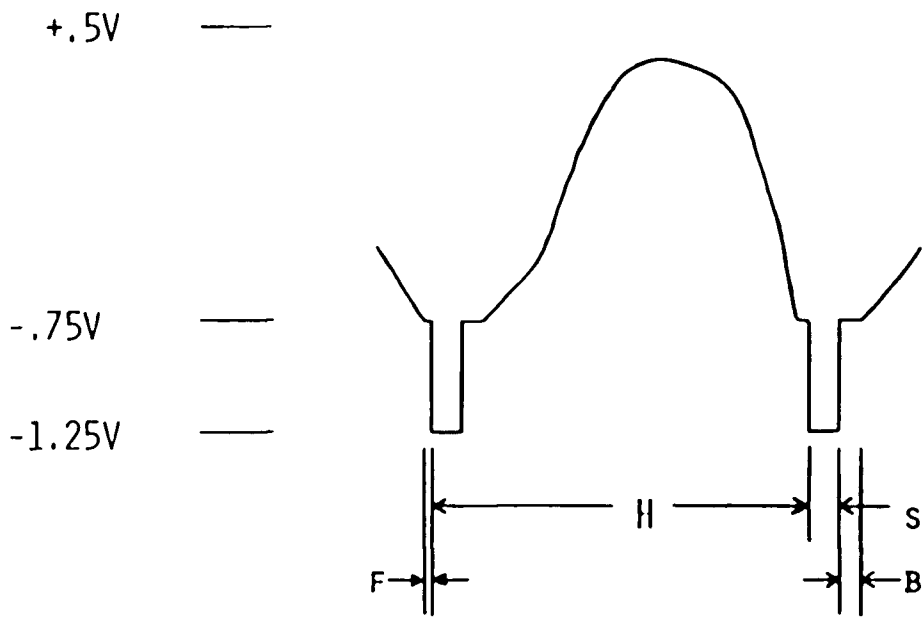


FIG. 3. THE VIDEO WAVEFORM



$$H = 63.492 \text{ S}$$

$$F = .02 H$$

$$S = .03 H$$

$$B = .06 H$$

FIG. 4. HORIZONTAL SYNCHRONIZING PULSE

### 3.2. HP-1000 Computer System

The computer is an HP-2113B supported by 32 K of semiconductor memory, a 15.5 MByte disk and a 9-track tape unit. The programming languages supported by the system are FORTRAN IV, ALGOL and assembly language.

Of major interest are two of its interface subsystems -- the A/D conversion subsystem and the TV interface subsystem.

The A/D interface subsystem is capable of multiplexing a maximum of 16 single-ended channels or 8 double-ended channels. The TV interface subsystem can drive a maximum of 5 TV monitors, connected in tandem, the farthest of them being 500 meters away.

Software support packages for these subsystems are available.

### 3.3. TV Interface Subsystem

The TV interface subsystem can be programmed to provide displays which combine both graphic images and alphanumeric characters on standard television monitors. Systems having two or three cards can display variable levels of gray on black-and-white monitors or color on color monitors. The monitors should be compatible with EIA RS-170 composite signals.

The subsystem is capable of three modes of operation. Mode I is the American Broadcast Standard, Mode II is the European Broadcast Standard, and Mode III is a non-standard scan to achieve full 256 vertical resolution with a 60 Hz vertical scan rate.

It is proposed to use Mode I or the American Broadcast Standard, the specifications of which are described in Appendix 9.1. Figure 5 shows the details of one horizontal sync pulse output from the subsystem.

Additionally, the TV display subsystem contains a 65,536 bit solid-state memory made up of 16 4K RAM's, which drives the raster scan to generate the picture. The bits stored in this memory are directly related to the points displayed on the TV monitor in a 256 x 256 array. One sixteen-bit computer word is used to address any point in the display memory. The lower 8-bit byte is used to specify the Y (vertical) axis of 256 (0-255) locations.

Figure 6 shows the scheme used to address the data points displayed in a TV picture.

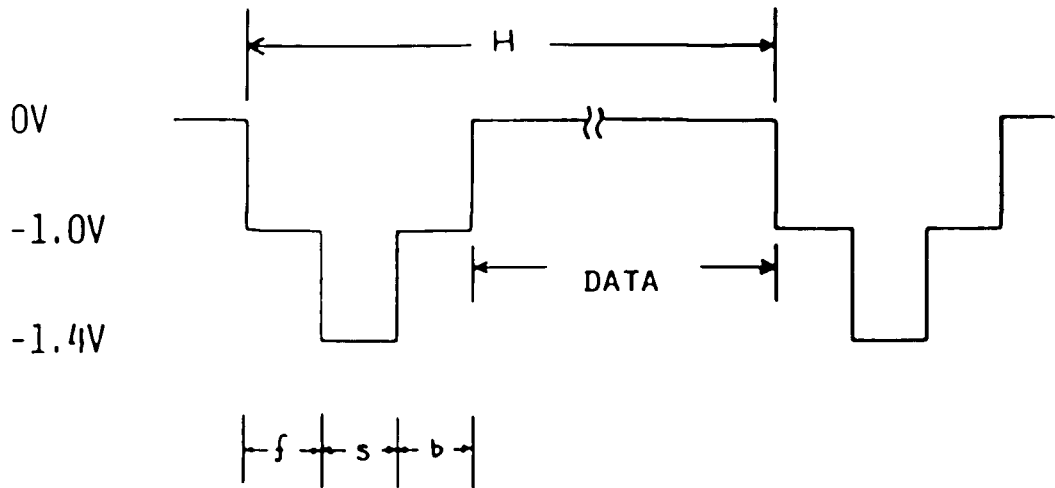


FIG. 5. OUTPUT OF TV INTERFACE CARD

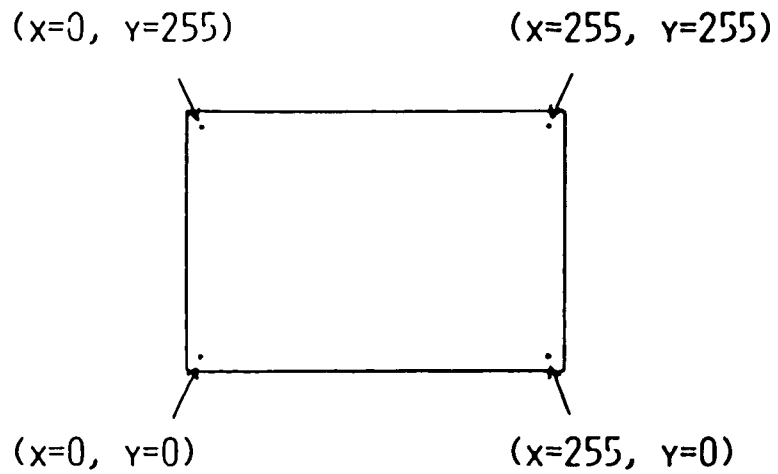


FIG. 6. ADDRESSES OF POINTS IN TV PICTURE

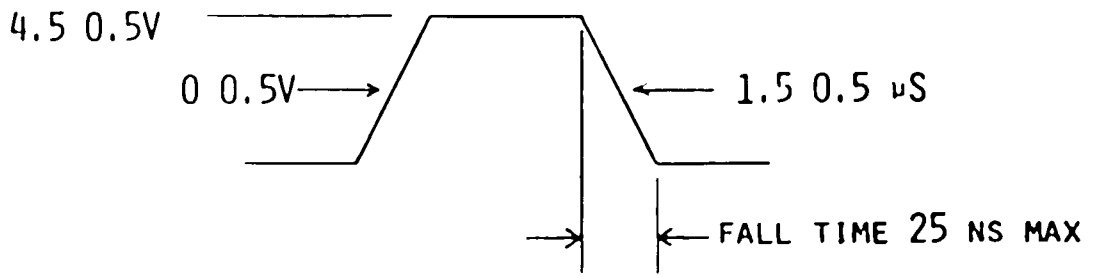
### 3.4. Analog to Digital Interface Subsystem

External analog data, either 8 differential or 16 single-ended channels can be input by using the A/D subsystem. This data acquisition subsystem scans the multiple analog input signals, converts them into 12-bit 2's complement binary representation and returns the data to the computer for processing. Input voltage range is +10.235 to -10.240, with overvoltage protection. This voltage range produces a resolution of exactly 5 mV for the least significant bit.

There are various modes of operation of this A/D subsystem. Most attractive for the interface design is the DMA mode with paced measurements. In this mode, an external pace-pulse has to be supplied to the subsystem, the trailing edge of which initiates the acquisition of the analog data.

Figure 7 shows the required characteristics of the pacer pulse. Figure 8 shows the characteristics of the sample-and-hold, which holds the analog signal for A/D conversion.

The maximum conversion-rate the system can fulfill is 20 KHz (when using DMA-direct memory access).



SOURCE IMPEDANCE: 100Ω MAX  
 RECOMMENDED SOURCE: STANDARD TTL)

FIG. 7. CHARACTERISTICS OF PACER PULSE

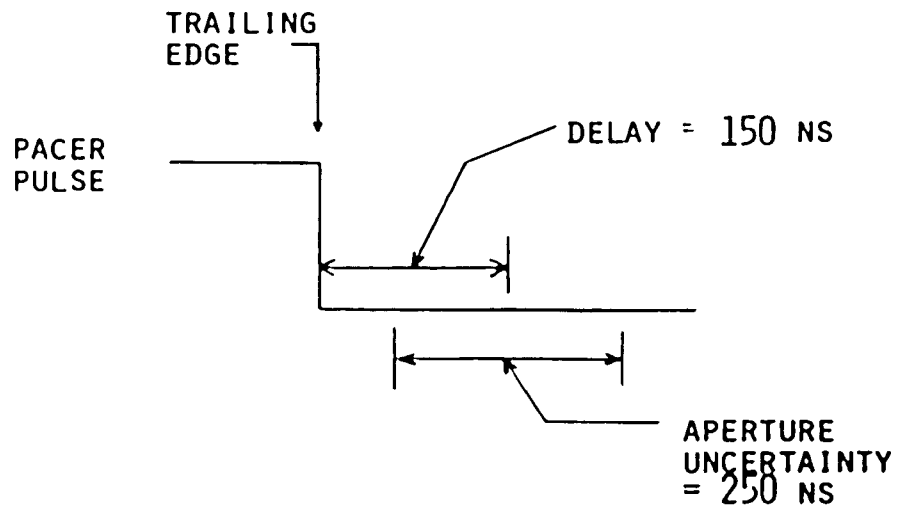


FIG. 8. CHARACTERISTICS OF S/II SUBSYSTEM



## MEASURED DATA FORMAT

The A/D subsystem provides the data to the computer in the following format

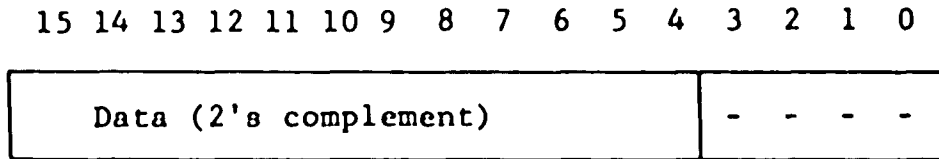


Figure 9. Measured Data Format

Bits 3-0 are unspecified during conversion. The following FORTRAN statement will convert the raw data into volts:

```
VOLTS = FLOAT(IAND(IDATA,177760B))*0.0003125
```

with the least significant bit equaling 5 mV.

The supporting software for this subsystem is described in 'Plug-In 20 KHz A/D Interface Subsystem -- Programming and Operating Manual.'

#### 4. EVOLVING A GOOD STORING SCHEME

##### 4.1. Deciding upon Resolution

The maximum resolution that can be achieved in storing a picture is determined by the TV scan rate. Since there are  $2 \times 243.5 = 487$  horizontal scan lines in a picture frame, the maximum vertical resolution (equals the number of points across the height of the picture) that can be obtained is 487 pixels (pixel means a picture element). Since the aspect ratio of standard television is 4:3, 648 points across the width of the picture will provide an equal resolution in the horizontal direction. So one could think of storing the picture as a 487 x 648 array of picture elements. But the TV interface subsystem of HP-1000 can only display a picture with a resolution of 240 x 256 pixels (in Standard American Broadcast mode).

Also because we wish to use TTL logic and inexpensive components, whose delays are substantial, it is more realistic to digitize the TV image with a resolution of 240 x 256 rather than 487 x 648 pixels.

#### 4.2. The Scheme of Sampling

A horizontal scan-line is 63.492  $\mu$ S long, out of which 18% is blanked out. The remaining 52.06  $\mu$ S carries video information. To pick up all 256 pixels from a line in 52  $\mu$ S would require sampling, digitizing and storing at the rate of 5 MHz. However, with the given 20 KHz A/D subsystem, one could not be that ambitious.

Therefore, the following sampling scheme was chosen:

As the scan starts at the top of the frame, the first pixel of the first scan-line is converted, then first pixel of the second scan-line is converted and so on till 240 pixels, representing the first 'column' of the TV field are converted. 1/60 second has elapsed at this point. When the next field starts, the interface converts the second column pixels of the picture field, and so on. Thus it takes 256 fields to pick up all the pixels in the frame.

Figure 10 illustrates the scheme of converting and storing the pixels. Since the time between two samples is 63.492  $\mu$ s, the A/D subsystem will be able to handle it.

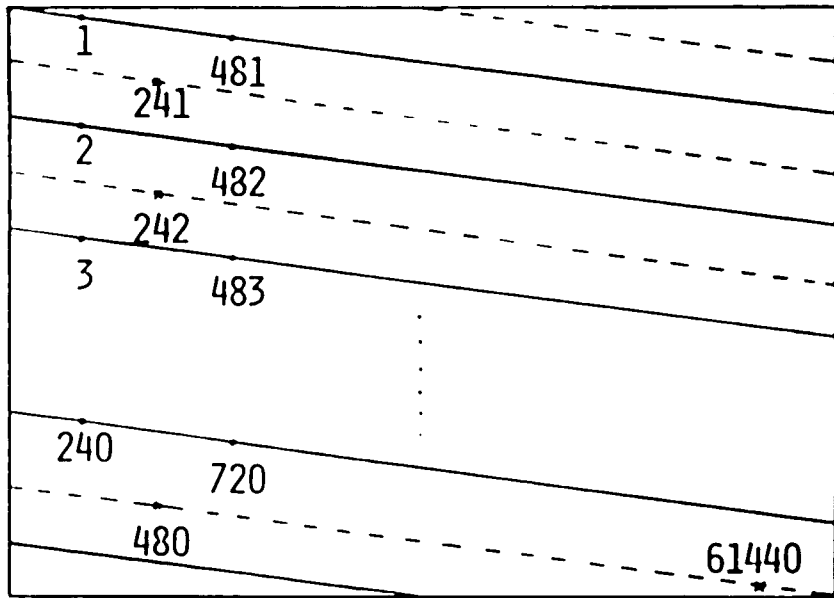


FIG. 10. THE SAMPLING SCHEME

### 4.3. Memory Management

The conversion scheme produces 61440 words of data representing a 240 x 256 picture. These data words come into memory by means of DMA (direct memory access). But the main memory has only 32 K words. This rules out the possibility of a one-shot storage process. In fact, since the program and other driver routines reside in main memory, we can not input more than 10,000 pixels at one time. This was determined experimentally.

It was decided to input 32 columns of picture (7680 pixels) at one time, then transfer them to the disk, get the next 32 columns of picture and so on. This will require the whole storing process to occur in 8 parts and will increase the time required for storing. The extra time will be spent on -

a. moving data in main memory from where it resides after completion of DMA, to the buffer from which it is transferred to the disk.

b. disk latency time for the right disk sector to come under the read/write head.

c. seek time if the head is to move to the right track.

d. actual transfer from memory buffer to disk.

e. after the data transfer is over, the circuit will wait for the next field of picture to start before starting to input the next 32 columns of data.

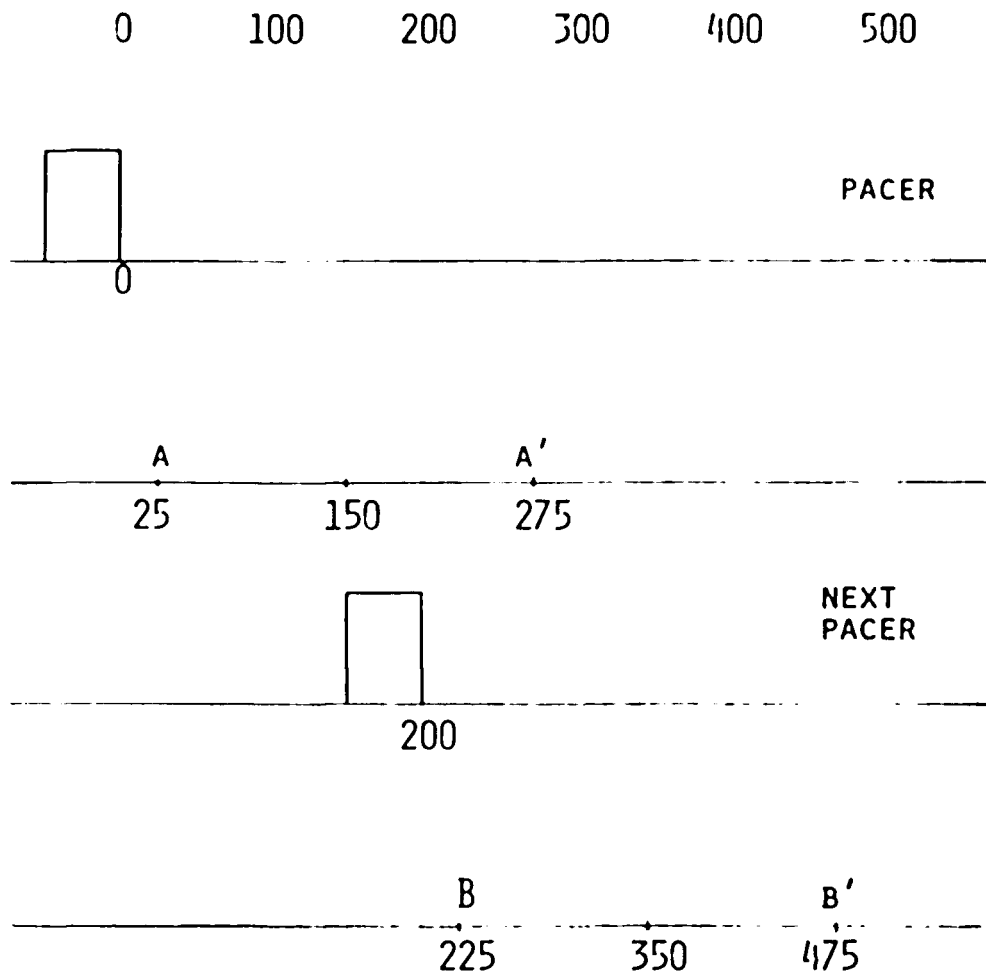
The total extra time required is 3 to 5 seconds.

#### 4.4. Uncertainty of the Sample and Hold

Two neighboring sampling points in the picture are separated by 200 ns. Figure 8 illustrates that the S/H circuit available in the A/D subsystem has an aperture uncertainty of  $\pm 125$  ns. The possible consequences of such uncertainty are shown in Figure 11.

The first pixel can be converted at any point between A and A' and the next consecutive one, which is supposed to be converted 200 ns later, can actually come in anywhere between -50 and +450 ns from the first one.

This being very undesirable, an external sample-and-hold amplifier with better aperture-uncertainty time was used. S/H 703, described in Appendix 912, was available and it gives an uncertainty of  $\pm 5$  ns, quite acceptable. However, the acquisition time of S/H 703 is specified to be 4  $\mu$ S with a holding capacitor of 1000 pf, while the required acquisition time for the present application is  $\leq 200$  ns. Although a much lower valued holding capacitor was used, S/H 703 may still not have the required acquisition time. This will affect the resolution of the picture.



HORIZONTAL AXIS IS TIME IN NS.

BECAUSE OF S/H UNCERTAINTY, ONE PIXEL CAN BE PICKED UP ANYWHERE BETWEEN A AND A' AND NEXT ONE BETWEEN B AND B'.

FIG. 11. CONSEQUENCE OF S/H UNCERTAINTY

#### 4.5. Design Specifications for Hardware

##### Input

The input is a 1 V p-p video signal available from a PANASONIC WV-342 camera. The source impedance is 75  $\Omega$ . The waveform is as shown in Figure 3.

##### Output

Two outputs are required from the hardware to be designed.

One is pacer pulses, one per pixel which occur at the right sampling times, and the second is the video signal held at the instant of occurrence of the pacer pulses.

The A/D subsystem will simply convert the held analog signal after the trailing edge of each pacer pulse.

After every 32 columns of storage, the pacer pulses stop so that the data can be transferred to disk.



## 5. DESIGN OF THE HARDWARE

### 5.1. The Block Schematic

The hardware for the project is illustrated by its major blocks as shown in Figure 12 and described as follows:

The process of storing has to start with the beginning of a TV field. Hence we need to extract the field sync pulses from the video signal. We can generate the composite sync signal (horizontal and vertical sync together) from the video waveform and then obtain the field recognition pulses.

When the STORE key is pressed, CTR A is set to 1. Upon arrival of the field recognition (FR) pulse, CTR B is set equal to CTR A, and the control circuitry activates the clock. The clock has a period of 200 ns (approx) -- the same as the pixel resolution. The clock goes into CTR B, which counts down by 1, and generates a pacer pulse. This moment of time is used to the first pixel on the first column of the field. The analog video signal is held at this moment and the A/D subsystem, prompted by the pacer pulse, converts it. The clock is stopped.

CTR C is incremented by 1 by this pacer pulse, indicating that the first element of the column has been stored.

When the next horizontal sync pulse arrives, CTR B is again set equal to CTR A and clock is started. CTR B counts down by 1, thereby generating a second pacer pulse, the second element of the first column is now held and converted. CTR C is again incremented by 1.

This goes on for 240 times, i.e. until the storing of the first column is complete. CTR C now generates a pulse which increments CTR A implying CTR A now holds 2. Each of the following 240 horizontal sync pulses sets CTR B equal to CTR A (now equal to 2) and CTR B counts down by 2 every time. The second column of pixels will thus be converted.

After 256 columns are converted, CTR A generates a pulse and resets the control circuitry, indicating that the storing is complete.

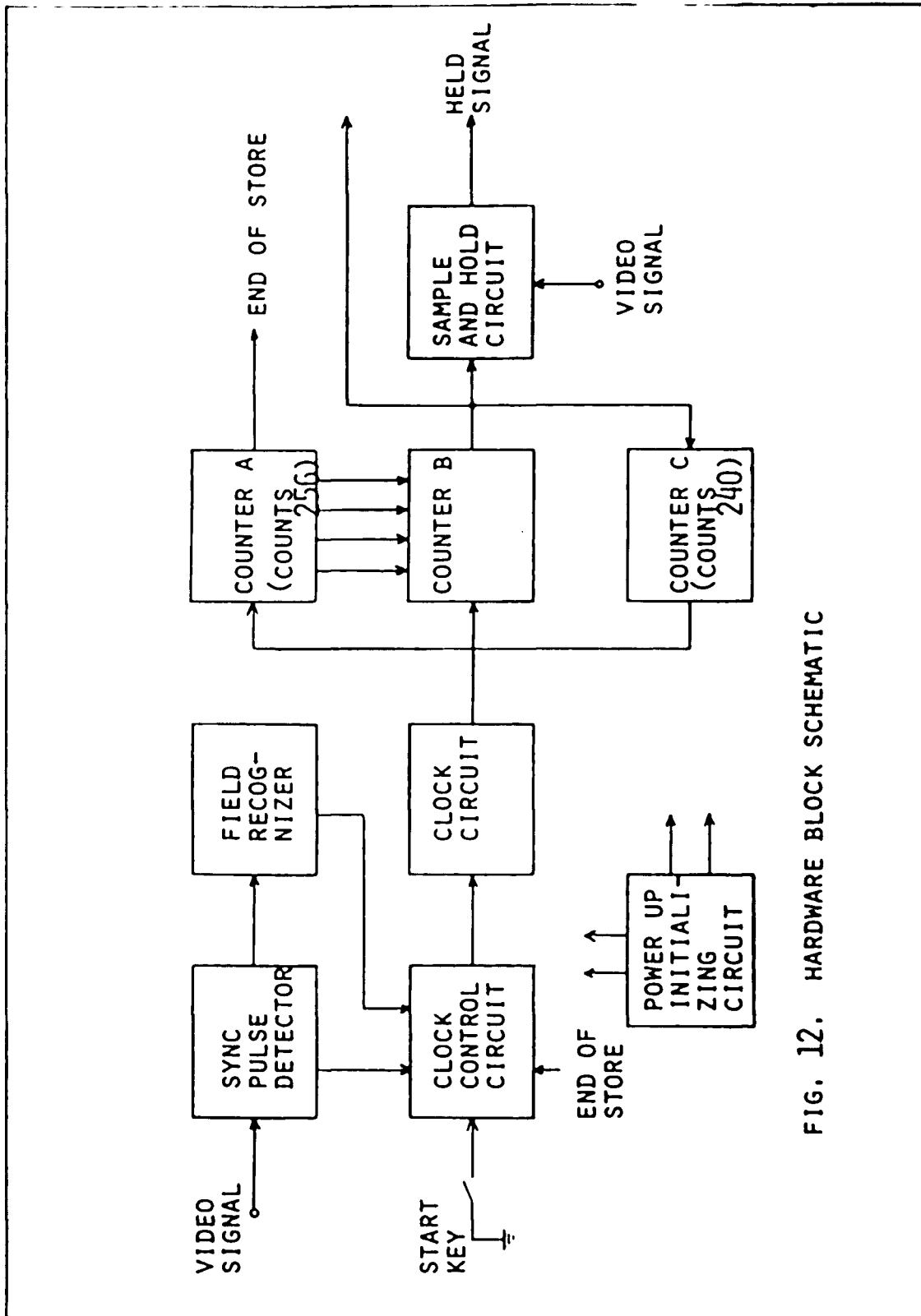


FIG. 12. HARDWARE BLOCK SCHEMATIC

## 5.2. Design of Special Circuits

For all circuits, please refer to Figure 14.

### 5.2.(a) Detection of Composite Sync Pulses

The voltage levels of the video waveform are shown in Figure 3. However, they change according to the brightness of the picture. A diode clamp was used to clamp the lower voltage near ground and then a comparator was used to output the composite sync signal. The reference voltage (.2 V) was provided by means of a 2 K $\Omega$  potentiometer.

### 5.2.(b) Detection of Field Recognition Pulses

From Figure 3, we know that the video signal has a pulse of width 150  $\mu$ S marking the beginning of every field. During this time, the horizontal sync pulses of 5  $\mu$ S width every 63.5  $\mu$ S do not occur.

If the composite sync signal is fed into a retriggerable monoshot of  $63.5 \mu\text{S} < T < 150 \mu\text{S}$ , then it will detect the field sync pulse (FR).

### 5.2.(c) Bounce Eliminator Circuit

The STORE key is a mechanical switch, which will trigger the storing process. Since any mechanical switch has bounces, they must be eliminated to avoid false triggering of the hardware.

Referring to the bounce-eliminator portion of Figure 14, we see that (3) of the monoshot 1C121 is normally HI. When the STORE key is depressed and released, the waveform at (3) is as shown in Figure 13. The monoshot triggers only once, on the first key closure, and not on release. The key-bounce is thus effectively eliminated.

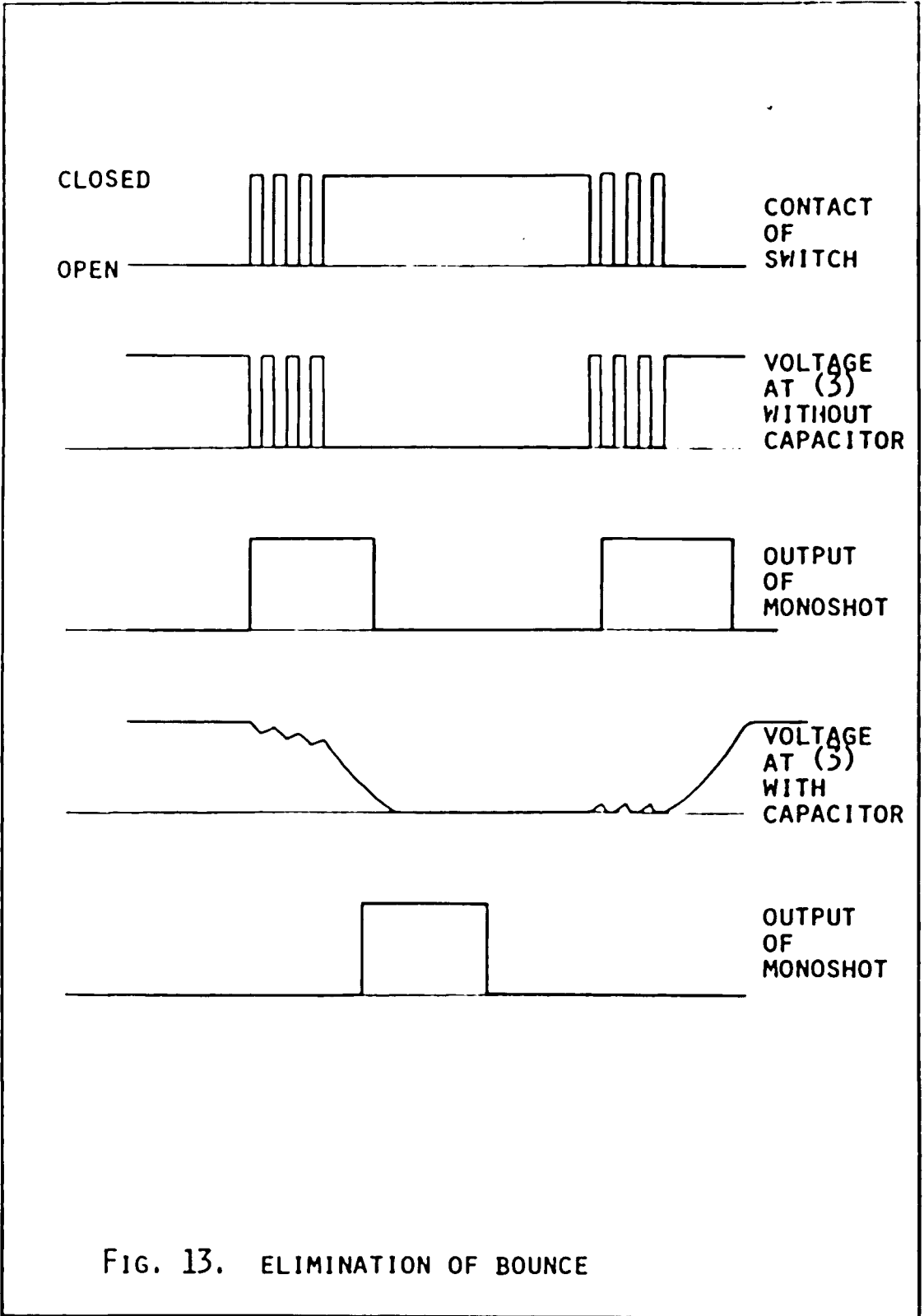


FIG. 13. ELIMINATION OF BOUNCE

### 5.2.(d) Initialization Circuit

When the power is turned on, we need to reset all memory elements in the circuit--flip-flops and counters --to a predetermined state. The initializing circuit works as follows:

When the power has just been turned on, the 100  $\mu\text{F}$  capacitor, connected to (5) of 1F121, is uncharged. It starts starts charging through the 10 K resistors and because of the sink current from (5) of 1F121. The sink current is 1 mA approximately and the parallel resistors effectively provide a charging resistance of 5 K $\Omega$ . The time constant for charging is roughly  $2\text{K} \times 100 \mu\text{F} = 200$  ms. When the voltage reaches a value above the monoshot input threshold voltage, the monoshot fires and the resulting pulse INIT is utilized for the necessary resetting. The pulse width is  $.7 \times 15 \text{K} \times .1 \mu\text{F} = 1$  ms.

### 5.2.(e) CLOCK Circuit

The duration of a horizontal scan is 63.492  $\mu$ S, out of which 18% is blanked. The portion with video information is therefore  $0.82 \times 63.492 = 52.06 \mu$ S. Since we wish to convert 256 samples in this elapsed time, the pixel distance is  $\frac{52.06}{256} = 203.36$  ns. The frequency of the required clock, then, is 4.9174 MHz. We also require that the clock start at the precise moment when GATE opens. A monoshot with a self triggering loop serves as the clock generator circuit-- 2F121 in Figure 14.



### 5.3. Detailed Working of Hardware

Figure 14 shows the completed hardware design. Figure 15 illustrates the signal waveforms at various points in the circuit. Almost all waveforms are pulses. A convenient notation of denoting a positive going pulse by an unbarred symbol and a negative going pulse by a barred symbol is followed throughout. The following is a detailed description of how the hardware operates.

#### 1. Power is applied.

The initializing circuit (1F121) generates the INIT pulse of 1 ms width. This pulse goes to various counters and flip-flops and resets them.

#### 2. STORE key is pressed.

KY pulse of 2 ms width appears at (3) of 4D08.  $\overline{KY}$ , applied to (4) of 1F121, fires it and the INIT pulse of 1 ms duration appears again. This makes doubly sure that the circuit is in reset state.

$\overline{KY}$  also goes to (3) of 1D74 flip-flop and ST gets set on the trailing edge of  $\overline{KY}$ . CTR A (3C93 and 3D93) is cleared by  $\overline{KY}$ .

#### 3. 1B123 is constantly giving out FR pulses at pin (4). When ST is set, the next FR to come sets STFR ((9) of 1D74). It also sets GO - (9) of 5C74.

$\overline{FR}$  at the same time, resets CTR P to a count of 0 and sets CTR C to a count of 16. Since  $\overline{STOP}$  at (1) of 3E121 is HI at this time, STFRT at (6)

of 3F08 goes HI.

4. CS pulses now reach CTR P (2A93) which counts down by 16, after which (11) of 2A93 makes a HI to Lo transition and fires monoshot 2B121, which in turn gives out CTRPP of 1.5  $\mu$ S. (As apparent from Figure 15, the vertical blanking time is now over and storing of picture must commence).
5. CTRPP sets CMD at (5) of 2C74.  $\overline{\text{CMD}}$  makes GO low. CTR P gets no more CS pulses.

CS is now free to go into 2D121 and triggers the monoshot on its negative transition. This monoshot has a time constant of  $.7 \times 14.7 \text{ K} \times 1000 \text{ pf} = 10 \mu\text{S}$ . This is kept so as to produce a delay equal to the width of the horizontal blanking pulse.

$\overline{\text{MONO}}$  loads the contents of CTR A into CTR B.

6. With the trailing edge of MONO, the horizontal blanking time is over and we are ready to sample. GATE is set by the trailing edge of  $\overline{\text{MONO}}$  and CLOCK is activated.
7. CLOCK goes into CTR B and starts counting down. Since CTR B had been set to 0, on the first going edge of the CLOCK,  $\overline{\text{CTR B}}$  appears at (13) of 4A193, which produces the pulse CTRBP of duration 1.5  $\mu$ S.  $\overline{\text{CTRBP}}$ , in turn, resets flip-flop 2C74. CTRBP is gated out to become the pacer pulse.
8. The pacer sets flip-flop 5C74 which commands

6A S/H 703 to hold the video signal at the moment.  
This is the first sample of video waveform.

9.  $\overline{\text{CTRBP}}$  goes into CTR C and increments it by 1 on its trailing edge.

The circuit is now idling and nothing is happening. The A/D interface card is converting the analog signal and is transferring it to main memory. That process takes 50  $\mu\text{S}$  and the computer is ready to accept the next sample.

10. As the next CS pulse goes into 2D121, the monoshot again generates the blanking time.  $\overline{\text{MONO}}$  sets CTR B equal to CTR A and resets 5C74/II. CLOCK is again turned on, CTR B counts down, generates  $\overline{\text{CTRBP}}$ , which holds the second sample and increments CTR C by 1.

This goes on for 240 samples and then  $\overline{\text{CTR}\overline{\text{C}}}$  appears. One column of pixels is now completely transferred.

11.  $\overline{\text{CTR}\overline{\text{C}}}$  goes to CTR A and increments it by 1.  $\overline{\text{CTR}\overline{\text{C}}}$  also goes to CTR M and increments it.

This repeats for 32 columns when 3E121 monoshot triggers and STFRT goes low, no more storing takes place after that for the duration of the STOP pulse (=0.5 sec). After that it starts again.

12. When 256th  $\overline{\text{CTR}\overline{\text{C}}}$  goes to CTR A,  $\overline{\text{CTR}\overline{\text{A}}}$  appears and resets ST and STFR. The total picture has by now been stored.

Figure 15 shows the various waveforms of the circuit.

NOTE: L NUMBERS INDICATE LANDINGS ON THE P.C.B.

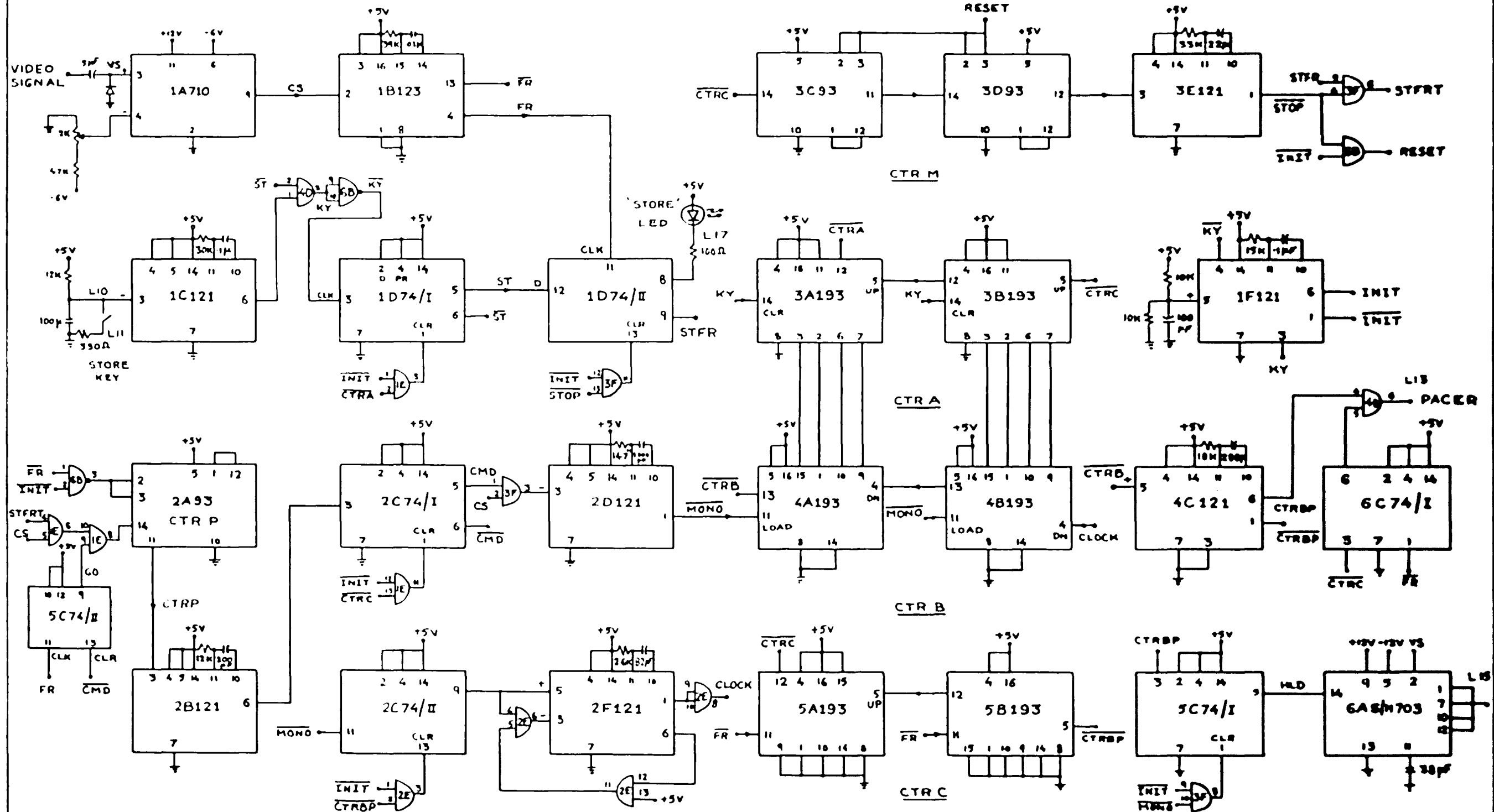


FIGURE 14. THE COMPLETE CIRCUIT

L15 - VIDEO OUTPUT

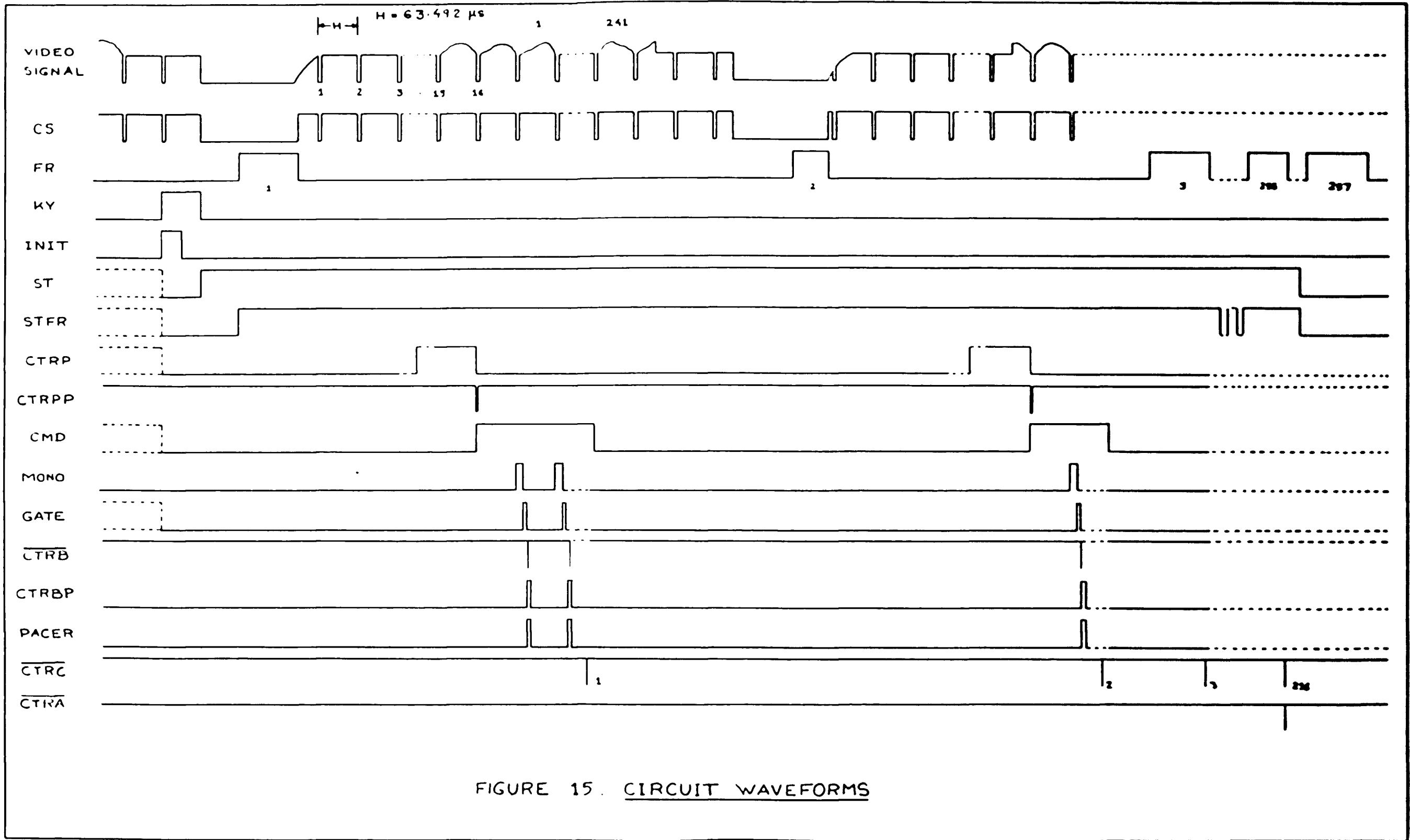


FIGURE 15. CIRCUIT WAVEFORMS

## 6. THE DESIGN OF SOFTWARE

### 6.1. Program Organization and File Structure

It is decided to develop two programs, the first to store an image and the second to recreate the image and display it on a TV monitor.

1. Program TVIN: This program can be used to input the picture and store it on a disk file specified by the user. It should be possible to use any of the 16 channels as the input channel for the A/D subsystem.

2. Program TVOUT: This program can be used for displaying the picture data residing on any disk file on a TV monitor. It will be possible to change the black-to-white threshold at will.

#### The File Structure

Since the A/D interface card changes the analog signal into a 16-bit word, each word of the data file will represent one pixel. The standard picture data file as used by TVIN and TVOUT programs has been defined as a type 2 HP-File-Manager-formatted file with the following characteristics:

Number of records = 256

Number of words/record = 256

Number of standard 128-word blocks occupied  
by the file = 512

Each record in the file represents a column of picture. The first word in a record is the top pixel of

the column while the 240th word is the bottom pixel of the column. Words 241-256 of the records contain no useful information since the total picture is only 240 elements long.

Figure 17 illustrates the file structure pictorially.



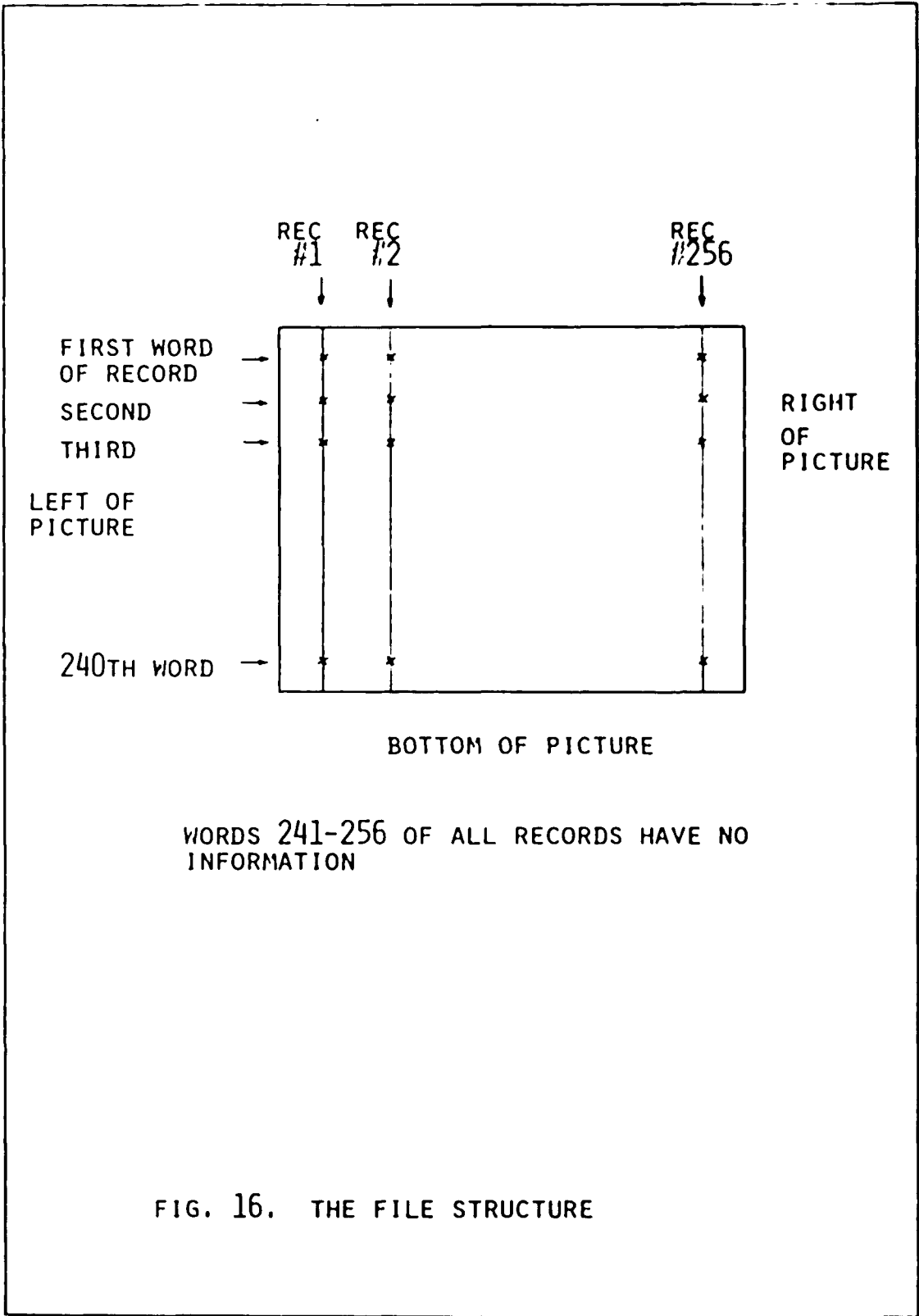


FIG. 16. THE FILE STRUCTURE

## 6.2. Program 'TVIN'

Function: Inputs, digitizes and stores on disk  
240 x 256 samples of a TV picture.

How to run it: RU, TVIN, ILU (where ILU is the  
logical unit number of the terminal)

Input to program: File name, LU number of A/D  
interface card, channel number.

Output: Type 2 file of given name on cartridge 13.

Time to run: Approximately 10 seconds.

Name of program file: & TVIN

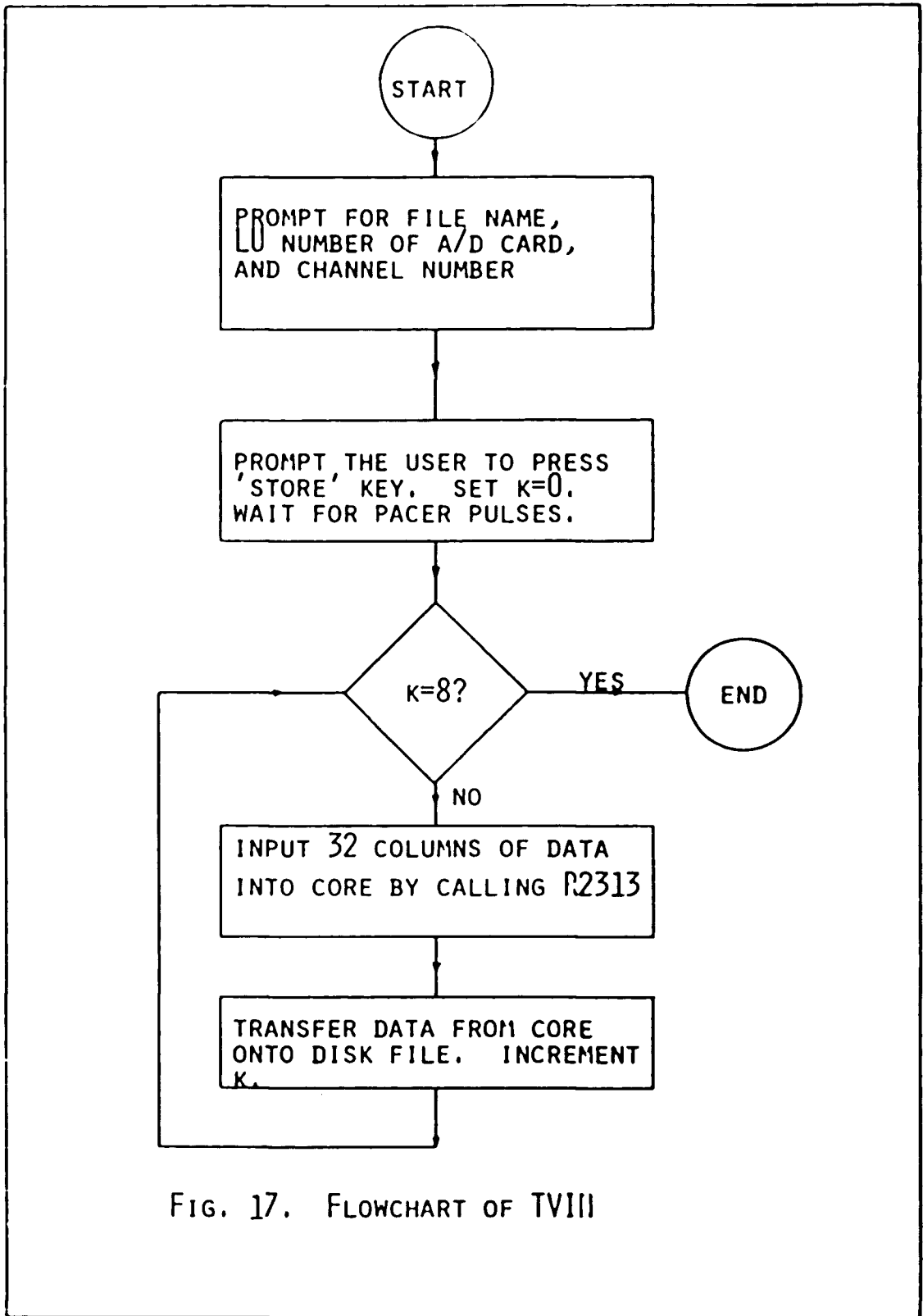


FIG. 17. FLOWCHART OF TVIII

### 6.3. Program 'TVOUT'

Function: Displays the picture samples from a type 2 disk file, as specified previously, on a TV monitor.

How to run it: RU, TVOUT, ILU (where ILU is the logical unit number of the terminal).

Input to program: File name, LU number of display card, writing sense (white-on-black display or vice versa) information, a black-to-white threshold number.

Output: Display of picture on standard TV monitor in only black and white dots (no shades of gray).

Time to run: Approximately 3 seconds.

Name of program file: &TVOUT

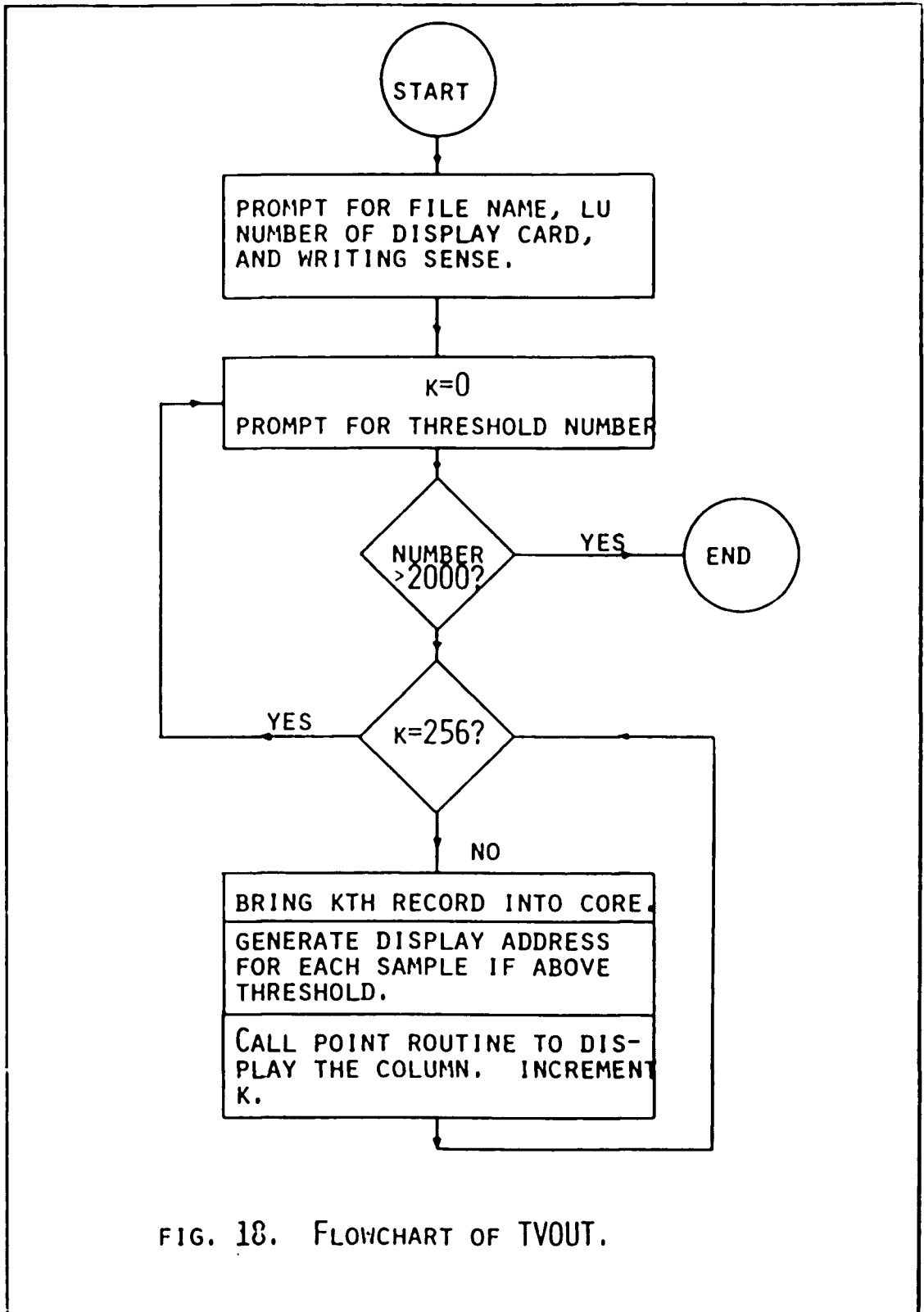


FIG. 18. FLOWCHART OF TVOUT.

## 7. THE FINAL PRODUCT

### 7.1. Evaluation of the System and Possible Improvements

Time to Store: The system takes about 10 seconds to store a picture frame. This sounds somewhat large but considering the fact that we are using a 20 KHz A/D converter to process a 5 MHz video signal and that we attempted to design an inexpensive system, this amount of time can be partially justified.

However, it may not really be necessary to stop the scan while main memory to disk transfer of data is taking place and a deeper look into the system software could reveal the possibility of data transfers in parallel with data input. Such a scheme would cut the storing time to about 5 seconds.

Resolution of the Picture: The resolution of the digitized image seems to be reasonable although no measurements have been made. The S/H amplifier being used is rated to have a 4  $\mu$ S acquisition time with a capacitor of 1000 pf. In order to achieve an acquisition time of  $\leq 200$  nS, we chose to use a capacitor of 38 pf. Whether that really brings down the acquisition time into the desired range or not should be investigated.

Quality of Picture: The picture is not uniform while in the areas where it should be. It has dark serrations interleaved with some regularity. This seems

to have to do with the imperfect decoupling of the power supply bus at various points, especially near the S/H amplifier. Some improvement can be made in this area.

Software: The present software is compatible with a single board display system. It can be upgraded to have the option of 1, 2 or 3 boards which will make it possible to display various shades of gray or a colored picture.

Figure 19 is an example of the picture reproduced from the stored data.

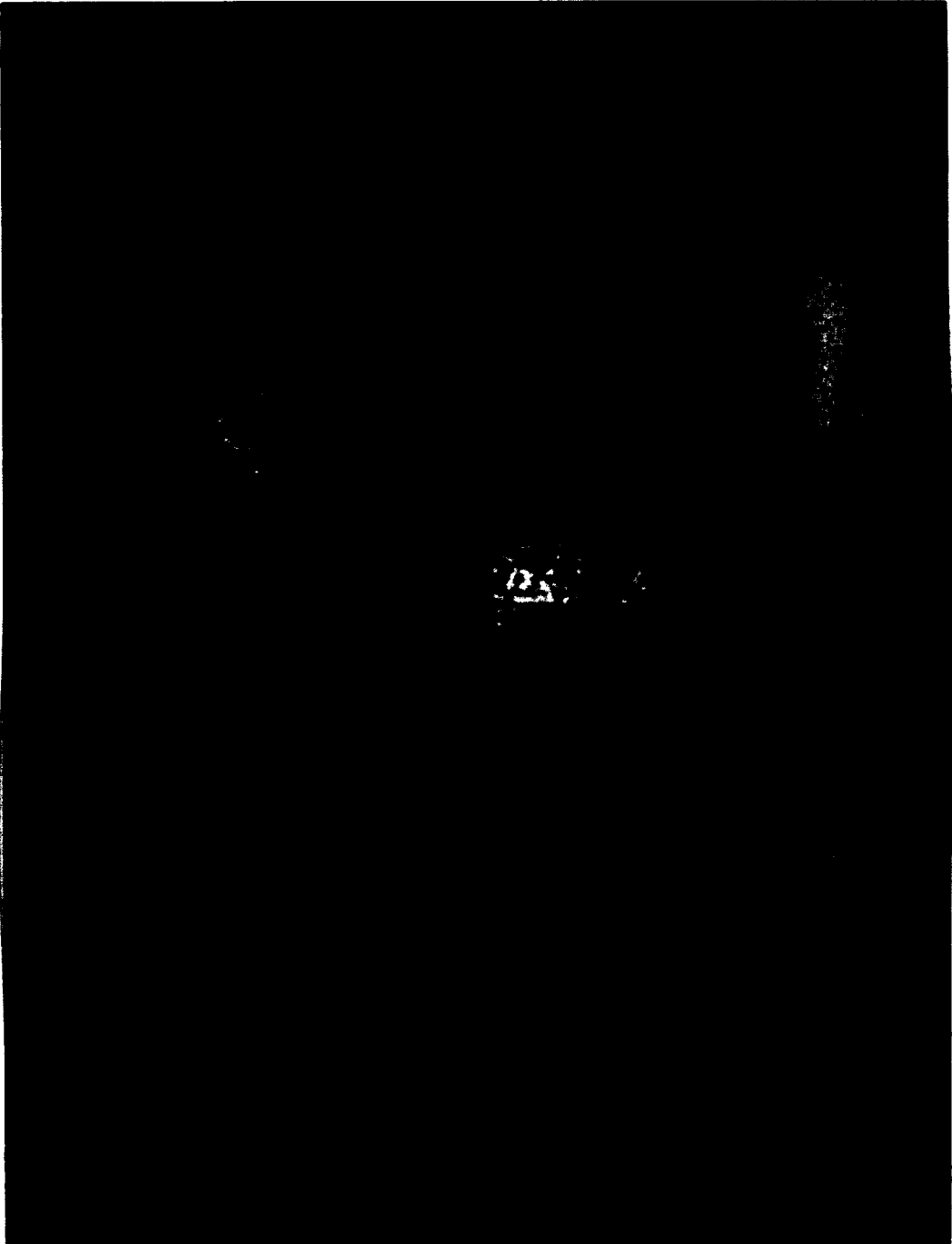


FIGURE 19. DISPLAY OF A STORED PICTURE.



## 8. LIST OF REFERENCES

1. Kerkhof, F., and Werner, W., Television, London: Philips Technical Library, 1952.
2. Reference Manuals, Hewlett-Packard, HP-1000 computers.

## 9. APPENDICES

### 9.1. Output Specifications of TV Interface Subsystem in Mode I

(Refer to Figure 5)

Lines per Frame	525
Lines per Field	262.5
Fields per Frame	2
Frames per Second	30
Fields per Second	60
Interlace	2:1
Lines of Data Field	240
Horizontal Scan Rate	15750
f	1.587 $\mu$ S
s	4.762 $\mu$ S
b	6.349 $\mu$ S
H	63.492 $\mu$ S

## 9.2 Characteristics of S/H 703

( $C_H = 1000 \text{ pF}$ ;  $V_S = \pm 15\text{V}$ )

### ACCURACY

Non-linearity ( $-55^\circ\text{C}$ to $+125^\circ\text{C}$ )	.003%
S/H Offset	2 mV
Bias Current	50 nA

### INPUT/OUTPUT

Input/Output Ranges	10 V Min
Input Impedance	10 Meg
Output Impedance (Hold Mode)	5 $\Omega$
Output Current	10 mA Min 10 mA Min

### MODE CONTROL

DTL/TTL Compatible

### DYNAMIC RESPONSE

Acquisition Time (10 V)	4 $\mu\text{sec}$ to .1%
Slew Rate	5 V/ $\mu\text{sec}$
Droop Rate ( $25^\circ\text{C}$ )	50 mV/sec Max
Aperture Time	50 ns
Aperture Uncertainty	5 ns
Gain Bandwidth Product	2 MHz

### POWER SUPPLY

Current	5 mA
Rejection Ratio	90 dB

### 9.3 Signals on the 44-pin Connector

<u>SIGNAL</u>	<u>PIN NUMBER</u>
+13 V	1, 2, 3
Ground	4, 5, 6
-13 V	7
Video input	9
'STORE' Key (end connected to the monoshot)	10
'STORE' Key (end connected to 330-ohm resistor)	11
Pacer Output	13
Video Output	15
'STORE' L.E.D.	17
'POWER' L.E.D.	19
+5 V	20

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