Low frequency admittance measurements on thin oxide MOS capacitors.

David W. Greve

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LOW FREQUENCY ADMITTANCE MEASUREMENTS ON
THIN OXIDE MOS CAPACITORS

by
David W. Greve

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Professor in Charge

Chairman of Department
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ABSTRACT

A new instrument has been developed for low frequency admittance measurements on MOS devices with substantial DC conductance. The operation of the instrument has been demonstrated under conditions where \( G \sim 100 \mu\text{C} \). This is two orders of magnitude more conductance than can be tolerated with the standard lock-in amplifier technique.

It is found that the admittance of thin oxide MOS devices becomes inductive at low frequencies. This effect is tenatively attributed to the AC tunneling current. A simple equivalent circuit for the tunneling admittance is proposed, and it is shown that a good fit to the observed frequency dependence can be obtained.
I. Introduction

C-V measurements on MOS capacitors are widely used to determine the surface potential and surface state densities. These parameters are necessary in order to compare present theories of current transport with experiment. However, these measurements are difficult in the presence of substantial DC conductance, particularly at the low frequencies necessary to ensure that all surface states are in equilibrium.

None of the commonly used methods of measuring admittance work well at low frequencies when the conductance is much larger than the capacitive susceptance. In this thesis, a new method of measurement which works under these conditions is described. First, however, the limitations of presently used techniques will be discussed.

II. The Conventional Admittance Bridge

One possible bridge arrangement for admittance measurements is shown in Fig. 1. This is not the circuit used in commercially available bridges such as the Boonton model 75C, but the limitations to be described apply to any bridge using a null detector which responds to the magnitude of the out of balance signal.

The imbalance voltage $V_{ab}$ can be obtained by voltage
division as
\[ V_{ab} = \left[ \frac{1}{2} - \frac{G + i\omega C}{G + G_m + i\omega(c + C_m)} \right] V_g \sin \omega t \]

When the bridge is near balance, the imbalance voltage becomes
\[ V_{ab} \approx \frac{\partial V_{ab}}{\partial G} \bigg|_{G=G_m} \Delta G + \frac{\partial V_{ab}}{\partial C} \bigg|_{C=C_m} \Delta C \]
\[ = \left[ \frac{1}{4(G_m + i\omega C_m)} \Delta G + \frac{i\omega}{4(G_m + i\omega C_m)} \Delta C \right] V_g \sin \omega t \]
where \( \Delta C \) and \( \Delta G \) are the deviations from exact balance.

Specializing to the case when \( Y_m \), the admittance to be measured, has large conductance \( (G_m \gg \omega C_m) \) the imbalance voltage becomes
\[ V_{ab} \approx \left[ \frac{\Delta G}{4G} + \frac{i\omega \Delta C}{4G} \right] V_g \sin \omega t \]

The null detector responds to the magnitude of the applied signal. Thus the meter indication is given by:
\[ I \sim |V_{ab}| = \sqrt{\left( \frac{\Delta G}{4G} \right)^2 + \left( \frac{\omega \Delta C}{4G} \right)^2} \cdot V_g \]

Suppose it is desired to obtain a given resolution in the measurement of capacitance. The detector must then be able to detect an imbalance signal of the magnitude caused by an imbalance \( \Delta C \), where \( \Delta C \) is the desired resolution. This means that the detector must be able to resolve signals at least as small as
\[ V_{\text{min}} < \frac{\omega \Delta C}{4G} \cdot V_g \]
In addition, this imbalance due to the capacitance can only be seen if it is not masked by the imbalance voltage due to the conductance. This requires that the first term in the square root be less than the second. This in turn requires the conductance be adjusted to give

$$\frac{\Delta G}{G} < \frac{\omega \Delta C}{G}$$

Both of these requirements are difficult to satisfy at low frequencies. There is a practical limit to the resolution available in variable resistors. In addition, as the frequency becomes lower, the detector must be made more sensitive.

In practice, it is difficult to make measurements at 5 KHz when the conductance is larger than $10^{-4} \Omega$. Commercial admittance bridges suitable for MOS measurements are not available below 5 KHz.

III. The Lock-in Amplifier Technique

Another technique, using the lock-in amplifier, has been used for measurements on thick MOS capacitors at very low frequencies—down to about 1 Hz. The method is an adaptation of that originally described by Shewchun and Waxman. The use of a lock-in amplifier permits the separation of an input voltage into a component in
phase with a reference signal, and a component which is out of phase. In addition, the narrow noise equivalent bandwidth permits the detection of very small signals.

A simplified block diagram of a lock-in amplifier is shown in Fig. 2. The analysis of the operation of the lock-in amplifier given below is simplified, although it gives the correct result. A more complete analysis can be found elsewhere.²,³

In the lock-in amplifier, noise immunity and phase resolution are obtained by using phase sensitive detection. This requires a reference signal at the same frequency as the signal of interest.

Consider first the case when the phase shift in the reference channel is zero. The mixer is designed to give an output signal which is the product of the two input signals. Thus the voltage at the output of the mixer is

\[ V_m = A \sin^2 \omega t + B \sin \omega t \cos \omega t \]

Using trigonometric identities, this can be rewritten as

\[ V_m = \frac{1}{2} \left[ A - A \cos 2\omega t + B \sin 2\omega t \right] \]

If the time constant of the low pass filter is long compared to \(1/\omega\), the second harmonic components will be filtered out and the output voltage will be

\[ V_0 \sim \frac{A}{2} \]
That is, the output voltage is proportional to the component of the input voltage which is in phase with the reference signal. Similarly, one may measure the out of phase component by setting the phase shift to 90°.

In practice, it is not possible to obtain complete separation of the two components of the input signal. Imperfections in the mixer and the phase shifter limit the separation which can be achieved.

First, consider the effect of a slight misadjustment of the phase Δφ. This could be due to drift in the component values or limited resolution in the phase adjustment. The output of the phase shifter will then be

\[ V = \sin(\omega t) + \Delta \phi \cos(\omega t) \]

This causes the appearance of a small component of the undesired signal at the output

\[ v_o \approx \frac{A}{2} + \frac{B}{2} \Delta \phi \]

where Δφ is given in radians. Typically, the phase error is about .1 degree, so the orthogonal component will be attenuated by a factor of approximately 2 x 10^{-3}.

In addition, the mixer has a limited dynamic range. If the total signal applied to the mixer exceeds the maximum allowable signal, the mixer operation becomes non-linear. The maximum allowable input signal depends on the design of the mixer, and may be from 10 to 1000 times full scale sensitivity. In almost all cases, however, the
limiting factor is the accuracy of the phase adjustment.

C-V measurements are used using the circuit shown in Fig. 3. The operational amplifier circuit produces an output voltage proportional to the current flowing into the input terminal. Simple analysis shows that the output voltage is \( V_o = -RI \) and the input impedance is approximately \( R_{in} \approx R/A \), where \( A \) is the gain of the amplifier. Since \( A \) is large, the input impedance is small and the input terminal is at virtual ground. Thus, the voltage applied to the input of the lock-in amplifier is

\[
V_{in} = -R \eta (G + j\omega C) \sin \omega t
\]

It was shown above that either component of the input voltage can be measured separately by suitable adjustment of the phase shifter. Thus the conductance and the capacitance can be measured independently.

In practice, the phase error limits the amount of conductance which can be tolerated when measuring capacitance. For an accuracy of \( .2\% \) in the capacitance measurement, \( G \) must satisfy the inequality

\[
G < 1.2 \omega C
\]

Fig. 5 shows the maximum allowable conductance as a function of frequency for the two techniques discussed above. Conductances less than the maximum will permit the measurement of a 100 pf capacitor to better than \( .2\% \). Also shown is the region accessible with a new technique to be
described below.

IV. The Lock- in Bridge

A. Previous Work

Recently, Barret and Vapille\textsuperscript{4} suggested a modification of an admittance bridge which allowed measurement at low frequencies when the conductance is large. In their method, shown in Fig. 4, a lock-in amplifier is used as a null detector in a bridge. In operation, the resistor $R$ is adjusted until the in phase component of the voltage $V_{ab}$ is zero; then the capacitance is obtained from the magnitude of the out of phase voltage and the value of $R$. This can be seen by writing the equation for the voltage $V_{ab}$:

$$V_{ab} = \left[ \frac{1}{2} - \frac{1}{1 + RG + j\omega RC} \right] V_g \sin \omega t$$

When the conductance is large ($G \gg \omega C$), this can be expanded to give:

$$V_{ab} \approx \left( \frac{1}{2} - \frac{1}{1 + RG} \right) V_g \sin \omega t + \frac{\omega R G}{(1 + RG)^2} V_g \cos \omega t$$

At balance, $R = 1/G$ and the in phase component is zero. The capacitance can then be obtained from

$$C = \frac{\sqrt{V_{ab} \text{ (out of phase)}}}{\omega R V_g}$$
In order to obtain a measurement of the capacitance it is necessary to know two quantities: the out of phase voltage and the resistance $R$. This is a problem since $R$ must then be a precision variable resistor with low stray capacitance. In addition, since the null detector is a high impedance device, the stray capacitance across its input is troublesome. This stray capacitance has the effect of causing a phase shift between the reference signal and the input signal to the lock-in amplifier, even if there is no capacitance in parallel with $G$.

B. Modified Lock-in Bridge

The modified bridge shown in Fig. 6 was developed in this thesis to eliminate the problems discussed above. The detector $D$ is a current sensitive detector of the type used in conventional lock-in capacitance measurements. As before, the output of this detector is connected to the input of the lock-in amplifier.

The operation of this circuit becomes more transparent when the two node pairs a-n and b-n are replaced by their Thevenin equivalents. This is shown in Fig. 7. For the special case $R' \ll R$, the detector current $i_d$ reduces to

$$i_d = \left( \frac{1}{R} - G \right) \nu \sin\omega t + \omega C \nu \cos\omega t$$

As before, the variable resistor $R$ is adjusted to
bring the in phase component of the current to zero. The capacitance is then obtained directly by measurement of the out of phase component. It is no longer necessary to know the value of R precisely. In addition, since the approximation $G \gg \omega C$ is not made, the method permits capacitance measurements even when the conductance becomes small. This is not the case in the bridge described by Barret and Vapille.

As always, the implementation of this method is not as simple as the circuit diagram would suggest. It is necessary to bias the MOS device without disturbing the measurement. In addition, stray capacitance effects and the proper choice of ground point need to be considered.

C. Grounding

The choice of the ground point is often a problem in AC impedance bridges. This is because the detector and the generator cannot have a common ground, yet both require DC power. In the bridge described above, it is also necessary to transmit phase information from the generator to the lock-in amplifier.

The most natural point to place the ground is the end of the current sensitive detector which is not connected to the sample. This is convenient since the lock-in amplifier and the current sensitive detector must share
a common ground, and the lock-in is already grounded through the power line. This choice also has the effect of reducing the error due to the stray capacitance. This can be seen in Fig. 8. Since the sample is mounted some distance from the bridge, it is necessary to connect it to the bridge with coaxial cables. The stray capacitance introduced by these cables appears across either the current sensitive detector or one of the resistors $R'$. Since both of these represent low impedances, very little current flows in the stray capacitors, and the measurement is unaffected.

The reference signal for the lock-in amplifier is obtained from a grounded signal generator. The signal to drive the bridge is obtained from an optical isolator which is also driven by the signal generator. The circuit of the isolator is shown in Fig. 9. The use of a commercial optocoupler in the linear mode permits different grounds on each side while still preserving phase information. An emitter follower is used as an output stage to provide an output impedance of less than 1 ohm.

In conventional bridges, transformers are used to lift the signal above ground to excite the bridge. In this case, however, the phase shift through the transformer would vary with load and thus cause errors in the measurement.
D. Biasing

For simplicity, the provisions for producing and measuring the bias on the MOS device were omitted from Fig. 6. These arrangements are shown in Fig. 10. The network consisting of the 15 ohm resistor in series with the generator ground together with the 500 ohm resistor approximates a voltage source while decoupling the bias supply from the bridge.

The bias is monitored with a digital voltmeter connected as shown through a 100KΩ resistor. Since the impedance to ground at that point is low, a negligible amount of AC current flows through the voltmeter. Thus it does not disturb the measurement and can be connected continuously.

E. Variable Resistor

The variable resistor R is crucial to the performance of the bridge. It must be stable and adjustable over a wide range of resistance. In addition, the stray capacitance must be low and preferably independent of resistance. Since R does not appear in the expression for C, however, it is not necessary for it to be calibrated precisely.

The conditions above are not satisfied by most available types of variable resistors. Common ten-turn
potentiometers have a large inductive reactance even at 100 Hz. The stray capacitance of a typical carbon composition potentiometer varies by about 3 pf over the full range of resistance. This would necessitate large corrections in the measured capacitance.

It was found that the common cadmium sulfide photocell forms an almost ideal variable resistor for this purpose. The admittance of two photocells connected in series was measured at 5 KHz with a Boonton capacitance bridge, and it was found that the stray capacitance varied less than ± .1 pf over a resistance range from 10 MΩ to 20 KΩ. The resistance is easily changed over this range by varying the current through an LED which shines on the photocells. This arrangement has the further advantage that the bridge is balanced by adjusting a voltage. Thus, it is easy to adapt the bridge for automatic balancing.

The conductance can also be obtained by measuring the voltage which appears across a resistor in series with the LED. The dependence of the conductance on this voltage is shown in Fig. 11.

F. Calibration

The accuracy of the measurements depends on the care with which the bridge is adjusted initially. In particular, the initial phase adjustment is crucial.
The phase adjustment is performed by connecting a 100KΩ resistor in place of the sample, and then deliberately unbalancing the bridge. This causes a current through the detector which is completely in phase with the generator voltage. The phase shift is then adjusted to give zero out of phase voltage at the lock-in amplifier. The calibration constant for the capacitance is then determined by replacing the resistor with a known capacitance.

G. Limitations on Accuracy

The ultimate accuracy of the capacitance measurement is limited by different factors depending on whether the measured capacitance is near full scale or near zero. When the reading is near full scale, the accuracy is limited by the resolution of the digital voltmeter which is used to measure the output voltage, and the \( \pm 0.1\% \) linearity of the lock-in amplifier. For small capacitance, the errors due to inaccuracy in the jig capacitance measurement and the stray capacitance of the variable resistor are dominant. From these considerations the accuracy was expected to be within \( \pm 0.2\% \), \( \pm 0.1 \) pf, independent of G.

The accuracy of the bridge was tested in two ways. First, parallel R-C combinations were measured on both
a conventional bridge and on the lock-in amplifier bridge. The conventional bridge (Boonton model 75C) was used at 5 KHz with a large exciting voltage to increase the accuracy. The R-C combinations used were metal film resistors in parallel with their own stray capacitance. Conductances up to $5 \times 10^{-5}$ \( \Omega \) were used, and measurements were made at 200 Hz, 500 Hz, and 1 KHz. In all cases the capacitances measured agreed within $\pm \, 0.1$ pf. Data taken for this test at 500 Hz is given in Table 1. Measurements were also made with fixed mica capacitors in parallel with the resistors. These measurements showed that the data was reproducible within $\pm \, 0.1\%$ and that the out of phase voltage was linearly related to the capacitance.

As a further test a thin oxide MOS device was measured at 5 KHz and 10 KHz using both types of bridge. The measurements agreed within the expected accuracy except in depletion where the lock-in bridge gave results that were consistently 0.2 pf low. This error can be attributed to a slight error in the measurement of the jig capacitance. The data taken for this test is presented in Table 2.

In practice, the measurements at low frequencies were limited in accuracy by noise due to imperfect contact with the wafer. This noise also caused difficulty at 5 KHz with the conventional bridge and significant
noise was noted when measuring the I-V characteristic. This problem can be eliminated by using samples mounted in headers or by using gold-plated probes.

The accuracy in the measurement of conductance is limited by the accuracy to which the calibration chart (Fig. 11) can be read. This accuracy is at least ± 5%. At present only conductances larger than $10^{-7} \Omega$ can be measured.

H. Automatic Balancing

When doing measurements on MOS devices with the lock-in bridge, it is generally necessary to readjust the variable resistor $R$ at each bias voltage. This can be done manually, by adjusting the voltage applied to the LED; or electrically, by means of a feedback loop. The second method is of particular interest since it permits simplified operation and also direct plotting of the results.

Since the variable resistor is controlled electrically, it is possible to arrange the bridge for automatic balancing if outputs proportional to both the in phase and the out of phase components are available. Both these outputs are available on the Princeton Applied Research model 129A two-phase lock-in amplifier. This instrument contains an additional mixer and a 90° phase
shifter, as shown in Fig. 12.

The circuit arrangement for self balancing operation is shown in Fig. 13. The out of phase signal is amplified and used to control the current flowing through the LED. If the correct sign is chosen for the amplifier gain, and if the feedback loop is stable, the effect will be to bring the bridge to balance. It was found experimentally that a 300 sec time constant for the lock-in low pass filter provided adequate loop stability down to 100 Hz. The requirements for stability of the feedback loop are discussed qualitatively in the Appendix.

V. Sample Preparation

Thin oxide MOS capacitors were prepared from <111> orientation, 1 ohm-cm n-type silicon wafers. The wafers were cleaned by boiling for 5 minutes in trichlorethylene, methanol, and acetone. After a deionized water rinse, the wafers were again boiled for 5 minutes in a 25% H₂SO₄ in H₂O₂ solution. Two cleaning oxidations in steam at 1130 °C were performed, for 30 and 15 minutes. After stripping the oxide in dilute HF, the final oxidation was performed.

The final oxidation was done in dry oxygen at 779 °C. The oxygen flow rate was greater than 200 cc/min. Oxidation times from 1 to 10 minutes were used, but good
samples were obtained only for the 7 and 10 minute oxidations. For both of these wafers the oxide capacitance was about 140 pf, corresponding to an oxide thickness of about 30Å.

Chromium dots of area $1.27 \times 10^{-4}$ cm$^2$ were evaporated onto the wafers in an ion-pumped vacuum system. The pressure during the evaporation was less than $10^{-7}$ torr. The back oxide was then removed and an aluminum layer evaporated to form the back contact.

VI. Measurements

A. Experimental Technique

The wafers were placed on a gold plated stage and the dots were probed with a tungsten tip mounted to a micropositioner. All measurements were performed in darkness and at room temperature. Raising the probe and setting it down again on the same dot changed the 1 MHz conductance, suggesting that the contact was imperfect. In addition, the 1 MHz capacitance was about 1% less than the 50 KHz capacitance in accumulation. This is consistent with a series resistance of about 200 ohms.

The C-V and G-V characteristics were measured over a range from 40 Hz to 1 MHz. Measurements above 5 KHz were made using commercial admittance bridges (Boonton...
models 75C and 75A). For measurements below 10 KHz the lock-in bridge described above was used. The I-V characteristics were also measured using a Keithley model 610B electrometer.

B. Results

A plot of the measured C-V data for a sample with a 7 minute oxide is shown in Fig. 14. The most striking feature is a dip in the 5 KHz capacitance at -.9 volts reverse bias. The 5 KHz capacitance at this bias is less than the 1 MHz capacitance.

At 5 KHz, measurements were made with both the Boonton bridge and the lock-in bridge. A dip in the 5 KHz capacitance below the 1 MHz capacitance is seen in both sets of data. In addition, the two sets of data agree within the expected experimental error. The magnitude of the observed dip is about 10 times the experimental uncertainty for the lock-in bridge, and 50 times the experimental uncertainty for the Boonton bridge.

At 500 Hz, measurements on the lock-in bridge show that the admittance becomes inductive, and a peak in the inductive admittance occurs at the same bias as the dip observed at 5 KHz. The capacitance curves all come together in accumulation, as they normally do.

The conductance as a function of bias for this sample is plotted in Fig. 15. It can be seen that the
conductance is essentially the same at 500 Hz and 5 KHz. In addition, the conductance at these frequencies is approximately the same as the DC conductance.

The observation of an inductive imaginary part is sufficiently surprising to cast doubt on the measurement technique. As noted, however, the inductive admittance peaks at the same bias as the dip in the 5 KHz capacitance, and that dip is observed in measurements made with two different instruments. In addition, the lock-in bridge was demonstrated to give correct results with R-C combinations at the same frequency at which the inductive admittance is observed. For these reasons, it was concluded that the effect was real and not due to measurement errors.

Experimental results for two additional samples are shown in Figs. 16-19. These measurements show an effect qualitatively the same as that discussed above.

C. Previous Work

So far as is known, a net inductive admittance in an MOS device has not been reported in the literature. However, some data is available which shows a dip in the low frequency capacitance similar to that observed here.

Kumar\textsuperscript{5} has observed a dip of 5 KHz capacitance below the high frequency capacitance in some thin oxide samples. This was attributed to incorrect sample preparation.
In addition, structure which could not be attributed to surface states was observed at 39 Hz in some thin oxide capacitors with aluminum metallization. Although the capacitance did not become less than the high frequency capacitance, the structure occurs at the beginning of deep depletion, as does the effect observed here. The dip was attributed by one of the authors to majority carrier effects, although no detailed analysis was presented.

Measurements made with a preliminary design of the lock-in amplifier bridge showed an inductive admittance at 500 Hz in some samples which had been prepared by Kumar. The samples displayed normal C-V characteristics down to 5 KHz, and had in fact been used in a study of I-V and noise characteristics. In these samples, the inductive admittance was also observed at the beginning of deep depletion. At that time, the effect was attributed to a defect in the measurement technique.

Table 3 summarizes the samples in which an inductive contribution to the admittance has been observed. In all cases, the oxides were thin and there were substantial tunneling currents. In addition, the out of phase AC current was always much smaller than the in phase current \((G>>\omega C)\). It is well known that such an inductive contribution is never observed in thick oxide MOS devices. This suggests that the presence of the inductive contribution is related to the presence of substantial tunneling
current. If the tunneling current lagged the applied AC voltage by a small angle, this would appear as an apparent inductive contribution to the admittance.

In summary, the anomalous inductive contribution observed here has also been observed by other workers. It had been observed, however, only at low frequencies and in the presence of large DC conductance. Previous measurement techniques were difficult to use under these conditions. The new technique described in this work unambiguously establishes the presence of this inductive contribution.

D. Analysis of Data

As discussed above, it is plausible to associate the inductive contribution with the tunneling admittance. It is useful, then, to look for a simple equivalent circuit which models the observed behavior. In that model, the tunneling admittance will have an imaginary part.

The tunneling admittance can be represented either as a sum of a real and an imaginary part, or, in polar coordinates, as a magnitude and a phase angle. The second representation is used below in order to emphasize the fact that the tunneling admittance is predominantly resistive.

It can be seen from the C-V curves that little
additional dispersion is observed for reverse bias less than -.9 volts when the frequency is below 15 KHz. This suggests that the dispersion due to surface states is also small for reverse bias larger than -.9 volts. Thus the observed dispersion should be entirely due to the tunneling admittance.

The imaginary part of the tunneling admittance can be extracted from the data by subtracting the low frequency capacitance from the measured capacitance at 15 KHz. The imaginary part of the tunneling admittance is then related to the capacitance dispersion $\Delta C$ through

$$\beta = \omega \Delta C$$

The real part of the tunneling admittance is just the measured conductance. The phase of the tunneling admittance at a frequency $\omega$ can then be calculated through

$$\phi(\omega) = -\tan^{-1} \frac{G}{\beta}$$

It is found that the conductance depends only very weakly on frequency in the range where the inductive contribution is significant. Thus the DC conductance can be used in the above calculation with small error.

The resulting phase is plotted as a function of frequency for several different bias voltages in Fig. 21 for the data of sample 2. The solid lines are a fit to an equation of the form:
This equation is the simplest form that satisfies the requirement that the observed phase shift go to zero for both high and low frequency. It can be seen that the fit to this equation is good, and that all bias voltages can be fit with the same value of \( \gamma \).

The above frequency dependence of the phase shift is obtained when the tunneling admittance is of the form

\[
\gamma_t = G_1 + G_2 \frac{1}{1 + \frac{1}{G_0} \omega t}
\]

where \( G_1 \gg G_2 \). Alternatively, an equivalent circuit can be constructed as shown in Fig. 22. The equivalent circuit for the tunneling admittance has three independent parameters \( G_1 \), \( G_2 \) and \( \gamma \). The conductance for zero frequency must equal the DC conductance, so one finds

\[
G_{dc} = G_1 + G_2
\]

The remaining two parameters can be obtained from the maximum phase shift and the frequency at which the maximum phase shift occurs:

\[
G_2 = G_{dc} \tan \phi_{max}
\]

\[
\gamma = \gamma_{max}
\]

The values of the parameters \( G_1 \), \( G_2 \) and \( \gamma \) obtained for sample 2 are given in Table 4.

Thus an equivalent circuit has been constructed with three frequency-independent elements. Of the two adjustable parameters, only one, \( G_2 \), depends on bias.
VII. Conclusions

A new measuring system has been developed to measure MOS admittance at low frequencies in the presence of large tunneling currents. The accuracy of this system has been verified by the measurement of R-C combinations and also by comparison with measurements of an MOS device obtained on a conventional bridge.

In previous studies of thin-oxide MOS devices, it had been assumed that the effect of tunneling could be represented by a pure conductance for small AC signals. The data presented here show that a complete description requires that the tunneling admittance have an imaginary part. The contribution of the imaginary part is significant only in depletion and when G >> ωC. Re-examination of data obtained in previous studies showed that this effect had been observed before. At present, an adequate theoretical explanation of this imaginary part is not available.

The occurrence of this effect is unfortunate as far as the determination of surface potential and surface state densities are concerned. This is because the inductive contribution to the admittance completely obscures the dispersion due to the surface states at low frequencies. An adequate theoretical explanation, however, may permit the extraction of useful information...
from the tunneling admittance.

Further experimental studies of this effect are desirable. Studies of the dependence of the inductive contribution on oxide thickness and temperature would aid in determining whether it is correct to associate the inductive contribution with the tunneling admittance.
In the automatic balancing mode, negative feedback is used to maintain the bridge in a balanced state. The stability of a given feedback arrangement can be investigated using any of the standard methods of control theory. Here, examination of the Bode plot is used to obtain an indication of the stability.

First, the system is redrawn in block diagram form. This is shown in Fig. 23. Only the signal path for the in phase component is shown. The lock-in amplifier is characterized by a transfer function
\[
\frac{\nu_o}{\nu_i} = \frac{A_L}{(1+\tau_1^L)(1+\tau_2^L)}
\]
where \(T_1\) and \(T_2\) are the time constants of the two cascaded low pass filters in the lock-in.

The voltage controlled variable resistor \(R'\) is inherently nonlinear. However, for small variations around an equilibrium point, it can be represented by the transfer function
\[
G' = \frac{1}{R'} = \frac{1}{1+\tau_3^L}
\]
where \(T_3\) represents the finite response time of the cadmium sulfide photocell.

The sample conductance \(G\) will be regarded as the input to the system and the lock-in output proportional to the in phase signal will be regarded as the controlled variable.
Then the transfer function relating them can be obtained as

\[ \frac{V_0}{G} = \frac{RA_1a_2}{(1+sT_1)(1+sT_2)} \]

First the steady state will be considered. The steady state response can be obtained by using the final value theorem:

\[ V_0(t \to \infty) = \lim_{s \to 0} sV_i(s) = s \cdot \frac{RA_1a_2}{(1+sT_1)(1+sT_2)} \cdot \frac{G}{1 + \frac{RA_1a_2}{(1+sT_1)(1+sT_2)}} \]

Thus the input voltage to the lock-in will be minimized and the bridge will be driven to a balanced condition if \( RA_1a_2 \) is large.

However, the overall gain \( RA_1a_2 \) cannot be made arbitrarily large or instability will result. This can be seen by considering the response of the bridge to a small disturbing signal of frequency \( \omega \). These disturbing signals are always present in the form of noise. It can be shown that for a general transfer function of the form

\[ T(s) = \frac{G(s)}{1 + GH(s)} \]

exponentially growing solutions exist if the phase of \( GH < -180^\circ \) when the magnitude of \( GH \) is unity. Thus a simple test for the stability can be made by examining the Bode plot of the quantity.
Fig. 24 shows the plot obtained for $R_1A_2\frac{\gamma^j}{\omega}$ = $10^3$ and time constants of 1000, 10, and .1 sec. It can be seen that the phase shift at the unity gain point is $-120^\circ$ and thus the system is stable. However, increasing $R_1A_2\frac{\gamma^j}{\omega}$ by an order of magnitude to $10^4$ will result in a phase shift of $195^\circ$ at the unity gain point thus giving an unstable system.

The overall gain required is determined by the operating frequency. As the frequency is decreased, the lock-in gain must be increased to keep the capacitance signal near full scale. From the analysis above, it can be seen that the gain cannot be increased indefinitely. Thus there is a lower limit to the frequency of operation in the self balancing mode. This lower limit is determined by the time constants of the components in the feedback loop.
BIBLIOGRAPHY


4. C. Barret and A. Vapille, Solid-St. Electron. 18, 27 (1975)

5. V. Kumar, private communication.


7. The explanation is due to A. Epstein.


<table>
<thead>
<tr>
<th>Conductance mhos</th>
<th>Measured capacitance pf</th>
<th>Boonton bridge</th>
<th>LIA bridge</th>
<th>Capacitance error pf</th>
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Table 1. Comparison of measured capacitance of R-C combinations at 500 Hz
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Table 2. Comparison of Lock-in and Boonton bridge measurements at 5 KHz and 10 KHz
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(All samples were on n-type, 1 ohm-cm substrates)

Table 3. List of samples in which an inductive contribution to the admittance has been observed
<table>
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<tr>
<th>Bias</th>
<th>$G_{dc}(U)$</th>
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Table 4. Tunneling admittance parameters for sample 2
Fig. 1. Bridge circuit for admittance measurements

$$V_0 \sin \omega t$$

Fig. 2. Block diagram of lock-in amplifier

$V_{ln} = A \sin \omega t + B \cos \omega t$

$V_{ref} = \sin \omega t$

$V_m = \text{DC amplifier}$

$\phi = \text{phase shifter}$

$V_o$
Fig. 3. Circuit for capacitance measurements

Fig. 4. Lock-in bridge as proposed by Barret and Vapille
Fig. 5. Maximum allowable conductance as a function of frequency
Fig. 6. Modified bridge circuit

Fig. 7. Modified bridge with Thevenin equivalent sources
Fig. 8. Effect of coaxial cable stray capacitance

Fig. 9. Optical isolator circuit
Fig. 10. Bias arrangements
Fig. 11. Dependence of conductance on applied voltage
Fig. 12. Block diagram of PAR model 129A two-phase lock-in amplifier

Fig. 13. Bridge arrangement for self-balancing operation
Fig. 14. C-V data for 7-minute oxide--Sample 1
Fig. 15. G-V data for sample 1.
Fig. 16. C-V data for Sample 2
Fig. 17. G-V data for sample 2
Fig. 18. C-V data for sample 3
Fig. 19. G-V data for sample 3
Fig. 21. Phase shift of the tunneling admittance as a function of frequency.
Fig. 22. Proposed equivalent circuit for MOS device with tunneling
Fig. 23. Self-balancing bridge in block diagram form
Fig. 24. Bode plot of $|G_H(j\omega)|$ dB and $\phi$.
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