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A microprocessor-controlled home security/ intercom/control system.

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A MICROPROCESSOR-CONTROLLED
HOME SECURITY/INTERCOM/CONTROL SYSTEM

by

Robert L. Siegel

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

1979

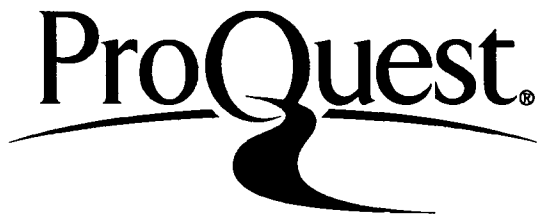
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This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

29 August, 1979
(date)

Professor in Charge

Chairman of Department

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ABSTRACT

This thesis describes a Microprocessor-Controlled Home Security/Intercom/Control System with Remote Terminals. The system is based on an Intel 8085 microprocessor with 4K of EPROM, 4K of RAM, a real time clock, memory mapped I/O, and full battery back-up. It supports up to sixteen remote terminals with room temperature monitoring, full intercom capability, two complete stereo receivers, ten channels of stereo speakers, all home heating and air conditioning control requirements, multiple burglar alarm switches, two smoke and fire detectors, and a roof siren.

The system is controlled by any of the remote terminals, which also serve as intercom stations and room temperature monitors. Each terminal has a sixteen-pad keyboard and ten individual LED'S for status display. Commands are entered via the keyboard and may be executed immediately; or at a specified time up to one week later.

The major functions of the system are:

1. Monitor Burglar Alarm switches on all doors and windows.
2. Monitor Smoke and Fire Detectors.
3. Monitor room temperature at any terminal and control heating and air conditioning.
4. Operate each Remote Terminal as a Master Intercom.
5. Control audio switching and attenuation for two independent stereo systems.
6. Control ten channels of stereo speakers.
7. Display desired system status at individual remote terminals.
8. Control Special Function outputs.
9. Self-checking of all system power supplies.
10. Self-checking of all system outputs.

This thesis describes the system architecture and hardware used to implement the Home Security/Intercom/Control System.

INTRODUCTION

The introduction of the 8-bit, general purpose, microprocessor by Intel Corp. in December 1971 [1], has lead to significant improvements in the area of electronic controllers. This device, along with its associated circuitry, has replaced many relay and hard-wired type controllers. The advantages of the microprocessor-based controller are: small size; large control capability; extremely fast operation; low operating power; ability to do calculations and store information for later use; ease of expansion; and software control of the functions. The ability to change the controller operation by changing only the software has been a main feature contributing to the success of microprocessor-based controllers.

As the above advantages indicate, the microprocessor controller is well suited to the controlling of multiple operations, such as those in a Home Security/Intercom/Control System (HSICS). The microprocessor controller, along with the additional versatility of remote interface terminals, produces a

system with readily available access to the controller's capabilities. It turns a simple security system into a sophisticated system with capabilities such as: automatic turn-on and turn-off of the intrusion alarm; easily changeable combinations to inhibit the alarm upon entry; the ability to ignore a status change of any intrusion switch; and the ability to display security status at any given time. The addition of a speaker and temperature sensor at each remote terminal further expands the capabilities. The speaker allows each remote terminal to operate as a master intercom station; to call or listen to any or all other stations. The temperature sensor at each terminal allows monitoring and control of heating and air conditioning from any terminal, as well as multiple automatic temperature set-backs. The system can be used to operate relays to control power and speaker loading to multiple stereo systems, and is expandable for future additions. It is obvious from the above discussions that a microprocessor is the best choice for a general purpose home controller, and this paper describes such a system.

The HSICS was implemented using the Intel 8085 microprocessor [2], advanced temperature sensors and other LSI devices; and is an example of a state-of-the-art microprocessor-controlled system.

Chapter 1

Functional Description

The heart of the Home Security/Intercom/Control System (HSICS) is the microprocessor. It transmits or receives information from all other elements of the system, and uses the received information in making calculations and decisions. Figure 1 shows a block diagram of the overall system.

The microprocessor receives interrupts from the real time clock, which allows it to keep track of time, and determines when scheduled functions are to be executed. It also communicates with all of the remote terminals via a 4-bit buffered I/O buss and 5 control lines. Information transfer to all hardware boards in the system is implemented via memory-mapped I/O. Internal CPU board I/O, which interfaces EPROM, RAM, and the SOL-20, is connected directly to the microprocessor buss; all off-board I/O signals are buffered and separated into independent input and output busses. All output signals have been implemented in such a manner as to allow read-back to

the microprocessor for data confirmation.

The Analog/Digital I/O Conversion board contains the D/A converter, analog level comparators, and the interface for the burglar alarm switches. It conveys alarm switch status to the CPU board, which also uses the D/A converter and level comparators to determine if all power supply levels are within normal operating range, and whether the smoke detectors have triggered. The drivers for the roof siren and trouble indicator LED'S, located at each remote terminal, are also located on this board.

The Low Level Audio Control board is used by the CPU board to control 4 channels of audio buffering, switching, and attenuation circuits; as well as a multi-tone modulated oscillator. This allows complete control for the amplifiers of two stereo systems.

The Intercom Control board contains all the necessary relays to allow the remote terminal speakers to be switched to intercom input or output, or to play background music from either of the stereo systems. An intercom preamp is also required to boost and clamp the speaker signal when used as an intercom input.

The Stereo Control board is used by the CPU to

control speakers for up to 10 stereo channels, which may be relay-connected to the outputs of the stereo amplifiers.

The Remote Terminals communicate with the CPU board via a 4-bit I/O buss and its control lines. Each terminal has an individual terminal address for CPU polling. Touching any pad of any 16-pad keyboard causes a common CPU interrupt. The CPU must determine which terminal caused the interrupt prior to data transfer. The status display LED'S may be updated by the CPU either by using the parallel select enable, which transmits information to all terminals, or by addressing a terminal individually. The temperature sensor at each terminal compares an internal signal to the CPU-controlled D/A converter output, and returns an above/below indication to the CPU. The D/A converter can be programmed to check any desired temperature.

The power for the system is derived from a 12 volt lead-acid storage battery which is constantly being charged by a line-operated supply. This single battery simplifies battery back-up operation, but necessitates power conversion via switching regulators for efficient system operation.

The system software, combined with the system hardware, provides the following capabilities to each remote terminal:

1. Enabling and disabling of the burglar alarm.
2. Displaying of: system status; individual alarm switch status; previously stored commands; or time and date in BCD.
3. Intercom and background music control.
4. Stereo receiver and speaker control.
5. Local control of heating and air conditioning.
6. Immediate or delayed execution of any function.
7. Security protection for specified functions.
8. Construction of a command file to execute any functions repeatedly at a specified time or interval.

Chapter 2

CPU Board

The CPU board generates a system reset pulse to all hardware, including the CPU, during power-up or manual reset. The reset pulse may also be generated under CPU control to try to clear a hardware malfunction.

Figure 2 shows a block diagram of the CPU board. the timing for the CPU is generated by a 5.00 MHz crystal and an on-chip oscillator. The buffered oscillator drives the real time clock which causes an interrupt every 200 ms.

The 8085 microprocessor multiplexes the 8 low-order address bits and the data bits on its I/O buss pins. The low-order addresses are valid early in the cycle and are latched using the address latch enable. The buss may then be used for reading or writing data during the remainder of the cycle. The 8 high-order address bits are also latched from the high-order address pins by the address latch enable. Each latch provides the necessary buffering for true/complement

outputs.

All CPU data transfers are implemented between RAM, EPROM, or memory-mapped I/O. The system contains 4K of EPROM, used for program storage, and 4K of RAM, which can be used for program or data storage. The address enable decoders use only the first 16K of address space and divide this space into 1K blocks. The allocation of the 1K blocks are as follows:

<u>SECTION</u>	<u>HEX ADDRESSES</u>	<u>FUNCTION</u>
0	0000 - 03FF	EPROM 0
1	0400 - 07FF	EPROM 0
2	0800 - 0BFF	EPROM 1
3	0C00 - 0FFF	EPROM 1
4	1000 - 13FF	EPROM EXPANSION
5	1400 - 17FF	EPROM EXPANSION
6	1800 - 1BFF	I/O
7	1C00 - 1FFF	SOL-20 INTERFACE
8	2000 - 23FF	RAM 0
9	2400 - 27FF	RAM 1
10	2800 - 2BFF	RAM 2
11	2C00 - 2FFF	RAM 3
12	3000 - 33FF	RAM EXPANSION
13	3400 - 37FF	RAM EXPANSION

14	3800 - 3BFF	RAM EXPANSION
15	3C00 - 3FFF	RAM EXPANSION

The 1K block of memory-mapped I/O actually contains only 64 individual addresses in a repetitive pattern; the SOL-20 interface block contains only 4. This is more than sufficient for all desired control functions and reduces the amount of address decoding. The memory-mapped I/O is further broken-down into discrete output strobes and input-pair strobes. All necessary addresses, enables and control signals, are buffered and sent off-board to allow expansion to the full 64 words of I/O. The CPU I/O buss is buffered to become the external data out complement buss and contains valid data for any I/O write. The buffered external data input buss is driven by tri-state 2-input multiplexers which determine the even/odd address for the input strobe pair. Address 0 of the I/O space is used to control the 4-bit open-collector I/O buss and outgoing control signals for the remote terminal. I/O address 0 is unique in that it is the only input address whose information resides on the CPU board. All other I/O address inputs use the external data

input buss, which is selected by not address 0. The interrupt line is used by the remote terminals to signal that an action has taken place that requires attention.

The SOL-20 interface mailbox has been implemented using 4 words of dual-port register files. This allows passage of 4 words of information in both directions; however, information written by the CPU can only be read by the SOL-20 and vice-versa. The SOL-20 also has the ability to generate a hardware interrupt to capture the CPU's attention.

Chapter 3

Analog/Digital I/O Conversion Board

The block diagram of the Analog/Digital I/O Conversion board is shown in Figure 3. The CPU output buss is buffered and inverted before going to each of the data latches. This is necessary to present true data to the latch inputs and only one unit load to the CPU output buss. All latched information can be read back to the CPU for data confirmation.

Data latched from I/O address 2, and the least significant half of 3, control the D/A converter. The 12-bit D/A has a voltage range of +/- 5.12 volts corresponding to a resolution of 2.5 mv. The other half of data latch 3 serves multiple functions: data bits 4 and 5 control the trouble indicator logic; data bit 6 controls the roof siren; and data bit 7 is the CPU-generated reset signal. The trouble indicator logic causes the trouble display LED'S, at each remote terminal, to operate in 1 of 4 modes: off; slow blink; fast blink; or on. This provides an indication range from normal operation to major system malfunction.

Each burglar alarm switch has one terminal connected to a reference supply and the other to a data bit on an input data multiplexer. The input is also pulled-up through a resistor to a second reference supply. The reference supplies can be programmed to either vcc or ground by data bits 0 and 1 of I/O address 1. Normal sensing of the alarm switches occurs with opposite states on the reference supplies; however, when both references are programmed identically, the state of the switches is ignored and proper operation of the input multiplexer can be confirmed.

Each voltage level of all system power supplies, including the alarm switch references, is sent to a separate comparator along with the D/A converter output, and the result may be read back to the CPU. This allows the CPU to actually measure any system voltage value and determine if it is within the normal operating range. Each of the smoke detector outputs is compared to a reference voltage to determine if it has triggered.

Chapter 4

Low Level Audio Control Board

The data latches on this board (See Figure 4) are buffered and have read-back capability as described for the Analog/Digital I/O Conversion board. The I/O addresses used for the Low Level Audio Control board are 4 through 7.

Data from I/O address 4 is used to control the stereo amplifiers; from 5 and 6, to control the intercom amplifiers which are used for intercom or background music. Data bits 0 through 5 of I/O address 7 are buffered and used as open-collector relay drivers, while data bits 6 and 7 control the multi-tone modulated oscillator. Relay drivers 0 and 1 control relays whose function are to supply AC power to the stereo and intercom receivers.

The multi-tone modulated oscillator can be operated in 1 of 4 modes: off; low tone; high tone; low/high warbled tone. The oscillator can be connected to the intercom amplifiers and used to signal that the intrusion alarm has been triggered and warns that the

alarm disable procedure should be implemented or the roof siren will be activated. The oscillator may also be connected to the stereo amplifiers, as well as the intercom amplifiers, to indicate that either of the smoke detectors have triggered, or a system malfunction has occurred. Another feature is to signal data entry at any of the remote terminals.

The preamp outputs of each channel of the stereo receiver and one channel of the intercom receiver are buffered by unity gain amplifiers to provide a constant load to the preamp output. A spare buffer also exists for future expansion. Each receiver channel is broken between the preamp and power amplifier to allow the insertion of the switching and attenuation control circuit. The normal configuration for the stereo receiver is to be tuned to FM stereo or playing stereo records or tapes. The normal configuration for the intercom receiver is to be tuned to an AM station.

The power amplifier sections of the stereo receiver are used to drive the stereo speakers; while the power amplifier sections of the intercom receiver use one channel for intercom A and the other channel for intercom B. This allows for two independent

selections of monaural background music at different remote terminals, or the same selection at different volumes. This is possible because the switching and attenuation control is independent for each channel of the intercom receiver.

The audio signals present at the 4 channel switching and attenuation circuits are provided by the unity gain buffers and the multi-tone oscillator. These signals may be gated individually by FET switches to the input of a second buffer amplifier whose gain can be programmed to 1 of 5 values. When using the intercom, channel B is disconnected from its power amplifier output and becomes the intercom input buss. The buss signal is amplified and becomes the intercom A power amplifier input. The output of the intercom A power amplifier is the intercom output buss and can be programmed to connect to any speakers not on the input buss.

Chapter 5

Intercom Control Board

The Intercom Control board block diagram is shown in Figure 5. The data latching and confirmation circuits are identical to those described for the previous boards. I/O addresses 12 through 15 control the 36 SPST reed relays used for intercom or background music at each remote terminal. Proper operation of the relays require that the power amplifier be in a quiescent state when relay switching occurs.

The first 14 channels of remote terminal speakers, located internally to the home, may be connected to the intercom A output amplifier or the intercom B output amplifier. The two remaining intercom channels share stereo speakers located at the front and back porch, and parallel the stereo channel speakers for intercom use. Each speaker has a 10 ohm resistor connected in series with it to reduce the amplifier loading when multiple channels are connected in parallel.

A preamp is required, when using the intercom, to boost the signal from the speakers on the intercom

input buss. The preamp is a transistor amplifier with a low frequency cut-off set above 60 HZ to reduce amplified pickup. The bandwidth of the preamp covers the normal voice range and has a diode-clamped output to prevent excessive input signal to the power amplifier.

Chapter 6

Stereo Control Board

The block diagram of the Stereo Control board is shown in Figure 6. The CPU output buss is buffered and inverted again to present true data to the latch inputs. The outputs of the data latches controlled by I/O addresses 8, 9 and 10 are buffered also to drive 40 SPST reed relays to control speakers for 10 stereo channels. I/O address 11 is reserved for future expansion. The buffered relay driver outputs and unbuffered spare outputs all may be read back to the CPU for data confirmation.

Each stereo speaker may be connected to its associated power amplifier by one of two paths. The first path is the high volume path and has a low value resistor in series with the speaker to reduce the amplifier loading when using multiple channels. The other path is connected to the amplifier through a resistor to provide 20 db of attenuation. This allows two different volume settings for any of the stereo speaker channels. The last two stereo speaker channels

have volume limiting resistors approximately equal to half the value of the first 8 channels. This allows the driving of less efficient acoustic-suspension speakers while maintaining similar volume levels. Proper relay operation requires the power amplifiers to be in a quiescent state when relay switching occurs.

Chapter 7

Remote Terminals

The HSICS supports up to 16 remote terminals. Each terminal provides: data communication with the CPU; room temperature sensing; trouble indication; and a speaker for intercom or background music. Figure 7 shows the block diagram of a Remote Terminal.

The Remote Terminals are all parallel connected, except for the speaker lines. Each speaker has a dedicated wire pair connecting it to the Intercom Control board.

Data communication with the CPU is implemented via an 8-bit byte and an interrupt line. The byte consists of a 4-bit, open-collector, I/O buss and 4 control bits. The control bits, two address and two strobes, generate the following functions: latch the I/O buss data for terminal selection; latch the I/O buss data for the two 4-bit LED displays; latch the I/O buss data for additional control information; clear the terminal selection latch; send data to the CPU; and clear the keyboard logic.

Individual remote terminal selection is implemented by a digital comparator and a one bit latch. The I/O buss data is compared to the terminal selection code and the result presented to the latch input; if a match occurs, the latch is activated upon strobing to enable the terminal. Any remote terminal may be individually selected, or all terminals selected in parallel to receive LED display data or keyboard clear pulses from the CPU. Only terminals individually selected may send data to the CPU. Signals controlling terminal selection, clearing, and control-word latching are always presented to each terminal. Any terminal has the capability of sending two 4-bit words to the CPU. Word one has the keyboard data and word two has the temperature comparator result bit, the key-being-touched bit, and two spare bits.

The terminal provides the following human interface elements: a 16-pad keyboard; an any-key-touched-indicator LED; a trouble indicator LED; 8 individual display LED'S; and a speaker. The keyboard logic latches the data corresponding to the key touched; signals the CPU via the interrupt line; and illuminates the key-touched LED. The touch indicator

will remain on until the key is released and the CPU has read the data and cleared the keyboard logic. Additional data entry is inhibited until the touch indicator turns off.

An additional function of the terminal is temperature sensing. The D/A converter output is connected to all terminals, and each compares it to its own internally-generated temperature signal. The comparator result may be read back to the CPU to determine, via appropriate D/A converter settings, the absolute room temperature or whether the temperature is above or below a preset limit.

Chapter 8

System Power Supplies

Figure 8 is the block diagram of the System Power Supplies. All system power is derived from a 12 volt lead-acid storage battery which is constantly being charged by a line-operated supply. This eliminates transients when AC power is interrupted or restored, but necessitates power conversion to generate the required system voltages.

Because of their excellent efficiency and soft-start capability, switching regulators are used for the high current step-down to 5 and 8 volts. The 5 volt supply powers the local system boards and the 8 volt supply is used for the remote terminals.

A switching regulator was also used to both double and then invert the main supply voltage. The doubled and the inverted voltages are regulated by a +/- 15 volt regulator to supply the D/A converter and low level analog control buffers. Also, the doubled voltage is regulated by a 3-terminal regulator to supply 11 volts to the smoke detectors, and the

inverted voltage is regulated to -6 volts to supply the temperature sensors at each remote terminal.

Chapter 9

System Software

The software for the HSICS has been written in assembly language, with extensively used subroutines stored in EPROM. The main program flow is executed from RAM, but can be stored in EPROM for a completely stand-alone system. The RAM is used for variable storage, and will retain its data during an AC power interruption due to the battery back-up system.

The HSICS also may be connected to an optional SOL-20 processing system. The additional features obtained by this connection are: cassette tape storage for down-loading of all RAM programs and data; extensive debugging capabilities; an editor and mnemonic code assembler for machine-code generation; and real-time message and status printing on the SOL-20 printer.

System operation is determined by commands entered from a remote terminal. Each terminal is assigned a block in RAM for its status word and command storage. Data entered at a terminal is stored in RAM until a

delimiter character is received, causing the status word to be set. The display at the remote terminal indicates the latest character entered and the total character count while that terminal is active for command entering. The monitor program, which is the main control software, constantly loops through all system status words to determine what action is necessary. A terminal status word set causes the monitor to send that terminal's command string to the command decoder. The decoder checks for a valid command, and then calls the appropriate function execution module while passing along the necessary control information. The system operates on one command at a time, determined by the order of entry, but allows multiple terminals active at any one time.

The monitor program receives interrupts from the real time clock every 200 ms and uses this information to keep track of time for display purposes and delayed function execution. The interrupt also signals the monitor to call the alarm-switch-check subroutine if the alarm is active. The alarm sequence will be initiated if any active alarm switch fails its test for three consecutive checks. Multiple consecutive failing

is used to prevent false activation due to noise. Temperature sensing is executed every 30 seconds and the required actions implemented. The highest priority of interrupt is assigned to the real time clock, followed by the SOL-20 interface, and then the remote terminals. All other functions are executed in background mode.

CONCLUSION

The Home Security/Intercom/Control System was built and checked-out using two remote terminals. Construction and installation of the remaining terminals is in progress.

The system functions which have been checked and operated satisfactorily are: intrusion alarm sensing; smoke and fire detector monitoring; temperature sensing and control of heating and air conditioning; master intercom capabilities at each remote terminal; stereo control; and self-checking of system outputs and power supplies.

The system is very flexible because of its microprocessor controller and delayed function execution, and provides much more capability than separate systems could have provided.

The completed system cost of approximately \$2300 is considerably more cost effective than the purchase of separate systems to implement each of the functions.

MICROPROCESSOR CONTROLLED HOME SECURITY/INTERCOM/CONTROL SYSTEM

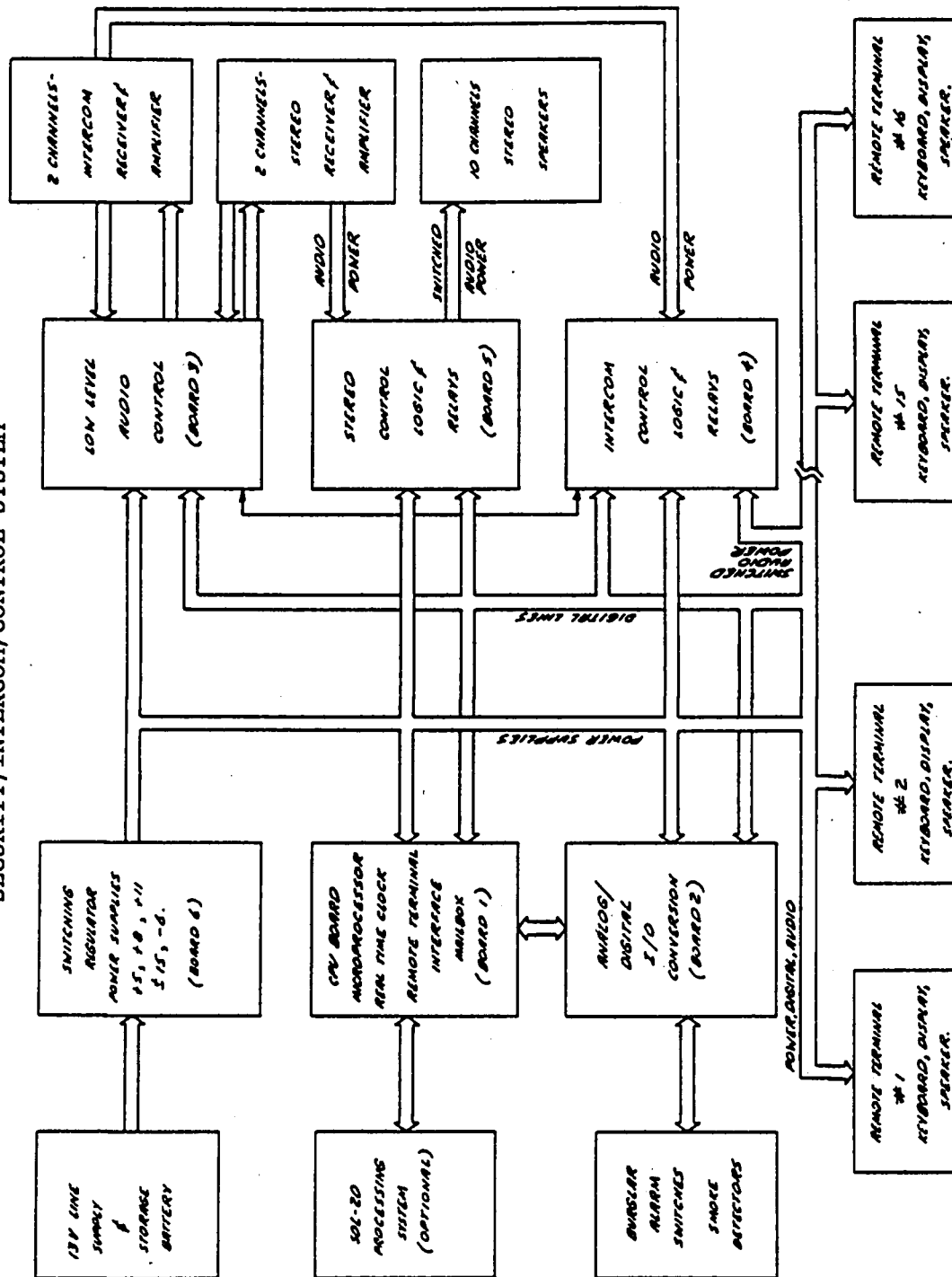


FIGURE 1

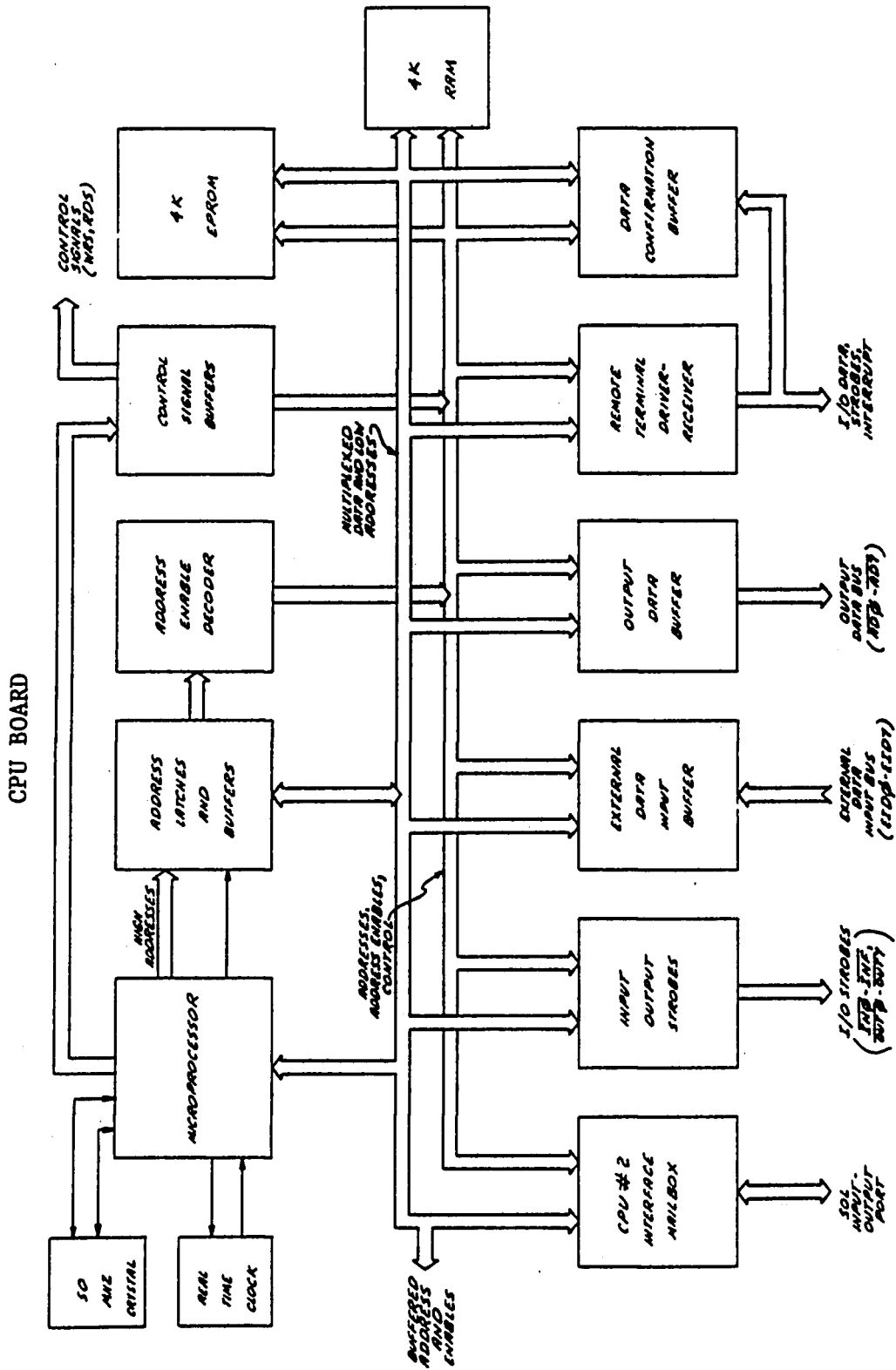


FIGURE 2

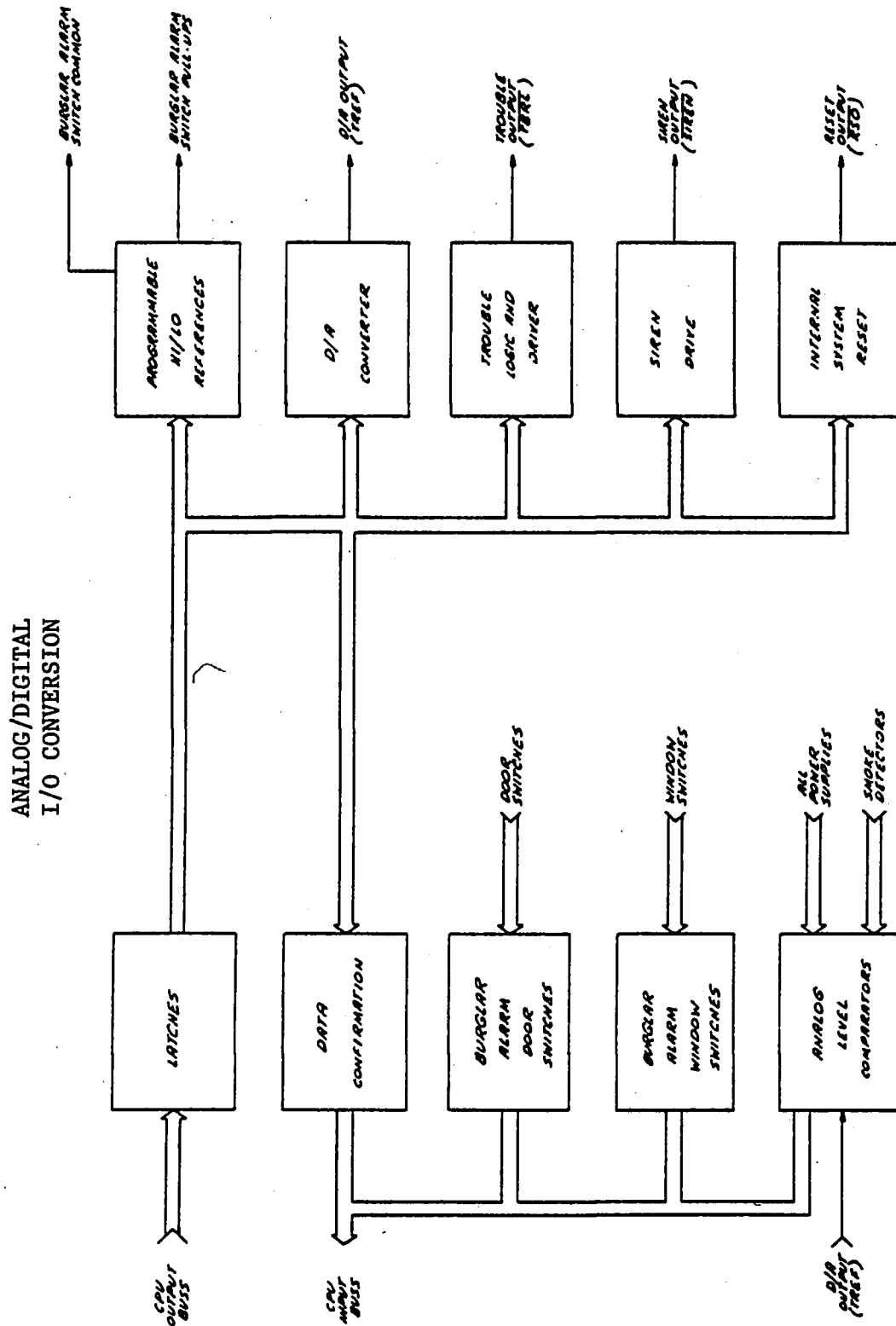


FIGURE 3

LOW LEVEL AUDIO CONTROL

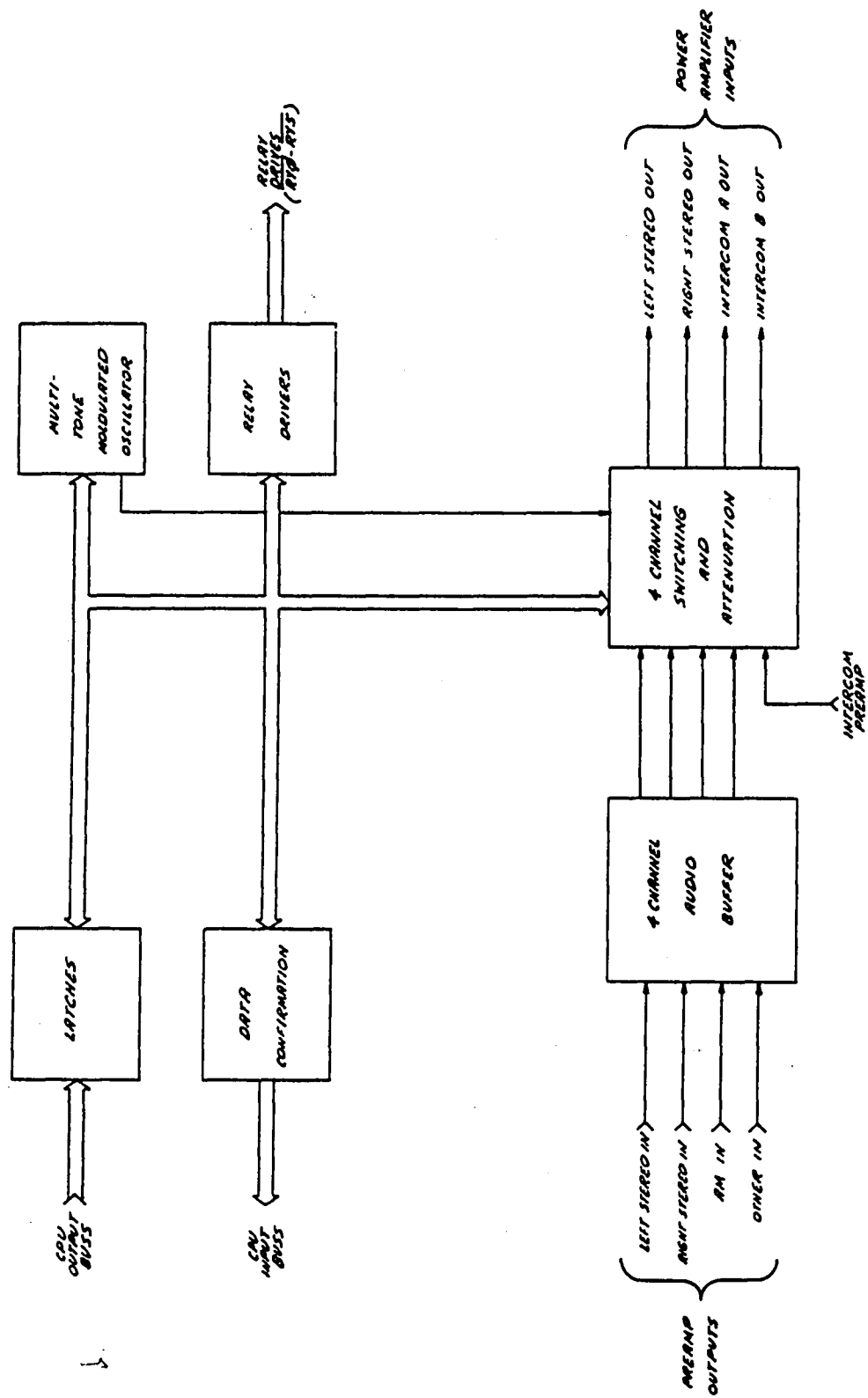


FIGURE 4

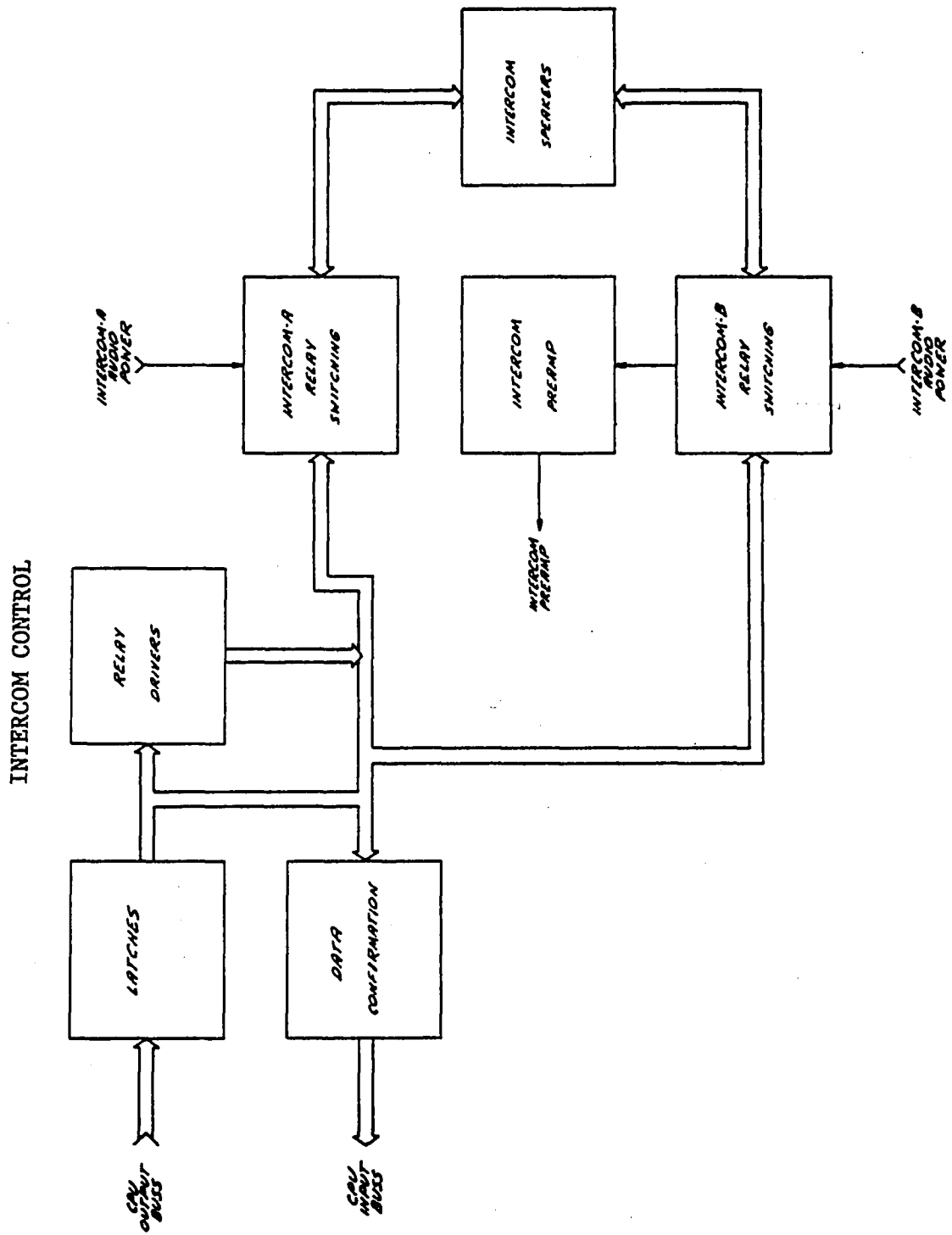


FIGURE 5

STEREO CONTROL

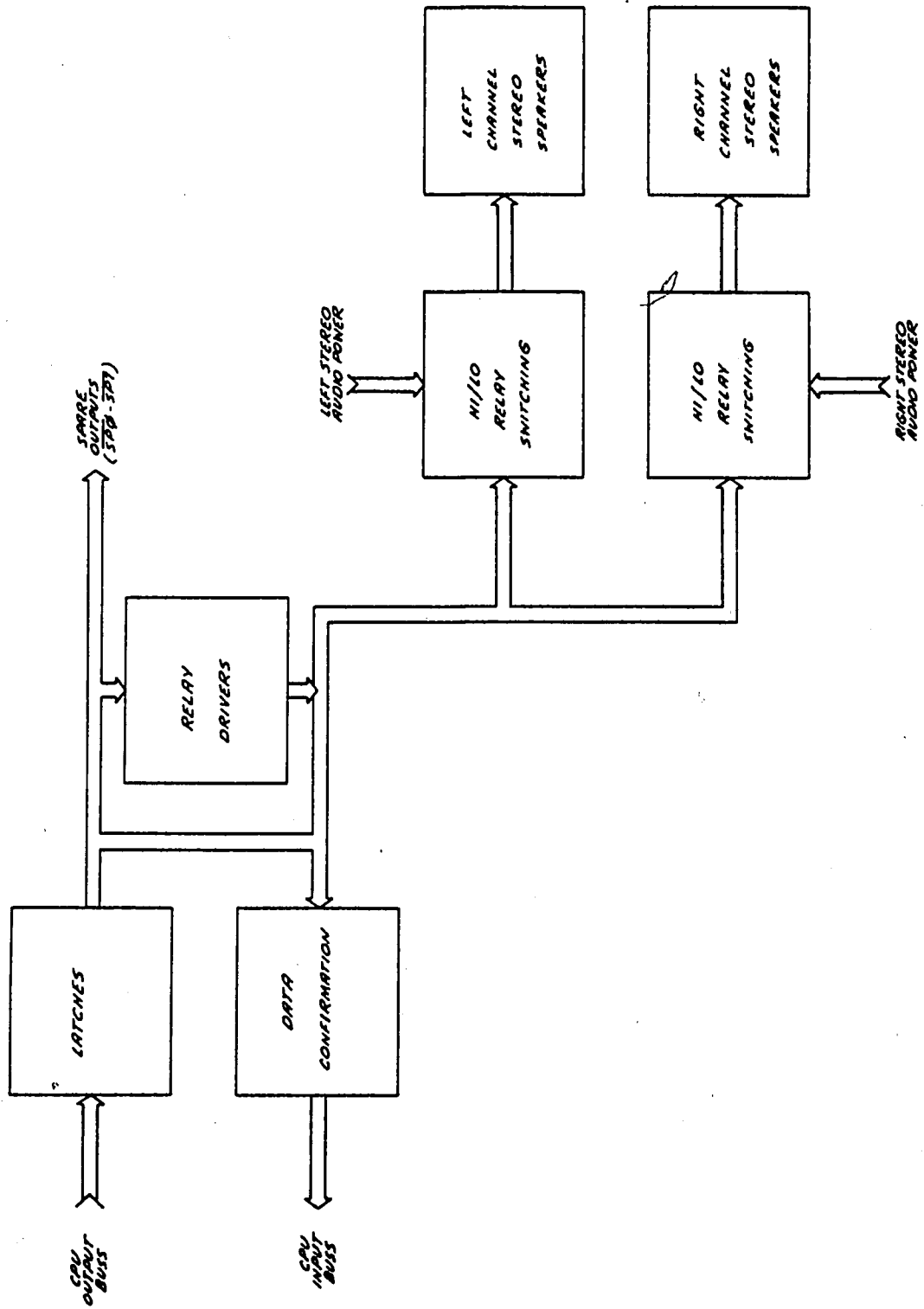


FIGURE 6

REMOTE TERMINAL

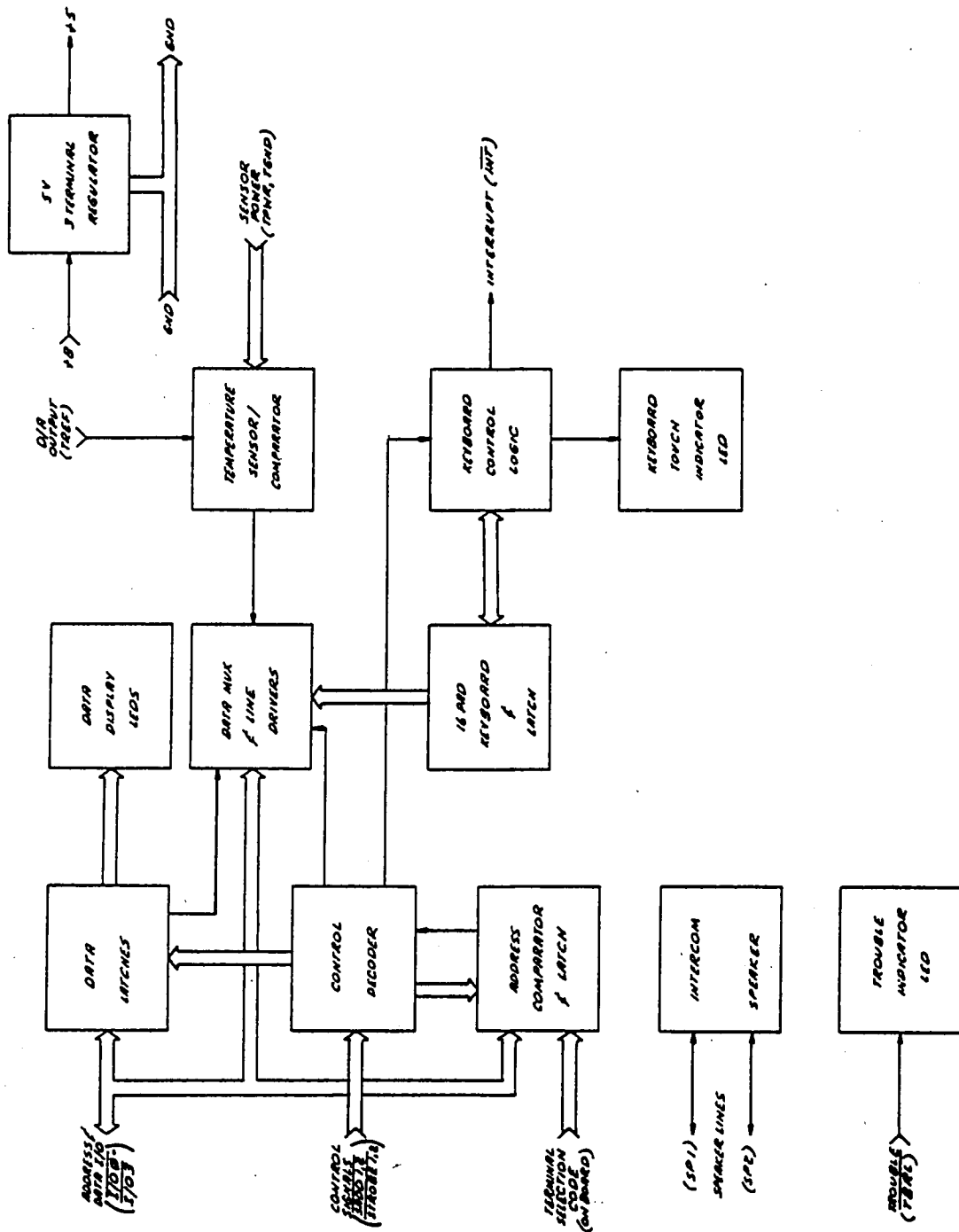


FIGURE 7

SYSTEM POWER SUPPLY

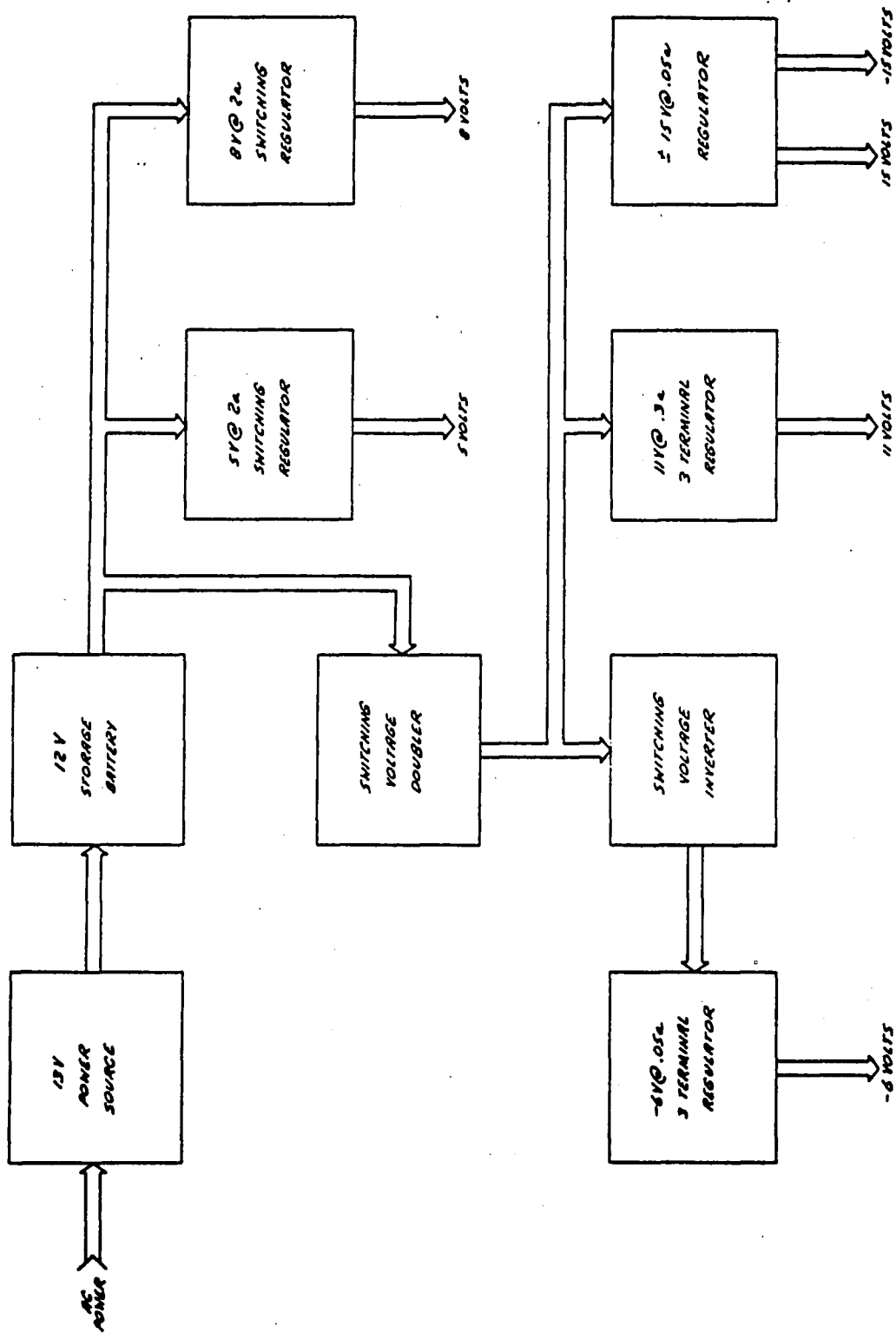


FIGURE 8
-39-

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- [1] INTEL 8008 User's Manual, December 1971.
- [2] INTEL MCS-85 User's Manual, January 1978.

Robert L. Siegel was born in Easton, Pennsylvania, on November 4, 1946. He is the son of Robert D. Siegel and Bessie A. Siegel, both of Easton, Pennsylvania. He married Anna L. Fehnel, also of Easton, on January 14, 1967.

He received an Associate Degree in Electrical Engineering from Pennsylvania State University in 1966. He then joined Western Electric Company, Inc., as an Associate Engineer in the Test Planning and Design Engineering Department. He attended Lafayette College from 1967 until 1975 when he received a Bachelors Degree in Electrical Engineering. He was promoted to Development Engineer in 1974 and took a position as Test Engineer in the Memory Chip Capability Department in 1977.

His hobbies include tennis, model airplanes, and personal computing.