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AN NMOS-LSI VOLTAGE REFERENCE

by

Saul J. Joseph

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

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November 28, 1979
Date

Professor in Charge

Chairman of the Department

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ABSTRACT

An NMOS-LSI Voltage Reference Circuit has been developed which has a low temperature dependence and a low process dependence, and is also insensitive to supply voltage variation. An analysis of the circuit is presented, as well as circuit simulation and experimental results. The temperature dependence of the circuit is approximately 2×10^{-4} V/°C over the operating temperature range. The overall accuracy of the circuit is approximately 1.9 per cent (or $\pm$ 0.95 per cent).

I. INTRODUCTION

Due to the increasing size and complexity of NMOS-LSI logic circuits, a voltage reference is needed to insure that proper voltage levels are available. In addition, development of certain types of circuits have been hindered by the lack of an on-chip voltage reference. In the past, the reference voltage was developed off-chip using bipolar techniques. Utilizing the voltage was often difficult and relatively inaccurate.

The requirement of the voltage reference is that it should have a low temperature dependence and a low process dependence. The circuit should also be invariant to voltage supply variations. A circuit which meets these requirements is presented.

The Composite Voltage Reference Circuit consists of two basic circuits. The Basic Reference Circuit produces two voltage levels. The difference in these two levels is amplified and referenced with respect to the ground voltage in the Voltage Difference Circuit.

A discussion of the various parameters affecting the MOS Device and how their effect is reduced by the circuit design is presented.

Finally, circuit simulation and experimental results are presented and discussed.

II. BASIC REFERENCE CIRCUIT

A number of voltage reference circuits which have a low temperature dependence have been studied.[1-3] The purpose of this study is to develop a voltage reference which not only has a low temperature dependence but also a low process dependence. In section A, the parameters affecting the threshold voltage of an MOS device are analyzed and found to be temperature and process dependent. In section B, a circuit is introduced which reduces the effect of the dependent terms providing a suitable voltage reference.

A. Threshold Voltage

1. Enhancement Device

An expression for the threshold voltage of an enhancement device can be given as

$$V_T = V_{FB} + \psi_{INV} + V_{BULK} \qquad (2.1)$$

where V_{FB} is the flat band voltage, ψ_{INV} is the total band bending for zero substrate bias and V_{BULK} is the bulk voltage.[4] Analysis of each individual term is necessary to determine the parameters affecting the threshold voltage.

The flat band voltage, V_{FB}, for a device with an N^+ polysilicon gate can be expressed as

$$V_{FB} = -\frac{E_g}{2} - \frac{\psi_{INV}}{2} - \frac{qN_{ox}}{Cox} \qquad (2.2)$$

where E_g is the band gap energy, q is the electronic

charge, N_{ox} is the equivalent oxide charge per unit area at the oxide-silicon interface, and Cox is the oxide capacitance per unit area.[5]

The surface potential ψ_{INV} is defined in the following way.[6,7] An n-channel MOS device is shown in Figure 1, with a non-uniform p-type substrate. The relationship between the electron and hole densities, n(x) and p(x), respectively can be expressed as

$$p(x)n(x) = n_i^2 e^{-\frac{qV_{s\text{-}sub}}{KT}} \qquad (2.3)$$

where x = 0 corresponds to the oxide-silicon interface, n_i is the intrinsic density, $\frac{KT}{q}$ is the equivalent thermal voltage, and $V_{s\text{-}sub}$ is the source to substrate voltage. The hole density can be expressed as

$$p(x) = N_B e^{-\frac{q\psi(x)}{KT}} \qquad (2.4)$$

where N_B is the bulk concentration and $\psi(x)$ is the potential referenced to the bulk intrinsic level. Substituting equation 2.4 into equation 2.3 and solving for $\psi(x)$ yields

$$\psi(x) = \frac{KT}{q} \ln \left(\frac{n(x)N_B}{n_i^2}\right) + V_{s\text{-}sub} \quad . \qquad (2.5)$$

For the nonuniform substrate, Doucet and Wiele suggest that the condition for strong surface inversion occurs when the surface minority carrier concentration equals or exceeds the majority carrier concentration at the boundary of the depletion region. Therefore,

$$\psi_{INV} = \frac{KT}{q} \ln \frac{N_A(x_d)N_B}{n_i^2} + V_{s\text{-}sub}. \qquad (2.6)$$

The bulk voltage term, V_{BULK}, can be expressed using Poisson's equation[7]

$$V_{BULK} = \frac{q}{Cox} \int_o^{x_d} N_a(x)\, dx. \qquad (2.7)$$

For simplicity, a uniform step profile with height N_s is assumed where the depth of the step is greater than the depletion width, x_d. Under this condition the bulk term becomes

$$V_{BULK} = \frac{q\, N_s x_d}{Cox} . \qquad (2.8)$$

The depletion width must be found to determine V_{BULK}. Again using Poisson's equation

$$V_{s\text{-}sub} + \psi_{INV} = \frac{q}{\varepsilon_{si}} \int_o^{x_d} \int_o^{x_d} N_a(x')dx'\, dx \qquad (2.9)$$

and solving for x_d yields

$$x_d = \left[\frac{2\,\varepsilon_{si}}{qN_s} (V_{s\text{-}sub} + \psi_{INV})\right]^{\frac{1}{2}} . \qquad (2.10)$$

Substituting equation 2.10 into equation 2.8 yields an expression for the bulk voltage term.

$$V_{BULK} = \left[\frac{2q\,\epsilon_{si}}{Cox^2}\,(V_{s\text{-}sub} + \psi_{INV})\right]^{\frac{1}{2}\,\frac{1}{2}} N_s \qquad (2.11)$$

Finally, substituting equations 2.2 and 2.11 into equation 2.1 yields an expression for the threshold voltage of an NMOS enhancement device.

$$V_T = -\frac{E_g}{2} + \frac{\psi_{INV}}{2} - \frac{qN_{ox}}{Cos} + \left[\frac{2q\,\epsilon_{si}}{Cox^2}\,(V_{s\text{-}sub} + \psi_{INV})\right]^{\frac{1}{2}} N_s^{\frac{1}{2}} . \qquad (2.12)$$

2. Depletion Device

The threshold voltage of a depletion device can be derived in a similar way.[8] The result is stated:

$$V_T = -\frac{E_g}{2} + \frac{\psi_b}{2} - \frac{qN_{ox}}{Cox} + \left[\frac{2q\,\epsilon_{si}}{Cox^2}\,(V_{s\text{-}sub} + \psi_b)\right]^{\frac{1}{2}} N_A^{\prime\,\frac{1}{2}} - \frac{Q_i}{\bar{C}} \qquad (2.13)$$

where $N_A^{\prime}$ is the composite concentration,

$$N_A^{\prime} = \frac{N_s\,N_B}{N_s + N_B} , \qquad (2.14)$$

ψ_b is the channel to substrate built-in voltage, Q_i is the implanted charge and $\bar{C}$ is the equivalent series capacitance of Cox and a channel depth defined capacitance. The built-in voltage for a step junction can be expressed as[9]

$$\psi_b = \frac{KT}{q}\,\ln\left(\frac{N_s N_B}{n_i^2}\right) . \qquad (2.15)$$

The terms that comprise the depletion and enhancement threshold voltages are both temperature and

process dependent. Specifically, ψ_{INV}, and ψ_b are temperature and process dependent while ^{N}ox, Cos, and ^{N}s are process dependent. Trying to achieve a process and temperature invariant threshold voltage would be quite difficult. Therefore, the threshold voltage of a device is not suitable for use as a voltage reference. However, if the effect of the dependent terms can be eliminated or reduced by the circuit design, then a suitable voltage reference can be derived.

B. Circuit Derivation

A circuit which reduces some of the dependent terms is shown in Figure 2. The desired outputs are $^{V}OUT_{L}$ and $^{V}OUT_{R}$. The voltage difference circuit, discussed in section III, is used to reference the difference in the outputs to the ground voltage. Due to the symmetry of the circuit the desired output, $^{V}OUT_{L} - {}^{V}OUT_{R}$, can be calculated in the following way. Transistor T1 and T2 are depletion load devices with equal geometries while transistor T3 and T4 are enhancement driver devices with equal geometries. The current through transistors T1 and T3 can be expressed as

$$I_{DS_{T1}} = \frac{1}{2}\left(\frac{\mu\ Cox\ W}{L}\right)_{T1} \quad V_{T_{T1}}{}^{2} \qquad (2.16)$$

and

$$I_{DS_{T3}} = \frac{1}{2}\left(\frac{\mu\ Cox\ W}{L}\right)_{T3} \left(V_{GS_{T3}} - V_{T_{T3}}\right)^2 \qquad (2.17)$$

where

$$V_{GS_{T3}} = V_{OUT_L} - V_{SS} \quad . \qquad (2.18)$$

Since the two devices are in series,

$$I_{DS_{T1}} = I_{DS_{T3}} \quad . \qquad (2.19)$$

Substitution of equations 2.16, 2.17 and 2.18 into equation 2.19 yields

$$\frac{1}{2}\left(\frac{\mu\ Cox\ W}{L}\right)_{T1} V_{T_{T1}}^2 = \frac{1}{2}\left(\frac{\mu\ Cox\ W}{L}\right)_{T3} \left(V_{OUT_L} - V_{SS} - V_{T_{T3}}\right)^2 . \qquad (2.20)$$

Solving for V_{OUT_L} yields

$$V_{OUT_L} = \frac{\left(\frac{\mu Cox\ W}{L}\right)_{T1}}{\left(\frac{\mu Cox\ W}{L}\right)_{T3}} \left|V_{T_{T1}}\right| + V_{SS} + V_{T_{T3}} \quad . \qquad (2.21)$$

During the layout of the circuit these four devices were placed physically adjacent to minimize mismatches in parameters due to gradients across the wafer. Therefore the mobilities and oxide capacitances are assumed to be equal. This reduces equation 2.21 to

$$V_{OUT_L} = \left(\frac{W}{L}\right)_{T1} \left(\frac{L}{W}\right)_{T3} \left|V_{T_{T1}}\right| + V_{SS} + V_{T_{T3}} \quad . \qquad (2.22)$$

By symmetry the equation for V_{OUT_R} can be written

$$V_{OUT_R} = \left(\frac{W}{L}\right)_{T2} \left(\frac{L}{W}\right)_{T4} |V_{T_{T2}}| + V_{SS} + V_{T_{T4}} \qquad (2.23)$$

The desired output, $V_{OUT_L} - V_{OUT_R}$, is calculated by subtracting equation 2.23 from equation 2.22 and recalling that the load devices and the driver devices have the same geometries. Therefore,

$$V_{OUT_L} - V_{OUT_R} = \left(\frac{W}{L}\right)_{T1} \left(\frac{L}{W}\right)_{T3} [|V_{T_{T1}}| - |V_{T_{T2}}|] + [V_{T_{T3}} - V_{T_{T4}}] \qquad (2.24)$$

Since transistors T1 and T2 are depletion load NMOS devices the absolute value signs can be eliminated.

$$V_{OUT_L} - V_{OUT_R} = \left(\frac{W}{L}\right)_{T1} \left(\frac{L}{W}\right)_{T3} [V_{T_{T2}} - V_{T_{T1}}] + [V_{T_{T3}} - V_{T_{T4}}] \qquad (2.25)$$

To evaluate equation 2.25 each term is considered separately. The first term of equation 2.25 can be evaluated by substituting the expression for the threshold voltage given in equation 2.13. Since transistor T1 and T2 are identical and physically adjacent, the only term comprising the threshold voltage which is different for the two devices is the source to substrate voltage, $V_{s\text{-}sub}$. This results in the cancellation of a number of terms. Therefore,

$$V_{T_{T2}} - V_{T_{T1}} = \left(\frac{2q\,\varepsilon_{si} N_A'}{\bar{C}}\right)^{\frac{1}{2}} [(V_{s\text{-}sub} + \psi_b)_{T2}^{\frac{1}{2}} - (V_{s\text{-}sub} + \psi_b)_{T1}^{\frac{1}{2}}]. \qquad (2.26)$$

The second term of equation 2.25 can be evaluated by substituting the expression for the threshold voltage given in equation 2.12. Since transistors T3 and T4 are identical and physically adjacent, the only term in the threshold voltage which is different for the two devices is the impurity doping, N_s. Again this results in the cancelling of a number of terms. In addition, the source to substrate voltage, $V_{s\text{-}sub}$, is zero. Therefore,

$$V_{T_{T3}} - V_{T_{T4}} = \frac{1}{2}\left(\psi_{INV_{T3}} - \psi_{INV_{T4}}\right) + \frac{(2q\,\varepsilon_{si})^{\frac{1}{2}}}{Cox}\left[(N_s\psi_{INV})^{\frac{1}{2}}_{T3} - (N_s\psi_{INV})^{\frac{1}{2}}_{T4}\right] \tag{2.27}$$

Substitution of equations 2.26 and 2.27 into equation 2.25 yields:

$$V_{OUT_L} - V_{OUT_R} = \left(\frac{W}{L}\right)_{T1}\left(\frac{L}{W}\right)_{T3}\frac{(2q\,\varepsilon_{si}N_A')^{\frac{1}{2}}}{\bar{C}}\left[(V_{s\text{-}sub}+\psi_b)^{\frac{1}{2}}_{T2} - (V_{s\text{-}sub}+\psi_b)^{\frac{1}{2}}_{T1}\right] + \frac{1}{2}\left(\psi_{INV_{T3}} - \psi_{INV_{T4}}\right) + \frac{(2q\,\varepsilon_{si})^{\frac{1}{2}}}{Cox}\left[(N_s\psi_{INV})^{\frac{1}{2}}_{T3} - (N_s\psi_{INV})^{\frac{1}{2}}_{T4}\right] . \tag{2.28}$$

The result, $V_{OUT_L} - V_{OUT_R}$ is dependent on two processing parameters; the doping of the devices and the silicon dioxide layer thickness, both of which are well controlled during processing.

C. Temperature Dependence

The temperature dependence of the output, V_{OUT_L}, V_{OUT_R}, can be found by differentiating equation 2.28 with respect to temperature. This calculation yields a result which is not in closed form. Therefore, to determine the temperature dependence of the circuit a simulation was completed using SPICE, a computer circuit analysis program.(10)

The circuit was simulated at various temperatures. The nodes voltages, V_{OUT_L} and V_{OUT_R}, versus temperature are shown in Figure 3. The curves show the voltages are linearly proportional to temperature and are essentially parallel to each other.

The voltage change per degree centigrade is approximately -2×10^{-3} V/°C. This implies that the difference, $V_{OUT_L} - V_{OUT_R}$, would be substantially less dependent upon temperature than either term separately. In Figure 4 the dependence of the output $V_{OUT_L}-V_{OUT_R}$ on temperature is shown to be substantially less than either of the two node voltages. The voltage change per degree centigrade is approximately -4×10^{-5} V/°C.

III. VOLTAGE DIFFERENCE CIRCUIT

In the Voltage Reference Circuit an operational amplifier is used with externally applied feed-back to provide a voltage difference circuit as shown in Figure 5.[11] The circuit provides a means whereby the difference of the two voltages V_a and V_b is amplified and referenced with respect to the ground voltage. Expressions can be developed relating the reference voltage to the input voltages.

A. Operational Amplifier

One of the most widely used integrated circuit building blocks is the operational amplifier. It is considered to be a voltage controlled voltage source. The circuit has high gain and is principally used with externally applied feedback to perform various functions.

The operational amplifier consists of the following structure as shown in Figure 6: 1) A differential input stage 2) intermediate gain stages 3) an output stage.[12] In this design, the differential input stage and the gain stages are identical. The two basic circuits are shown in Figures 7 and 8.

The differential stage consists of a differential pair of transistors being driven by a common current source. Active devices are used as load resistors, as is typical with MOS circuits. The source followers shift the D.C. level of the inputs to a lower D.C. potential. This

allows the outputs of the current stage to be directly connected to the inputs of the next stage. The output stage consists of two inverters properly biased to achieve an output voltage swing which encompasses the desired reference voltage.

In MOS design, the gain increases as the square root of the quotient of the channel width to length ratios of the driver and load transistors.[13] This allows only a moderate amount of gain per stage. In addition, the gain achieved in the differential circuit is reduced since the source followers have a gain which is less than one.[13] Due to the symmetry of the differential circuit the gain can be analyzed in the following way. Referring to Figure 7, transistors T5 and T7 are operating in the saturation region. Therefore, using the equations that describe the operation of an MOS device, the current through each device can be expressed as[14]

$$I_{DS_{T5}} = \frac{1}{2} \left(\frac{\mu \, Cox \, w}{L}\right)_{T5} \left(V_{GS_{T5}} - V_{T_{T5}}\right)^2 \qquad (3.1)$$

and

$$I_{DS_{T7}} = \frac{1}{2} \left(\frac{\mu \, Cox \, w}{L}\right)_{T7} \left(V_{GS_{T7}} - V_{T_{T7}}\right)^2 \qquad (3.2)$$

where

$$V_{GS_{T5}} = \left(V_{DD} - V'_{OUT_L}\right) \qquad (3.3)$$

and

$$V_{GS_{T7}} = (V'_{IN_L} - V_B). \tag{3.4}$$

Since the two devices are in series, the currents $I_{DS_{T5}}$ and $I_{DS_{T7}}$ are equal. Therefore,

$$(\frac{\mu\ Cox\ w}{L})_{T5}(V_{GS_{T5}}-V_{T_{T5}})^2 = (\frac{\mu\ Cox\ w}{L})_{T7}\ (V_{GS_{T7}}-V_{T_{T7}})^2 \quad . \tag{3.5}$$

Substitution of equation 3.3 and 3.4 into 3.5 yields

$$(\frac{\mu\ Cox\ w}{L})\quad (V_{DD}-V'_{OUT_L}-V_{T_{T5}})^2=(\frac{\mu\ Cox\ w}{L})_{T7}\ (V'_{IN_L}-V_B-V_{T_{T7}})^2 . \tag{3.6}$$

During the layout of the circuit the devices were placed physically adjacent to minimize mismatches in parameters due to gradients across the wafer. Therefore the mobilities and oxide capacitances are assumed to be equal. Solving equation 3.6 for V'_{OUT_L} yields

$$V'_{OUT_L} = -\left[\frac{(\frac{w}{L})_{T7}}{(\frac{w}{L})_{T5}}\right]^{\frac{1}{2}}(V'_{IN_L}-V_B-V_{T_{T7}})+(V_{DD}-V_{T_{T5}}) \quad . \tag{3.7}$$

Similarly, the equation for V'_{OUT_R} can be written as

$$V'_{OUT_R} = -\left[\frac{(\frac{W}{L})_{T8}}{(\frac{W}{L})_{T6}}\right]^{\frac{1}{2}} (V'_{IN_R} - V_B - V_{T_{T8}}) + (V_{DD} - V_{T_{T6}}) \quad . \tag{3.8}$$

By symmetry the geometries of the respective load and driver devices are equal. Subtracting equation 3.7 from equation 3.8 yields

$$V'_{OUT_R} - V'_{OUT_L} = \left[\frac{(\frac{W}{L})_{T7}}{(\frac{W}{L})_{T5}}\right]^{\frac{1}{2}} (V'_{IN_L} - V'_{IN_R}) \quad . \tag{3.9}$$

the gain of the circuit is defined as the ratio of the difference in the outputs to the difference in the inputs.

$$A_{DIFF} = \frac{(V'_{OUT_R} - V'_{OUT_L})}{(V'_{IN_R} - V'_{IN_L})} \tag{3.10}$$

Substitution of equation 3.9 into 3.10 results in an expression for the gain of the circuit.

$$A_{DIFF} = -\left[\frac{(\frac{W}{L})_{T7}}{(\frac{W}{L})_{T5}}\right]^{\frac{1}{2}} \tag{3.11}$$

The gain of the source follower circuits are now analyzed. Referring to Figure 7, transistor T1 is operating in the saturation region while transistor T3 is operating in triode region. Therefore the currents through each

device can be expressed as

$$I_{DS_{T1}} = \frac{1}{2} \left(\frac{\mu \, Cox \, w}{L}\right)_{T1} (V_{GS_{T1}} - V_{T_{T1}})^2 \tag{3.12}$$

and

$$I_{DS_{T3}} = \left(\frac{\mu \, Cox \, w}{L}\right)_{T3} [(V_{GS_{T3}} - V_{T_{T3}}) V_{DS_{T3}} - \frac{1}{2} V_{DS_{T3}}^2] \tag{3.13}$$

where

$$V_{GS_{T1}} = V_{IN_L} - V'_{IN_L}, \tag{3.14}$$

$$V_{GS_{T3}} = V_{DD} - V_{SS} \tag{3.15}$$

and

$$V_{DS_{T3}} = V'_{IN_L} - V_{SS} \quad . \tag{3.16}$$

Since the two devices are in series the currents $I_{DS_{T1}}$ and $I_{DS_{T3}}$ are equal. Therefore,

$$\frac{1}{2}\left(\frac{\mu \, Cox \, w}{L}\right)_{T1} (V_{GS_{T1}} - V_{T_{T1}})^2 = \left(\frac{\mu \, Cox \, w}{L}\right)_{T3} [(V_{GS_{T3}} - V_{T_{T3}}) V_{DS_{T3}} - \frac{1}{2} V_{DS_{T3}}^2] . \tag{3.17}$$

Again, due to adjacent placement the respective oxide capacitances and the mobilities are assumed equal. Sub-substitution of equations 3.14, 3.15, and 3.16 into equation 3.17 results in

$$\frac{1}{2}\left(\frac{W}{L}\right)_{T1}\left(V_{IN_L} - V'_{IN_L} - V_{T_{T1}}\right)^2 =$$

$$\left(\frac{W}{L}\right)_{T3}\left[\left(V_{DD}-V_{SS}-V_{T_{T3}}\right)\left(V'_{IN_L}-V_{SS}\right)-\frac{1}{2}\left(V'_{IN_L}-V_{SS}\right)^2\right]. \tag{3.18}$$

Differentiation of equation 3.18 with respect to V_{IN_L} and solving for the gain, $\frac{dV'_{IN_L}}{dV_{IN_L}}$, yields

$$\frac{dV'_{IN_L}}{dV_{IN_L}} = \frac{1}{1 + \frac{\left(\frac{W}{L}\right)_{T3}}{\left(\frac{W}{L}\right)_{T1}}\left[\frac{V_{DD} - V'_{IN_L} - V_{T_{T3}}}{V_{IN_L} - V'_{IN_L} - V_{T_{T1}}}\right]}. \tag{3.19}$$

The output stage is made up of two inverters and was designed to exhibit a low output impedance with respect to the feedback devices. This was achieved by using devices with large geometries. The circuit was biased to achieve a voltage swing encompassing the reference voltage. Also, inherent in the inverter structure is a gain factor which is analyzed in the following way.

Referring to Figure 8, transistor T10 is operating in the triode region while transistor T12 is operating in the saturation region. Therefore the currents through these devices can be written as

$$I_{DS_{T10}} = \left(\frac{\mu\ Cox\ w}{L}\right)_{T10} \left[\left(V_{GS_{T10}} - V_{T_{T10}}\right)V_{DS_{T10}} - \frac{1}{2} V_{DS_{T10}}^2\right] \tag{3.20}$$

and

$$I_{DS_{T12}} = \frac{1}{2} \left(\frac{\mu\ Cox\ w}{L}\right)_{T12} \left(V_{GS_{T12}} - V_{T_{T12}}\right)^2 \tag{3.21}$$

where

$$V_{GS_{T10}} = V_{DD} - V_{OUT_L} = V_{DS_{T10}} \tag{3.22}$$

and

$$V_{GS_{T12}} = V''_{IN_L} - V_{SS} \quad . \tag{3.23}$$

The output impedance of the circuit is small compared to the feedback resistance. Therefore the current loss through the feedback devices can be considered negligible. Since the two devices are in series the currents $I_{DS_{T10}}$ and $I_{DS_{T12}}$ are equal. Therefore,

$$\left(\frac{\mu\ Cox\ w}{L}\right)_{T10} \left[\left(V_{GS_{T10}} - V_{T_{T10}}\right)V_{DS_{T10}} - \frac{1}{2} V_{DS_{T10}}^2\right] =$$

$$\frac{1}{2}\left(\frac{\mu\ Cox\ w}{L}\right)_{T12} \left(V_{GS_{T12}} - V_{T_{T12}}\right)^2 \quad . \tag{3.24}$$

Since the devices are closely spaced, substitution of equations 3.22 and 3.23 into equation 3.24 yields

$$\left(\frac{W}{L}\right)_{T10}\left[\left(V_{DD}-V_{OUT_L}-V_{T_{T10}}\right)\left(V_{DD}-V_{OUT_L}\right)-\frac{1}{2}\left(V_{DD}-V_{OUT_L}\right)^2\right] =$$

$$\frac{1}{2}\left(\frac{W}{L}\right)_{T12}\left(V''_{IN_L}-V_{SS}-V_{T_{T12}}\right)^2 \quad . \tag{3.25}$$

Differentiation with respect to V''_{IN_L} and solving for the gain, $\frac{d\,V_{OUT_L}}{d\,V''_{IN_L}}$, yields

$$\frac{d\,V_{OUT_L}}{d\,V''_{IN_L}} = -\frac{\left(\frac{W}{L}\right)_{T12}\left(V''_{IN_L}-V_{SS}-V_{T_{T12}}\right)}{\left(\frac{W}{L}\right)_{T10}\left(V_{DD}-V_{OUT_L}-V_{T_{T10}}\right)} \quad . \tag{3.26}$$

The entire operational amplifier circuit is shown in block form in Figure 6. There are two intermediate gain stages. The gain of the circuit can be found by multiplying the gain of each successive stage. Therefore,

$$A_{TOTAL} = \left(A_{\text{gain stage}}\right)^3 \left(A_{\text{output stage}}\right). \tag{3.27}$$

where $A_{\text{gain stage}}$ is calculated by multiplying the gain of the differential circuit (equation 3.11) by the gain of the source followers (equation 3.19). Substituting the appropriate values found in Table 1 into equations 3.11 and 3.19 results in:

$$A_{DIFF} = 9 \tag{3.28}$$

and

$$\frac{dV'_{IN_L}}{dV_{IN_L}} = 0.9 \quad . \tag{3.29}$$

Therefore,

$$A_{\text{gain stage}} = 8.1 \tag{3.30}$$

The gain of the output stage is calculated by substituting the appropriate values into equation 3.26. Therefore

$$A_{\text{output stage}} = 0.4 \tag{3.31}$$

The gain of the operational amplifier is calculated by substituting equations 3.30 and 3.31 into equation 3.27 yielding

$$A_{TOTAL} = 200 \quad . \tag{3.32}$$

B. Feedback Network

The externally applied feedback network consists of four resistors and is shown in Figure 9. The following analysis shows the relationship between the reference voltage V_{REF} and the input voltages V_a and V_b which are supplied by the Basic Reference Circuit.

Consider an ideal operational amplifier where: 1) the input resistance is infinite; 2) the output resistance is zero; 3) the input offset voltage is zero; 4) the gain is large.[15] Referring to Figure 5, the currents I_1 and I_2 can be expressed as:

$$I_1 = \frac{V_R - e_a}{R_1} \tag{3.33}$$

and

$$I_2 = \frac{e_a - V_a}{R_2} \quad . \tag{3.34}$$

Since the input resistance can be considered infinite the currents are equal. Therefore,

$$\frac{V_R - e_a}{R_1} = \frac{e_a - V_a}{R_2} \quad . \tag{3.35}$$

Solving for V_R:

$$V_R = e_a \left(1 + \frac{R_1}{R_2} \right) - \left(\frac{R_1}{R_2}\right) V_a \quad . \tag{3.36}$$

Resistors R_3 and R_4 form a voltage divider resulting in

$$e_b = \left(\frac{R_4}{R_3+R_4}\right) V_b \quad . \tag{3.37}$$

Assuming a zero input offset voltage results in

$$e_a = e_b \quad . \tag{3.38}$$

Therefore substitution of equations 3.37 and 3.38 into equation 3.36 results in:

$$V_R = \left(\frac{R_4}{R_3+R_4}\right) \left(\frac{R_1+R_2}{R_2}\right) V_b - \left(\frac{R_1}{R_2}\right) V_a \quad . \tag{3.39}$$

However, the actual input offset voltage is not zero.[15] This results in an additional term in the equation for V_R. Assuming the input offset voltage is Δ then

$$e_a = e_b + \Delta. \tag{3.40}$$

Substitution of equations 3.40 and 3.37 into equation 3.36 results in:

$$V_R = [V_b \left(\frac{R_4}{R_3+R_4}\right) + \Delta] \left(1+\frac{R_1}{R_2}\right) - \left(\frac{R_1}{R_2}\right) V_a . \tag{3.41}$$

Rearrangement of the terms yields:

$$V_R = V_b \left(\frac{R_4}{R_3+R_4}\right) \left(\frac{R_1+R_2}{R_2}\right) - \left(\frac{R_1}{R_2}\right) V_a + \Delta \left(\frac{R_1+R_2}{R_2}\right) . \tag{3.42}$$

Equation 3.42 can be expressed as:

$$V_R = V_{R_o} + \Delta \left(\frac{R_1+R_2}{R_2}\right) \tag{3.43}$$

where V_{R_o} is the reference voltage for zero input offset voltage.

IV. COMPOSITE VOLTAGE REFERENCE CIRCUIT

A. Implementation

The Composite Reference Circuit consists of the Basic Reference Circuit and the Voltage Difference Circuit. As shown in Figure 9, the outputs of the Basic Reference Circuit, V_{OUT_L} and V_{OUT_R}, are directly connected to the inputs V_b and V_a, of the Voltage Difference Circuit. The layout of the circuit was done in six ways to incorporate a number of features.

The feedback network of the Voltage Difference Circuit causes a loss in current in the Basic Reference Circuit thereby reducing its accuracy. Increasing the value of the resistors in the feedback network decreases this current loss. Circuits 1 and 2 were implemented using ion-implanted polysilicon resistors. Since the ion-implanted polysilicon has a sheet resistivity of 40-60 ohms per square, a large amount of area would be required for resistors in the kilo-ohm range. Therefore area considerations limit the accuracy. Circuit 3 through 6 were implemented using intrinsic polysilicon resistors. The intrinsic polysilicon has a sheet resistivity of approximately 10^{10} ohms per square, therefore eliminating the area consideration. In addition, the output resistance of the Basic Reference Circuit was reduced in Circuits 1, 2, 5 and 6 to reduce the current loss. This was

accomplished by increasing the size of the output devices.

The value of the threshold voltages of the enhancement devices in the Basic Reference Circuit was varied to determine the accuracy of the processing and the predictability of the value of the reference voltage. The difference in the threshold voltage is created by an additional Boron implant for one of the devices. The amount of the additional dose needed to achieve the high enhancement threshold voltage was extrapolated from previously measured data. The accuracy of the voltage reference is dependent on the threshold voltage matching of the two enhancement devices. Two different values of high enhancement threshold voltage were evaluated. This necessitated using two different values for overall gain of the operational amplifier, in the Voltage Difference Circuit, to achieve the same absolute value of the reference voltage for all of the circuits.

Circuits 1, 3, and 5 have a large implant dose which yields a difference in the output voltages of approximately 3 volts. Referring to Table II, the resistors in the Voltage Difference Circuit are chosen so that the closed loop gain is reduced to one. This is accomplished by minimizing the mismatches in their size. This is shown by substitution into equation 3.41 yielding

$$V_R = V_b - V_a + 2\Delta \quad . \qquad (4.1)$$

Circuits 2, 4, and 6 have a lower implant dose which yields a difference in the output voltage of approximately 1.5 volts. To achieve the same absolute value of the reference voltage for all six circuits the resistors are chosen so that the closed loop gain is reduced to two. Again this is shown by substitution into equation 3.41 yielding

$$V_R = 2(V_b - V_a) + 3\Delta \qquad (4.2)$$

B. Simulation

Circuits 1, 2, and 3 were simulated using SPICE. The following parameters were incorporated into these simulations.

1.	Substrate Doping:	$2.0 \times 10^{15} \pm 5 \times 10^{14}$	cm^{-3}
2.	Temperature Range:	0 to 100	°C
3.	Voltage Supplies	$+5.0 \pm 5\%$	Volts
		$-5.0 \pm 5\%$	Volts
4.	Threshold Voltage Variation (See Table I)	$\pm$ 0.3	Volts

The effect on the reference voltage of each circuit due to these variations is shown in Figures 10 through 12. The results for circuits 1 and 2 are approximately the same while the results for circuit 3 are different. This is due to the circuit implementation. Referring to Table 2, circuits 1 and 2 were implemented

using ion-implanted polysilicon resistors which have a value in the kilo-ohm range. Circuit 3 was implemented using intrinsic polysilicon resistors which have a value of approximately 10^{10} ohms. As discussed in section II, the larger value resistors increase the accuracy of the Basic Reference Circuit and therefore the accuracy of the reference voltage. The temperature dependence of the reference voltage is related to the temperature dependence of the Basic Reference Circuit discussed in section II and the input offset voltage of the operational amplifier. The reference voltage is unaffected by the temperature dependence of the resistors in the feedback network as it depends on the ratio of the resistors. The temperature dependence of the reference voltage is approximately 2×10^{-4} V/°C for circuits 1 and 2 and 2×10^{-5}V/°C for circuit 3. The variation in the reference voltage with changes in substrate doping is caused by the stronger temperature dependence of the threshold voltage of heavier doped substrates than lighter doped substrates.[16] The variation of the reference voltage when the voltage supplies are varied is due to the change in the operating point of the input devices of the operational amplifier. This change directly affects the input offset voltage of the operational amplifier. Referring to equation 4.1, as the input offset voltage varies, the reference voltage will vary.

The total variation of the reference voltage is shown as a function of all three parameters and is approximately 1.9 per cent (or $\pm$ 0.95%) for circuits 1 and 2 and 0.7 per cent (or $\pm$ 0.35%) for circuit 3.

C. Layout

The circuit layout was done using an interactive layout design aid. The major consideration was the adjacent placement of appropriate devices to minimize mismatches of parameters due to gradients across the wafers. Two of the six circuits, circuit 1 and 6 are shown in Figures 13 and 14, respectively. These two circuits were chosen as examples as they include all the features which were previously discussed.

Circuit 6 shows the minimum geometry Basic Reference Circuit. The minimum gate length dimension was 10μm. This relatively large size minimizes the effects of mismatches in the line widths. Each stage of the operational amplifier was laid out individually so that the driver and load devices could be appropriately matched and placed adjacent to each other. The outputs of each stage are connected directly to the inputs of the following stage. The feedback network consists of intrinsic polysilicon resistors. Again, the large dimensions were used to minimize the effects of mismatches in the line widths.

Circuit 1 shows an enlarged Basic Reference Circuit and operational amplifier output stage. The increase in size reduces the output resistance of each circuit. This was done so that ion-implanted polysilicon resistors could be used in the feedback network.

There are eight pads connected to each circuit, four of which are essential to the circuit operation. The remaining four are connected for measurement purposes. The paths of diffusion in series with the pads are used for static protection of the gates of the input devices during testing and handling.

V. MEASUREMENTS

Circuits 3 through 6, which were implemented using the high resistance polysilicon, did not operate properly due to insufficient matching between the individual resistors.

Circuits 1 and 2 were tested and the results are shown in Figures 15 and 16, respectively. The temperature dependence of the reference voltage is approximately 3.5×10^{-3} V/°C for circuit 1 and 4.1×10^{-3} V/°C for circuit 2. The increased dependence of the reference voltage on temperature and supply voltage is due to a shift in the operating points of the devices away from the design value. The investigation of these results indicates that the desired parameters were not achieved in the fabrication of the circuit.

To determine the actual parameters of the fabricated circuits, individual transistors were isolated and characterized. The fabricated threshold voltages are shown in Table III. The circuits were resimulated using the fabricated parameters to determine whether the performance of the fabricated circuits could accurately be predicted. The results are shown in Figures 17 and 18.

Comparison of Figures 16 and 18 reveals that the experimental results and the simulation results are not in close agreement. Specifically, the measured variation in

the internal voltage difference of the Basic Reference Circuit with respect to substrate doping is larger than predicted. The reference bias currents are reduced by a factor of two caused by the fabricated depletion threshold voltage being one volt less than the design value. The difference is further increased by the Voltage Difference Circuit using a gain of two for this circuit compared to a gain of one for circuit 1.

Comparison of Figures 15 and 17 reveals a close correlation between the experimental results and the circuit simulation results of circuit 1. These results show that the actual measured circuit performance is closely predicted by the circuit simulation when the fabricated device parameter values are used. This demonstrates that the design performance should be achieved by this circuit with process parameters which fall within the original design values.

VI. CONCLUSION

The purpose of this study was to develop a voltage reference which has a low temperature dependence and a low process dependence. The differential threshold voltage of the MOS transistor appeared to be a suitable reference voltage.

The first step was to research the MOS fabrication process and to determine the parameters affecting the MOS transistors. The terms which comprise the threshold voltage are both temperature and process dependent yielding it unsuitable as a reference voltage. Further research was completed to reduce the effect of the temperature and process dependent terms by applying suitable circuit design techniques. The temperature dependence of the voltage difference in the two output nodes of the Basic Reference Circuit is substantially less than each individual node. The Voltage Difference Circuit is used to reference the difference of the two output nodes of the Basic Reference Circuit with respect to the ground voltage.

To reduce the process dependence, the circuit layout was very carefully chosen. The major consideration was the adjacent placement of appropriate devices to minimize mismatches of parameters due to gradients across the wafers. The fabrication of the circuit was completed on

the Allentown-Western Electric Company process line.

The results of testing the fabricated circuits showed a larger variation in the reference voltage than expected. The variation is due to a shift in the operating points of the devices. This is a result of the fabricated parameter values being different from the desired parameter values. The circuit was resimulated using the fabricated parameters and close agreement was found between the experimental and simulated results. From this, it is concluded that had the desired parameters been achieved in fabrication the circuits would have worked within the initially simulated accuracy.

The voltage reference as originally designed has a temperature dependence of approximately 2×10^{-4} V/°C over the operating temperature range. The total variation of the reference voltage due to changes in the voltage supplies, substrate doping, threshold voltage, and temperature is approximately 1.9 per cent (or $\pm$ 0.95 per cent).

The need for a circuit of this type is quite apparent. The development of certain types of MOS circuits have been greatly hindered by the lack of an accurate, temperature stable voltage reference. Circuits that perform analog to digital or digital or analog conversions require a reference voltage. In the past this voltage was developed off-chip using bipolar techniques.

Utilizing the voltage was often difficult and relatively inaccurate. The on-chip Composite Voltage Reference presented here could easily be used for this purpose.

TABLE I

DEVICE SIZE AND THRESHOLD VOLTAGE

Device	Width/Length $\mu m/\mu m$	Threshold Voltage (Volts)
Basic Reference Circuit		
T1	127/10	-3.5 $\pm$0.3
T2	127/10	-3.5 $\pm$0.3
T3	10/127	+1.0 $\pm$0.3
T4	10/127	+4.0 or +2.5 $\pm$0.3
Voltage Difference Circuit		
T1	63/10	+1.0 $\pm$0.3
T2	63/10	+1.0 $\pm$0.3
T3	10/63	+1.0 $\pm$0.3
T4	10/63	+1.0 $\pm$0.3
T5	10/90	+1.0 $\pm$0.3
T6	10/90	+1.0 $\pm$0.3
T7	90/10	+1.0 $\pm$0.3
T8	90/10	+1.0 $\pm$0.3
T9	10/90	+1.0 $\pm$0.3
T10	148/10	-3.5 $\pm$0.3
T11	74/10	-3.5 $\pm$0.3
T12	148/10	+1.0 $\pm$0.3
T13	74/10	+1.0 $\pm$0.3

TABLE II

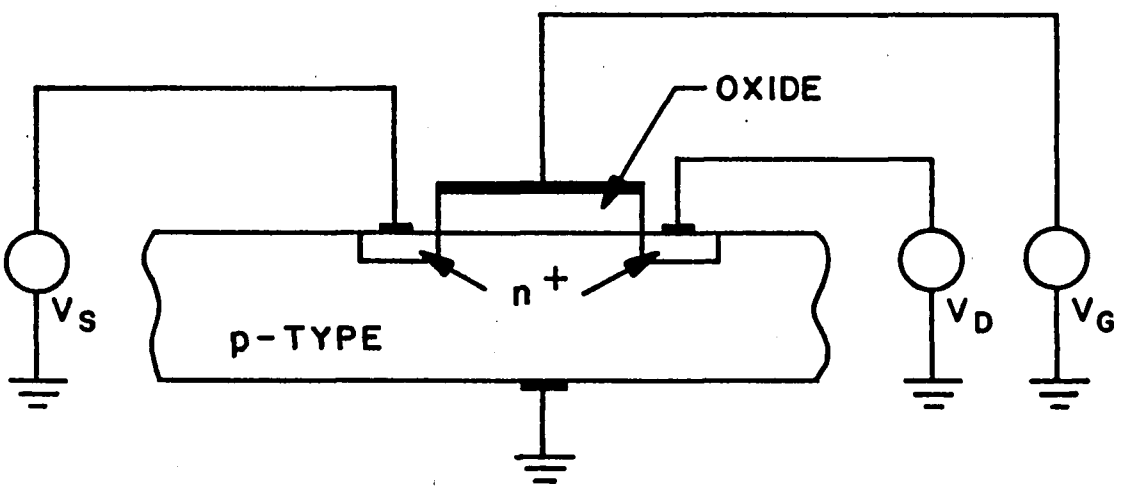
CIRCUIT IMPLEMENTATION

	CIRCUIT					
	1	2	3	4	5	6
I. Basic Reference Circuit						
a. Threshold Values						
T1	+1.0	+1.0	+1.0	+1.0	+1.0	+1.0
T2	+4.0	+2.5	+4.0	+2.5	+4.0	+2.5
b. Output Resistance	very low	very low	very low	very low	low	low
II. Voltage Difference Circuit						
a. Resistor Type	ion-implanted	ion-implanted	intrinsic	intrinsic	intrinsic	intrinsic
b. Resistor Relationship	R1=R2=R3=R4	R1=2R2=2R3=R4	R1=R2=R3=R4	R1=2R2=2R3=R4	R1=R2=R3=R4	R1=2R2=2R3=R4
c. Gain of Feedback Network	1	2	1	2	1	2

TABLE III

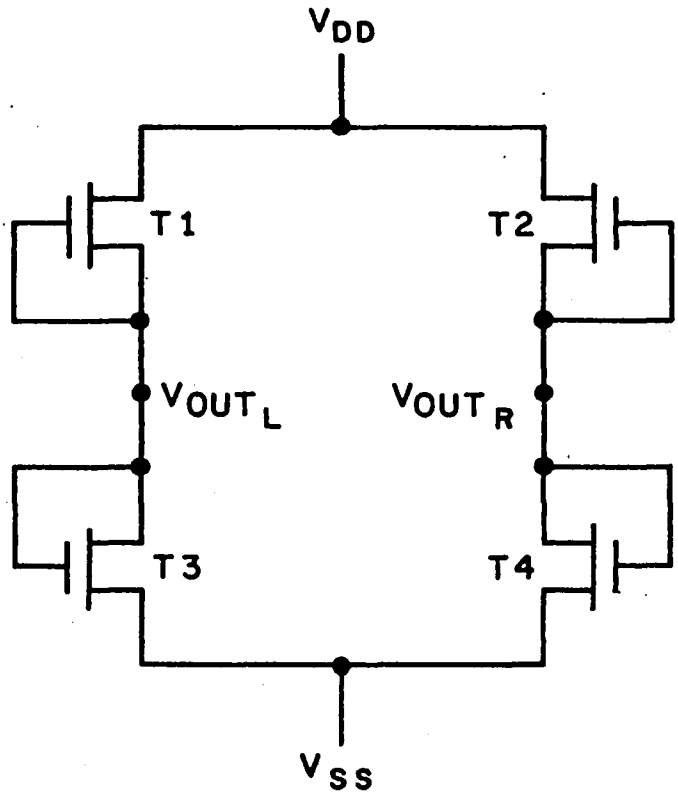
THRESHOLD VOLTAGES

Device	Design Value (Volts)	Fabricated Value (Volts)
Depletion	-3.5	-2.5
Enhancement	+1.0	+1.0
High Enhancement		
Circuit 1	+4.0	+5.25
Circuit 2	+2.5	+3.0



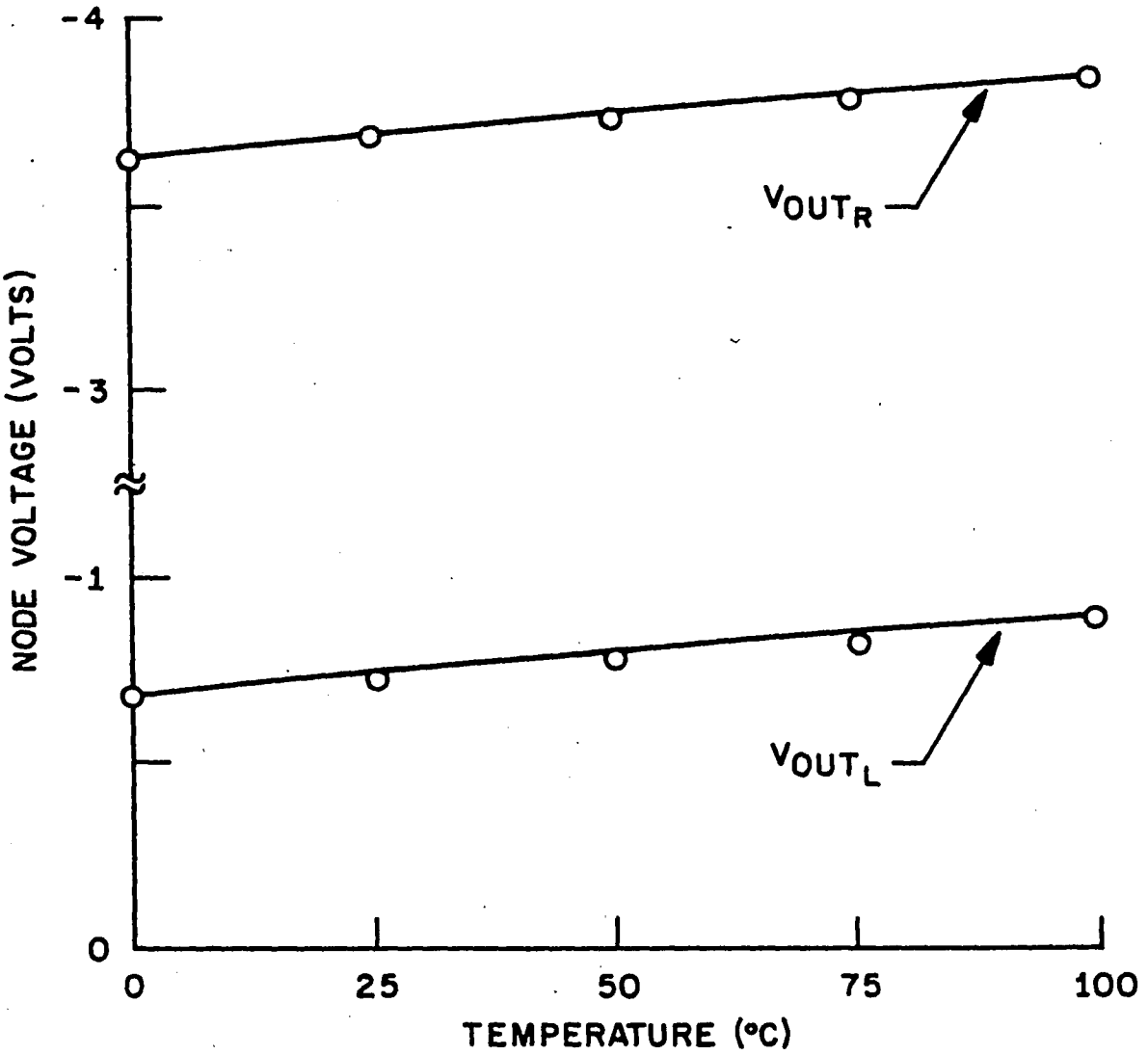
NMOS DEVICE STRUCTURE

FIGURE 1



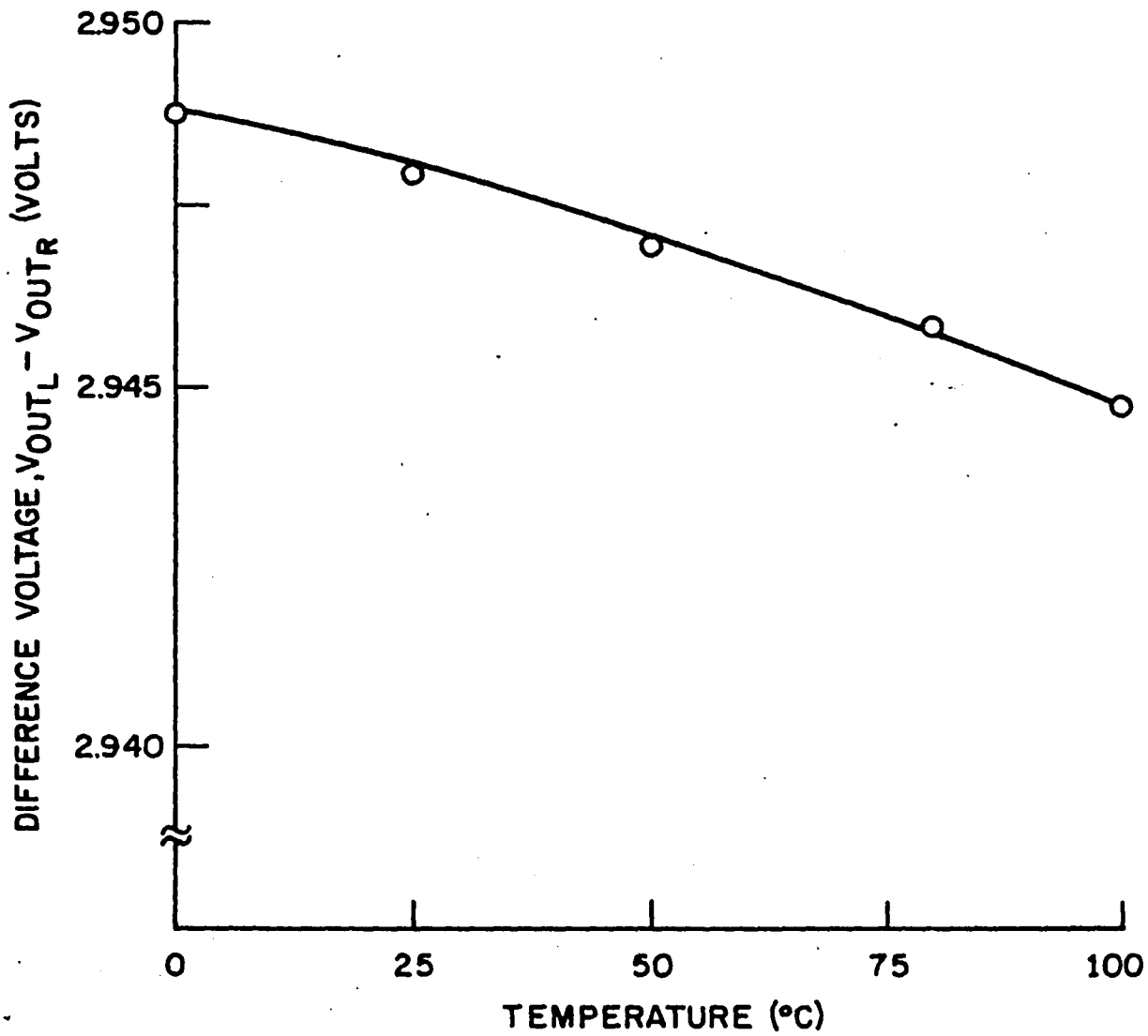
BASIC REFERENCE CIRCUIT

FIGURE 2



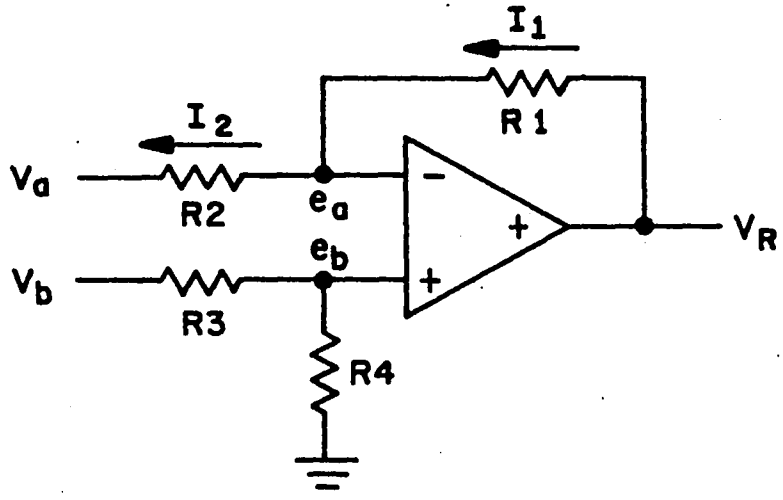
BASIC REFERENCE CIRCUIT NODE VOLTAGE
AS A FUNCTION OF TEMPERATURE

FIGURE 3



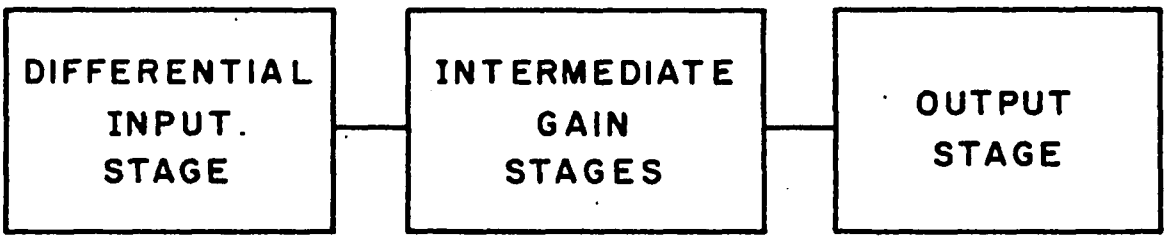
DIFFERENCE VOLTAGE
AS A FUNCTION OF TEMPERATURE

FIGURE 4



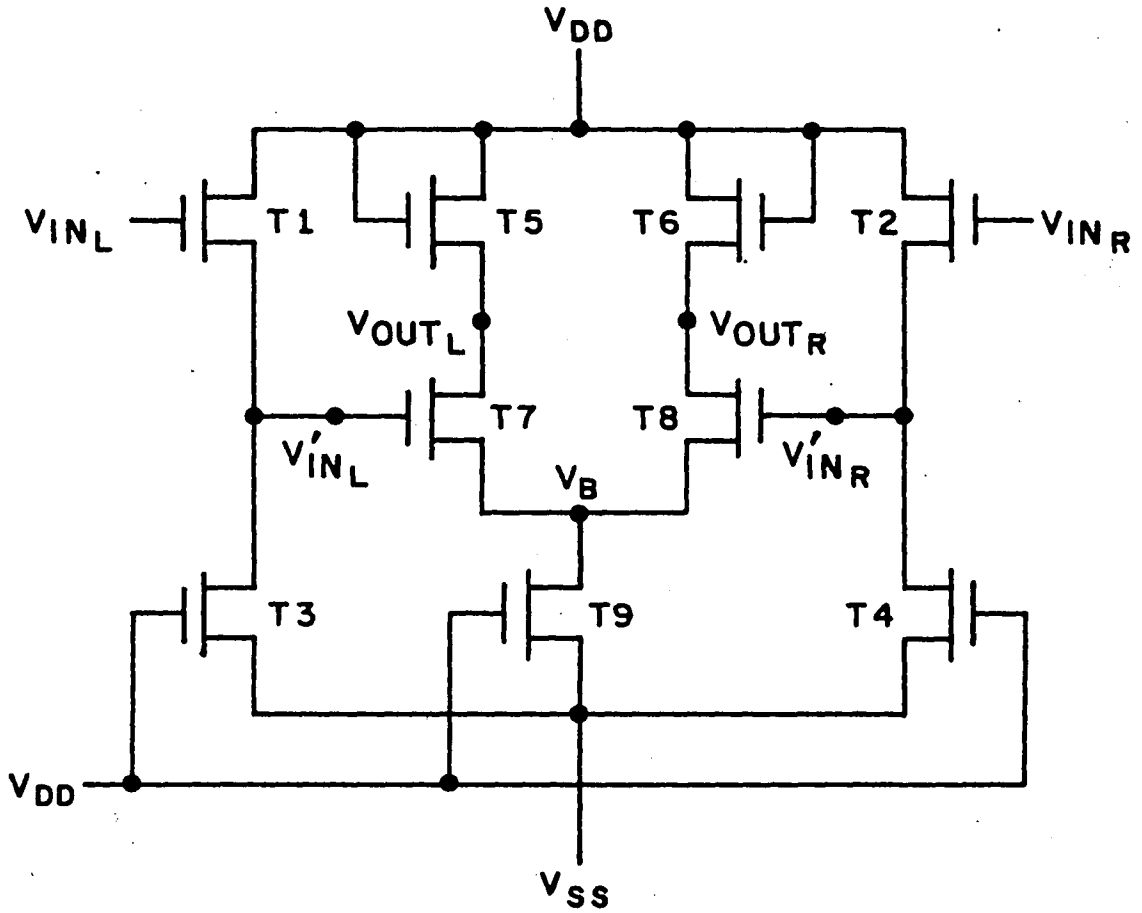
VOLTAGE DIFFERENCE CIRCUIT

FIGURE 5



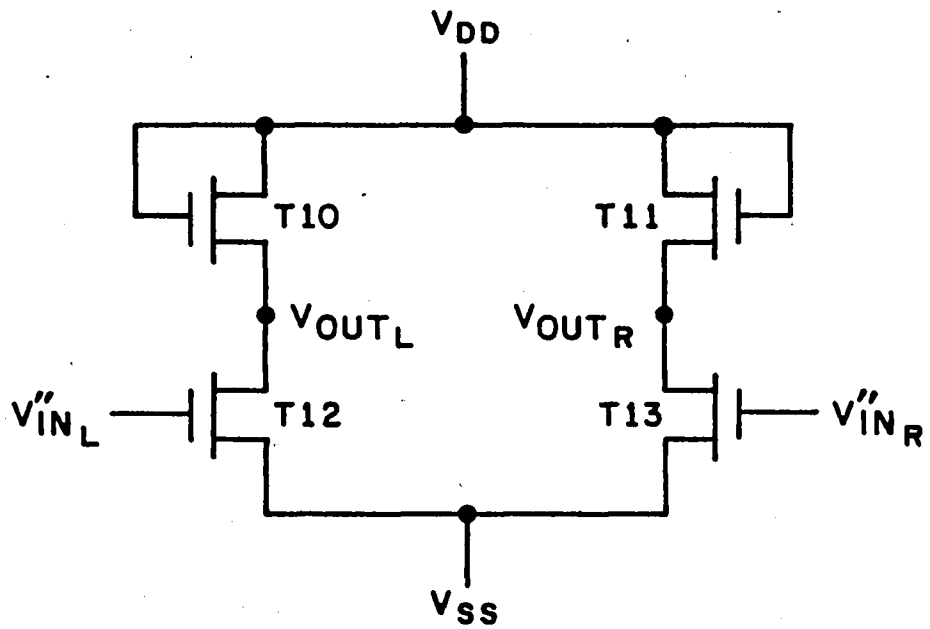
STRUCTURE OF OPERATIONAL AMPLIFIER

FIGURE 6



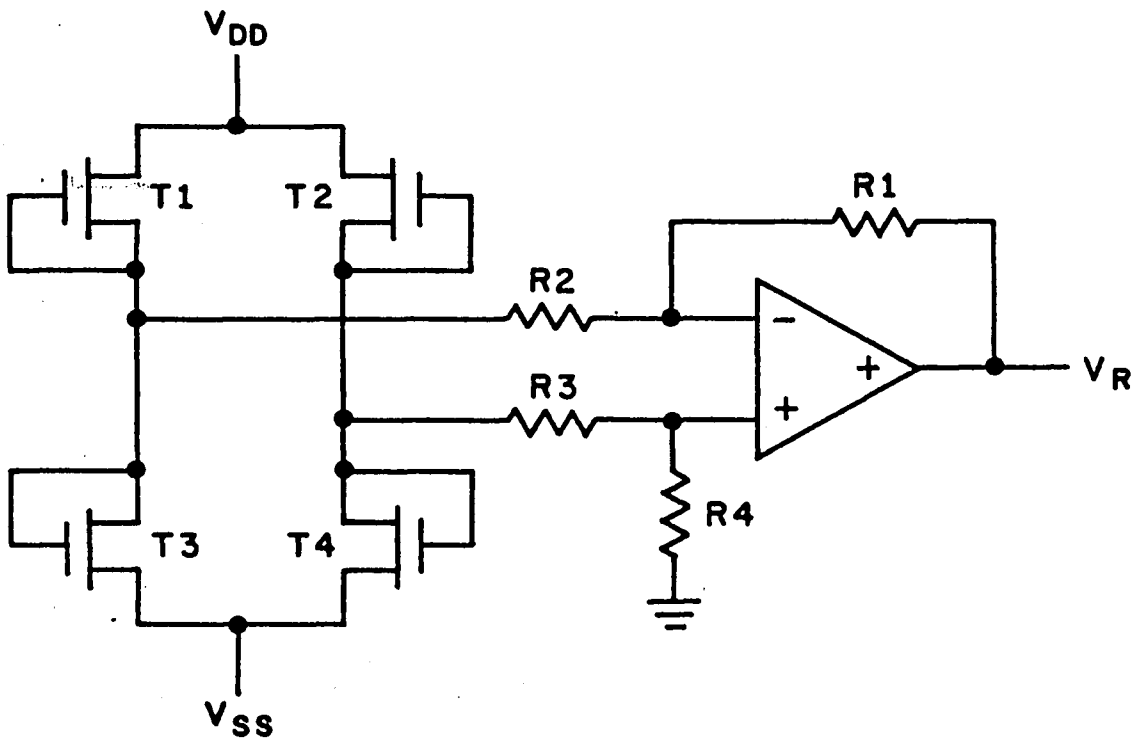
DIFFERENTIAL INPUT STAGE
OF OPERATIONAL AMPLIFIER

FIGURE 7



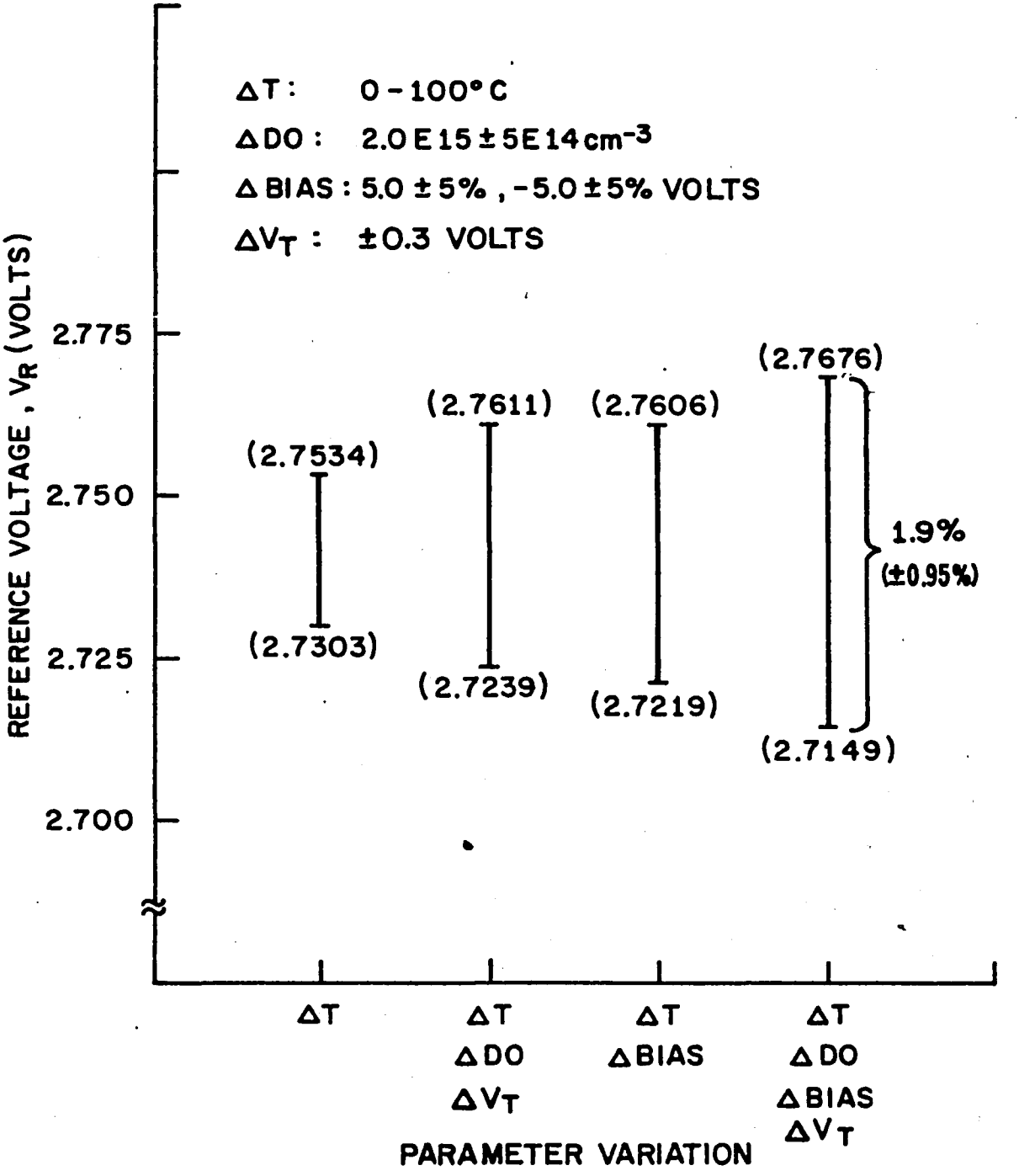
OUTPUT STAGE
OF OPERATIONAL AMPLIFIER

FIGURE 8



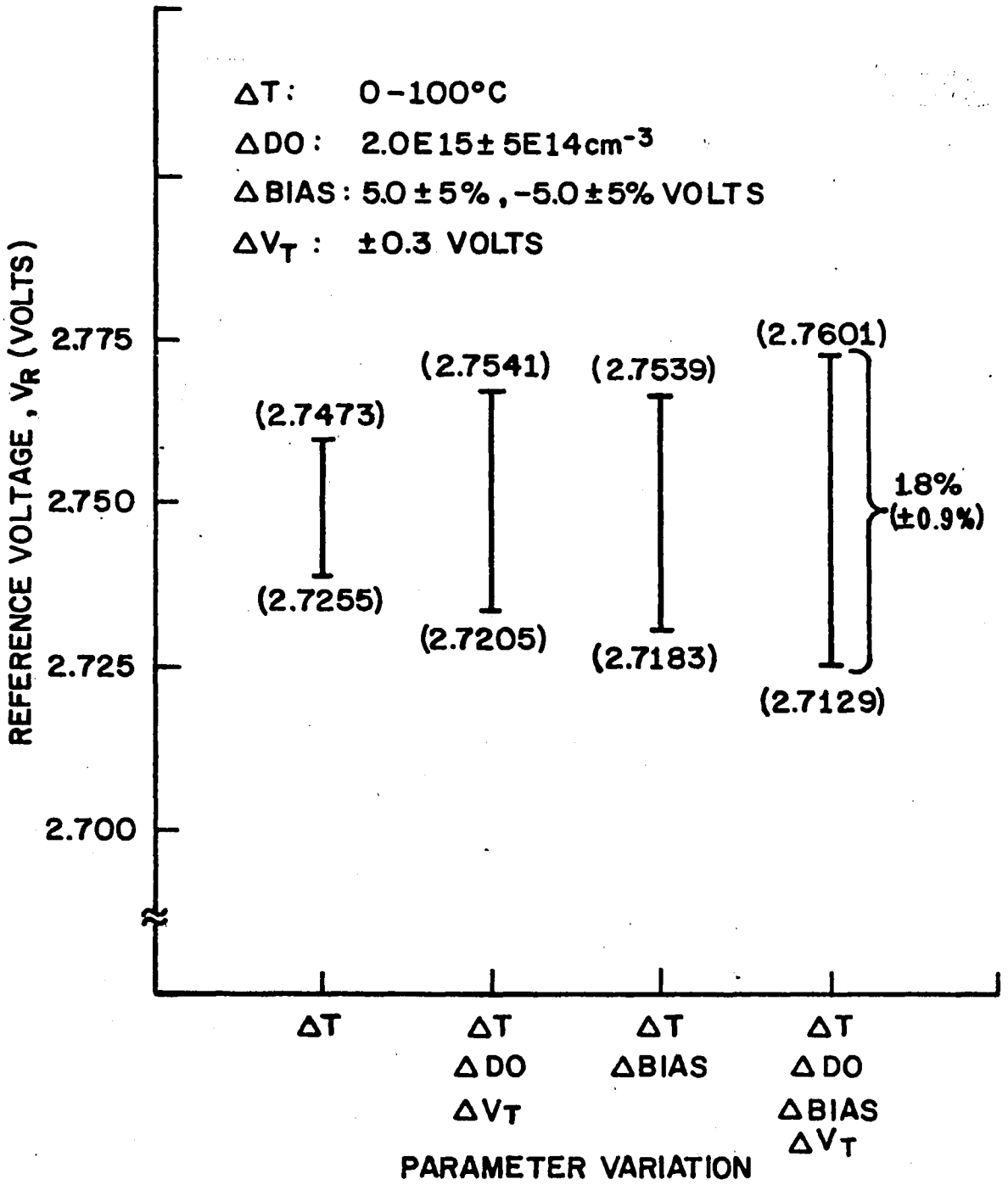
COMPOSITE REFERENCE CIRCUIT

FIGURE 9



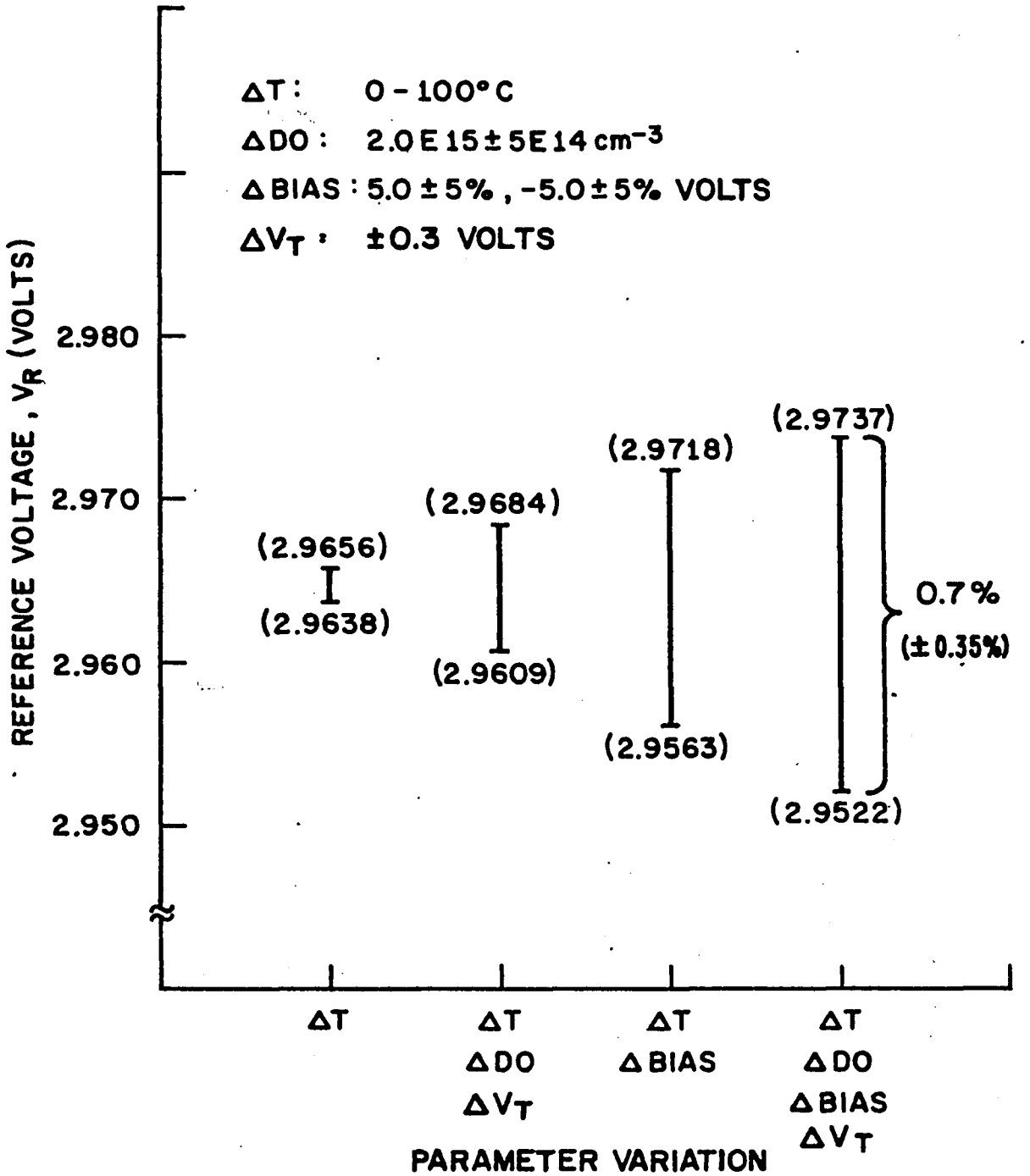
CIRCUIT 1 - REFERENCE VOLTAGE AS A FUNCTION OF PARAMETER VARIATIONS

FIGURE 10



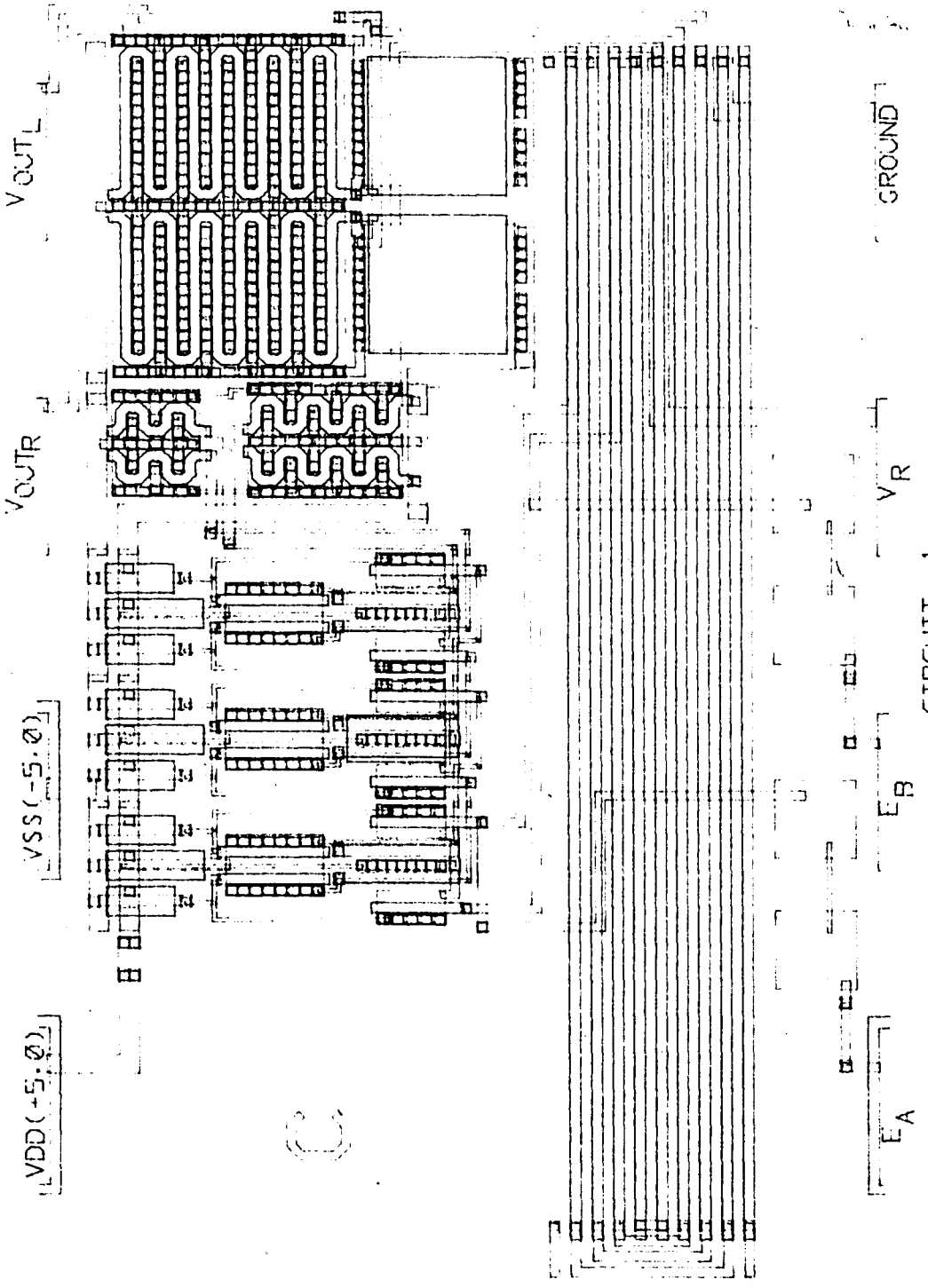
CIRCUIT 2 - REFERENCE VOLTAGE AS A FUNCTION OF PARAMETER VARIATIONS

FIGURE 11



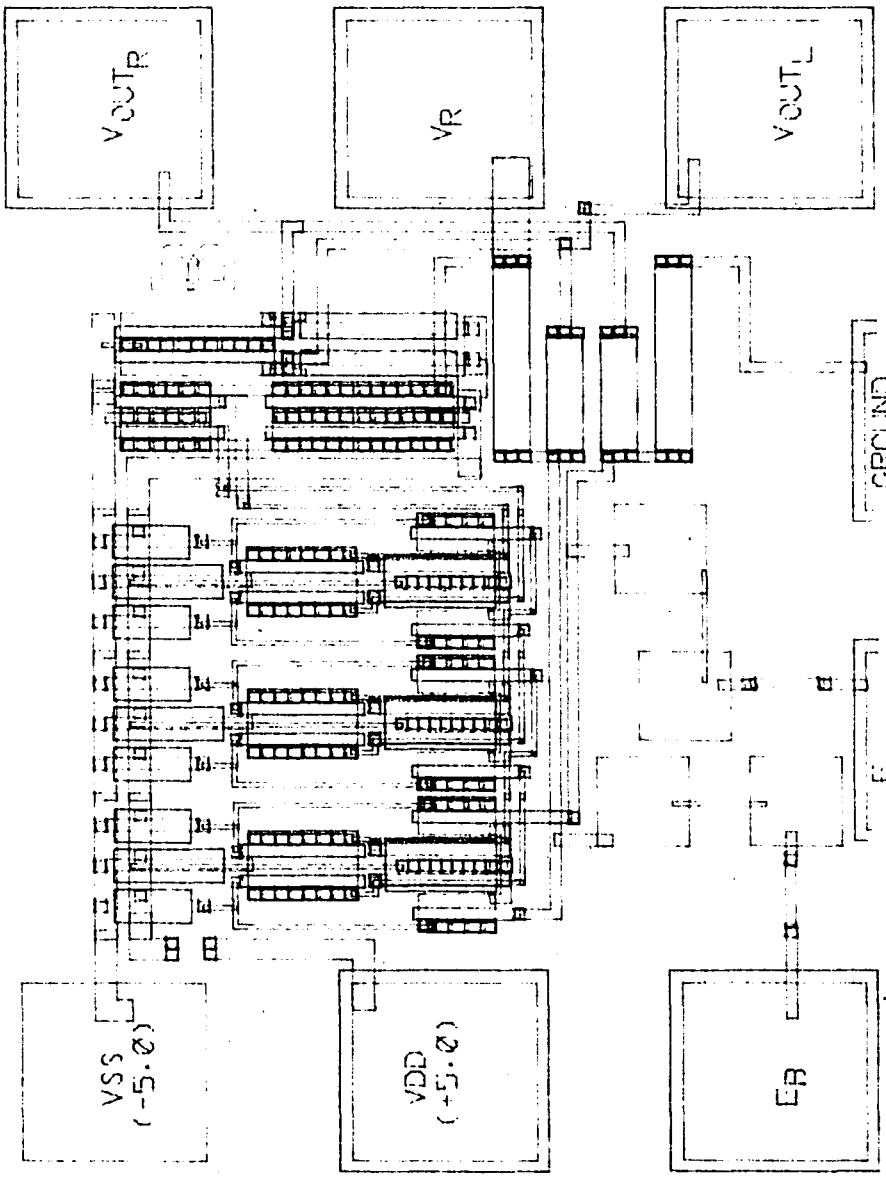
CIRCUIT 3 - REFERENCE VOLTAGE AS A FUNCTION OF PARAMETER VARIATIONS

FIGURE 12



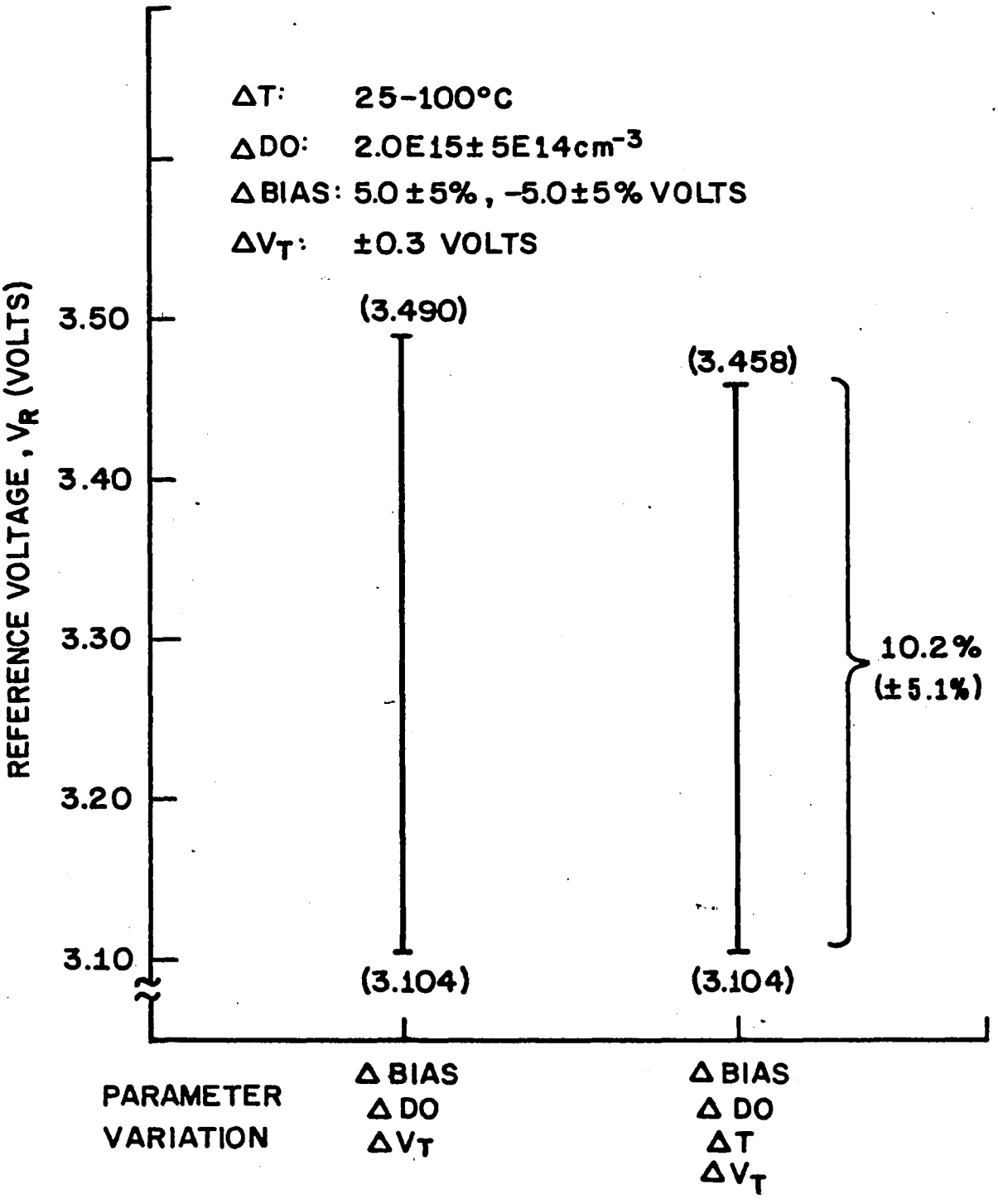
CIRCUIT 1

FIGURE 13



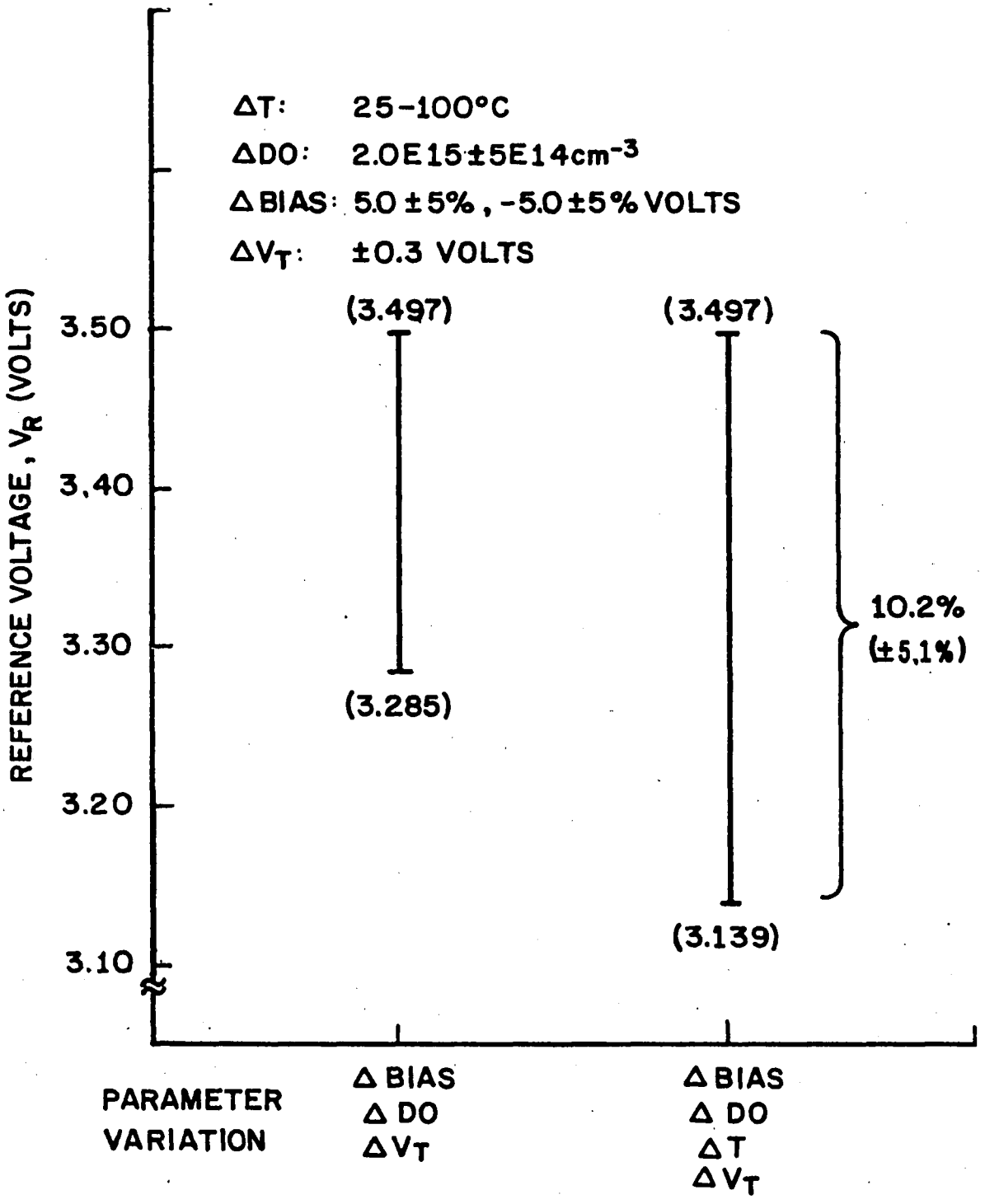
CIRCUIT 6

FIGURE 14



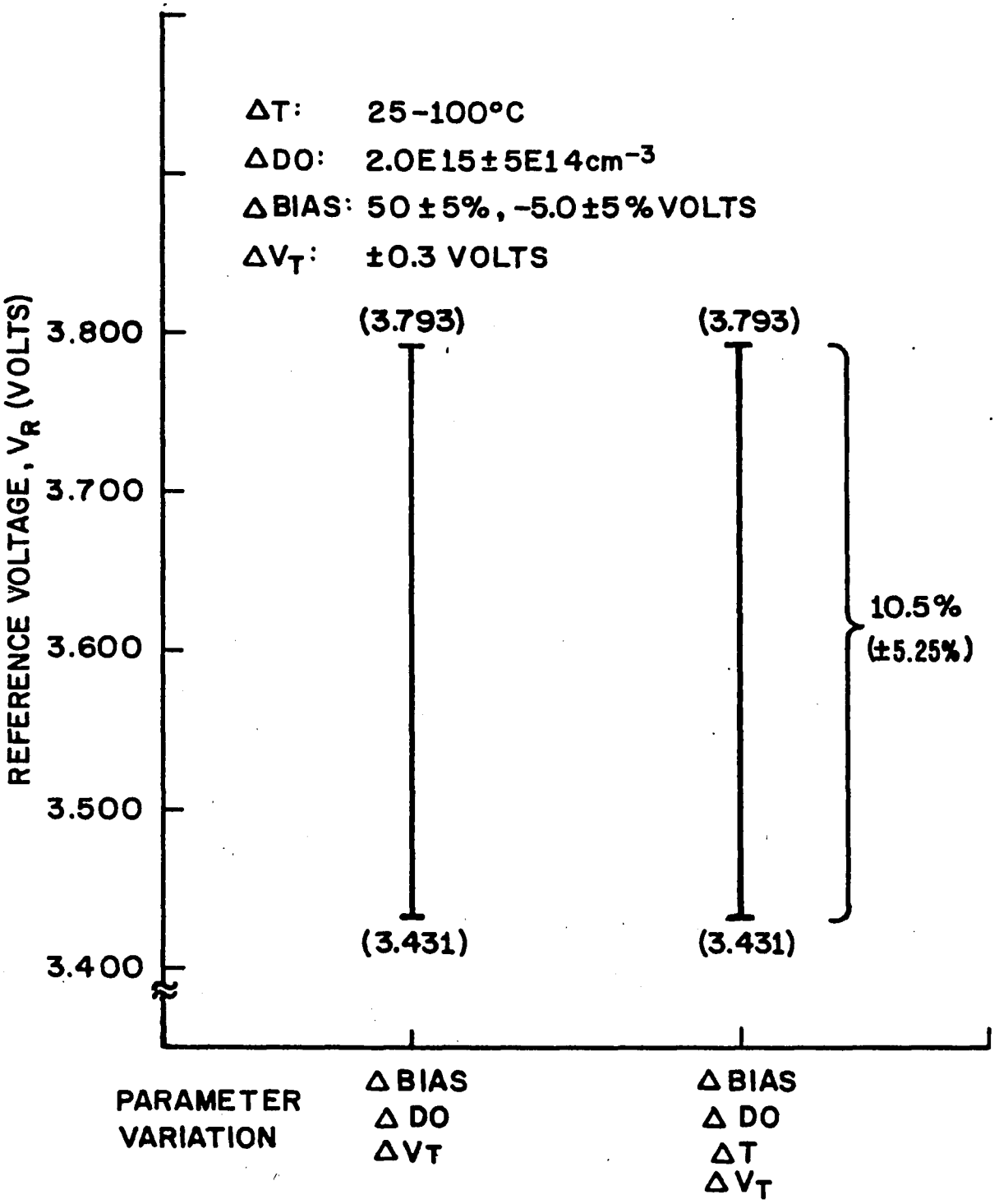
CIRCUIT 1 – EXPERIMENTAL RESULTS OF REFERENCE VOLTAGE AS A FUNCTION OF FABRICATED PARAMETER VARIATIONS

FIGURE 15



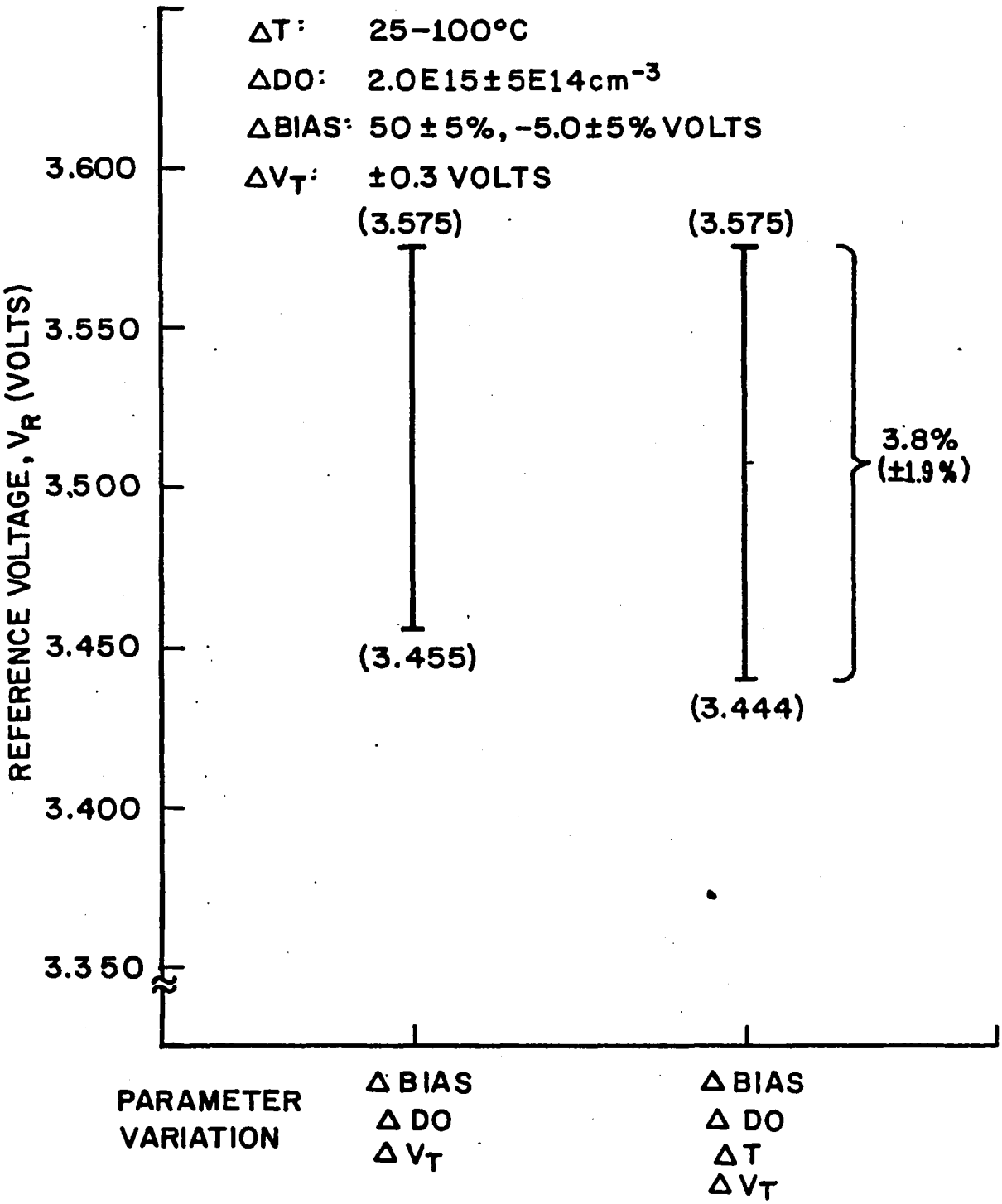
CIRCUIT 2- EXPERIMENTAL RESULTS OF REFERENCE VOLTAGE AS A FUNCTION OF FABRICATED PARAMETER VARIATIONS

FIGURE 16



CIRCUIT 1 – SIMULATION RESULTS OF REFERENCE VOLTAGE AS A FUNCTION OF FABRICATED PARAMETER VARIATIONS

FIGURE 17



CIRCUIT 2 – SIMULATION RESULTS OF REFERENCE VOLTAGE AS A FUNCTION OF FABRICATED PARAMETER VARIATIONS

FIGURE 18

REFERENCES

1. R. A. Blauschild, P. A. Tucci, R. S. Miller, and R. G. Meyer, "A New NMOS Temperature-Stable Voltage Reference", IEEE Journal of Solid-State Circuits, Vol. SC-13, pp. 767-774, December, 1978.

2. W. J. Butler and C. W. Eichelberger, "Temperature-Stable MOSFET Reference Voltage Source", Technical Digest 1976 International Election Devices Meeting, pp. 587-589, December, 1978.

3. Y. P. Tsividis and R. W. Ulmer, "A CMOS Voltage Reference", IEEE Journal of Solid State Circuits, Vol. SC-13, pp. 774-778, December, 1978.

4. G. Schottky, "Decrease of FET Threshold Voltage Due To Boron Depletion During Thermal Oxidation", Solid-State Electronics, Vol. 14, pp. 467-474, June, 1971.

5. V. L. Rideout, F. H. Gaeneslen, and A. LeBlanc, "Device Deisgn Considerations for Ion Implanted n-Channel MOSFETs", IBM Journal of Research and Development, Vol. 19, pp. 50-59, January, 1975.

6. W. E. Dahlke, Professor at Lehigh University, private communication.

7. G. Doucet and F. VanDeWiele, "Threshold Voltage Of Nonuniformly Doped MOS Structures", Solid-State Electronics, Vol. 16, pp. 417-423, March, 1973.

8. J. S. T. Huang and G. W. Taylor, "Modeling of an Ion-Implanted Silicon-Gate Depletion-Mode IGFET", IEEE Transactions On Electron Devices, Vol. ED-22, pp. 995-1001, November, 1975.

9. A. S. Grove, Physics and Technology of Semiconductor Devices, John Wiley and Sons, Inc., 1967.

10. L. W. Nagel and D. O. Pederson, "Simulation Program with Integrated Circuit Emphasis", Proc. Sixteenth Midwest Symposium on Circuit Theory, Waterloo, Canada, April 12, 1973.

11. J. Millman and C. C. Halkias, Integrated Electronics, Mc-Graw-Hill Book Co., 1972.

12. D. J. Hamilton and W. G. Howard, Basic Integrated Circuit Engineering, McGraw-Hill Book Co., 1975.

13. R. H. Crawford, MOSFET in Circuit Design, McGraw-Hill Book Co., 1967.

14. W. N. Carr and J. P. Mize, MOS/LSI Design and Application, McGraw-Hill Book Co., 1972.

15. A. B. Grebene, Analog Integrated Circuit Design, Van Nostrand Reinhold Co., 1972.

16. R. Wang, J. Dunkley, T. DeMassa, and L. Jelsma, "Threshold Voltage Variations with Temperature in MOS Transistors", IEEE Transactions on Electron Devices, Vol. ED-18, pp. 386-388, June, 1971.

VITA

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