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Design and Fabrication of a Beam-Leaded 10 Volt Silicon Regulator Diode Using Arsenic Implant Technology.

F M. Ogukeck

Design and Fabrication of a Beam-Leaded 10 Volt Silicon Regulator Diode Using Arsenic Implant Technology

by

F. M. OGURECK

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Professor in Charge

Chairman of Department

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I. Abstract

This thesis discusses the design and development of a beam-leaded 10 volt silicon regulator diode using arsenic implant technology to form the junction. Characterization data, both electrical and thermal, are also contained in the paper.

The application for the 10 volt regulator diode is as a level shifter in a driver hybrid integrated circuit that requires a pair of devices that are matched to within one percent for breakdown voltage at an operating current of I_R=10mA. The HIC is part of an 18 GHz digital transmission system.

Arsenic implantation technology was chosen over standard diffusion techniques in order to take advantage of the uniformity of properties associated with this process. Results indicate that very uniform electrical characteristics for breakdown voltage (V_{BR}) and forward voltage (V_F) are realized over a single wafer. Tight control of the breakdown characteristic is important because of the one percent matching requirement on diode pairs by the circuit application.

II. Introduction

This thesis describes the design and development of a silicon beam-leaded 10 volt regulator diode. The device is one of a matched pair utilized as a level shifter in a driver hybrid integrated circuit. This circuit is part of an 18 GHz digital transmission system. Ion implant technology is used to form the arsenic N^+ junction. Previously, encapsulated regulator diodes utilized diffused junctions from both boron and arsenic sources. The advantage of using an implanted arsenic junction is the potential of precise control and uniformity of properties associated with this process. Thus, very uniform electrical characteristics can be realized over a single wafer, and wafer to wafer variations can be kept to a minimum. Consequently, the use of implant technology can result in a potential increase in the overall yield for this application and a reduction of the cost of fabrication. In addition, the tight control of the electrical characteristic is important because of the matching requirement of less than one percent for the breakdown voltage of diode pairs for the circuit application. The device is a prototype for a potential family of low voltage regulators utilizing beam-lead sealed junction and ion implant technology.

Included in this paper are details relating to the design, development and fabrication of the device, distributions of the device electrical parameters and specific characterization data.

III. Review of Voltage Breakdown Theory[1,2,3]

In a PN junction in silicon, breakdown is primarily a function of two mechanisms: Zener which is a tunneling process and avalanche multiplication.

The Zener or tunneling effect is dominant for junctions with a breakdown voltage less than $4E_{g/q}$. Consequently, the junction must have relatively high doping concentrations, in excess of 10^{18} cm^{-3}, on both the n and p sides. In order for tunneling to take place, a very high electric field on the order of 10^6 V/cm is necessary. This initiates electron and hole conduction which corresponds to a transition of an electron from the valence band to the conduction band. In other words, the electron tunnels through the forbidden energy gap (E_g). The tunneling current density is given by

$$J_t = \frac{\sqrt{2m^* q^3 EV}}{h^2 E_g^{1/2}} \exp\left(-\frac{8\pi\sqrt{2m^*} E_g^{3/2}}{3qEh}\right)$$

where E = electric field
E_g = band gap
V = applied voltage
m* = effective mass
h = Planck's constant

Since the band gap in silicon decreases with increasing temperature, the breakdown voltage due to tunneling has a negative temperature coefficient.

The avalanche breakdown effect is dominant for junctions with a breakdown voltage greater than $6E_{g/q}$. The avalanche mechanism relies on the impact ionization of carriers. Electron-hole pairs are generated within the depletion region by the collision of high energy carriers, resulting from a strong electric field, with the lattice structure. The newly generated carrier pairs are, in turn, accelerated by the electric field to produce more collisions to generate additional carrier pairs. This process results in a multiplication effect of carriers termed avalanching and eventually leads to the breakdown of the junction (see Figure (a) below).

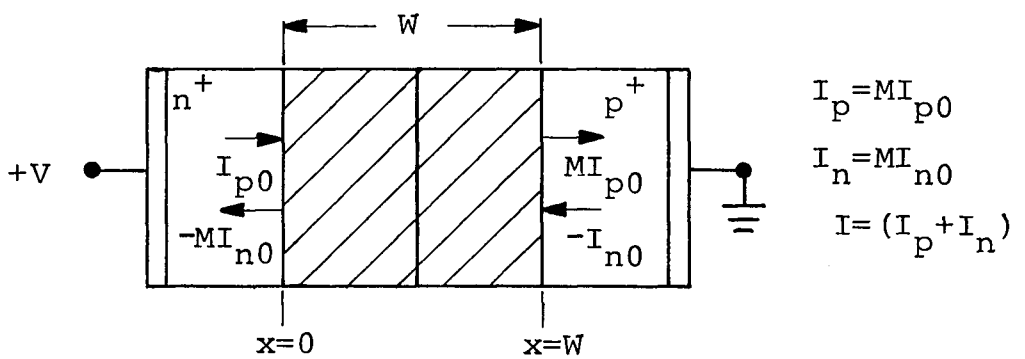

Figure (a) Avalanche Multiplication of Holes and Electrons in the Depletion Region

If the avalanche process is initiated by holes, the incremental hole current at x is given by Equation (1).

$$\frac{dI_p}{dx} - (\alpha_p - \alpha_n) I_p = \alpha_n I \qquad (1)$$

Similarly, if the avalanche process is initiated by electrons, the incremental electron current is given by Equation (2).

$$\frac{dI_n}{dx} - (\alpha_n - \alpha_p) I_n = \alpha_p I \qquad (2)$$

where

$$\alpha = A \exp\left(-\left[\frac{b}{E(x)}\right]^m\right) \qquad (3)$$

and for electrons

$A = 3.8 \times 10^6$ cm^{-1}

$b = 1.75 \times 10^6$ V/cm

$m = 1$

for holes

$A = 2.25 \times 10^7$

$b = 3.26 \times 10^6$

$m = 1$

The solutions of Equations (1) and (2) with the following boundary conditions

$I = I_p(W) = M_p I_{po}$ for holes

$I = I_n(o) = M_n I_{no}$ for electrons

are given as follows.

For holes,

$$1 - \frac{1}{M_p} = \int_o^W \alpha_p \exp\left[-\int_o^x (\alpha_p - \alpha_n)dx'\right]dx \qquad (4)$$

For electrons,

$$1 - \frac{1}{M_n} = \int_o^W \alpha_n \exp\left[-\int_x^W (\alpha_n - \alpha_p)dx'\right]dx \qquad (5)$$

where

$$M_p = \frac{I_p(W)}{I_p(o)}$$

and

$$M_n = \frac{I_n(o)}{I_n(W)} \quad .$$

The avalanche breakdown is defined as the voltage where M_p or M_n become infinite. Thus, Equations (4) and (5) reduce to Equations (6) and (7).

$$\int_o^W \alpha_p \exp\left[-\int_o^x (\alpha_p - \alpha_n)dx'\right]dx = 1 \qquad (6)$$

$$\int_o^W \alpha_n \exp\left[-\int_x^W (\alpha_n - \alpha_p)dx'\right]dx = 1 \qquad (7)$$

If both electrons and holes contribute to the avalanche process, the breakdown condition is given by solving Equations (6) and (7) simultaneously.

Poisson's equation states that

$$\frac{dE}{dx} = \frac{\rho}{K_S \varepsilon_o} \qquad (8)$$

where ρ = charge density per unit volume q/cm^3

K_S = dielectric constant

$\varepsilon_o = 8.86 \times 10^{-14}$ F/cm

The ionization rate α given by Equation (3) is a function of the electric field. From the above breakdown conditions (Equations (6) and (7)), the solutions of Poisson's equation for the electric field and potential and the field dependence of the ionization rates, the maximum electric field and depletion layer width can be calculated. From this is derived the breakdown conditions for the abrupt junction

$$V_B = \left(\frac{K_S \varepsilon_o E_m^2}{2q}\right) \left(\frac{1}{N_B}\right) \tag{9}$$

and for the linear junction

$$V_B = \frac{4E_m^{3/2}}{3} \sqrt{\frac{2K_S\varepsilon_o}{qa}} \tag{10}$$

where N_B = background doping

a = impurity gradient

E_m = maximum electric field

For the 10 volt regulator diode, the primary breakdown mechanism is avalanche multiplication. Consequently, the temperature coefficient is positive.

IV. Device Structure

The device structure consists of a 500μm square chip with four gold beams extending from the chip as shown in Figure 1. The beams are 80μm wide and extend 170μm from the edge of the chip. The beam with the flag indicates the one that connects to the N^+ junction, the beam directly opposite connects to the P^+ substrate. The purpose of the two other beams is primary for mechanical stability in handling and bonding. The beams are offset in order to obtain the maximum possible number of devices on a wafer. Thick gold (~12μm) is utilized for the entire gold pattern in order to insure good thermal characteristics. The active N^+ contact is a 160μm diameter dot, Figure 1, the area being 2.01×10^{-4} cm^2. The P^+ substrate contact consists of a horseshoe-shaped area 2.15×10^{-4} cm^2 (Figure 1).

V. Design Considerations

A. Electrical

In the design of the 10 volt regulator diode, particular attention was paid to the matching requirement of a pair of devices to match within one percent for breakdown voltage. Arsenic implant technology was chosen over diffusion techniques in order to take advantage of the uniformity of properties associated with this technique.

Low resistivity starting material (.014 to .018 Ωcm) was chosen in order to keep series resistance to a minimum. Tentative requirements of the circuit are given in Table I.

TABLE I

Parameter	Test Condition	Min.	Nom.	Max.
I_S	V_R=1V			0.1μA
* BV	I_R=10mA	9.5V	10.0V	10.5V
Z_{br}	I_R=10mA i_R=1mA F=1KC			17.0Ω
TCBV	I_R=10mA		+6mV/°C	

*Matched pair required for circuit within ±1.0%.

B. Thermal and Mechanical

The actual device design required consideration of heat dissipation associated with the device's relatively high current (I_R=10mA) requirement. In order to lower the heating effects, thick gold (12 μm) was utilized over all the metallization paths and beams. This is a change from the standard fabrication techniques where thin gold (1 to 2 μm) normally is utilized over the metallization paths on the chip and thick gold is used only for the beams. Results of thermal analyses[4] (see Figures 2,3) for ideal conditions indicates that the operating temperature

at the circuit bias conditions (I_R=10mA) will be approximately 34.6°C above the ambient. Actual junction temperature measured on devices operated at I_R=10mA is approximately 36.5°C above the ambient which is somewhat higher than the model predicts. This is expected since the simple model relates to ideal conditions. Figure 3 is a plot of the temperature rise as a function of dissipated power. Both the measured curve and a calculated value at 100mw are included.

Four beams are included in the design structure, only two of which are electrically active. The remaining two beams are intended to facilitate mechanical stability in handling of the devices during subsequent testing and bonding operations.

VI. Experimental Work

A range of starting material from .007 Ωcm to .020 Ωcm boron doped P-type bulk material with a <111> crystal orientation and a reference flat cut on the <211> plane were used to make control samples in order to determine a suitable range in starting material. Silicon dioxide was thermally grown to a thickness of 8000 angstroms and 400μm diameter windows were opened to implant the arsenic junction. The arsenic dose utilized for this phase of the experiment was 5.0×10^{15} cm^{-2} implanted at 50 keV.

From the results of the experiment, the suitable range of starting material for the 10 volt diode was

selected to be from .014 to .018 Ωcm. With this range of starting material, the variation of the breakdown characteristics could be held to less than ±5 percent. Lower resistivity material such as .007 Ωcm required longer drive-in times at 1270°C (200 minutes), and resulted in a sheet resistance (ρ_S) that was relatively high (130 Ω/□). In addition, the surface concentration calculated from the gaussian profile was also lower, 2.3×10^{19} cm^{-3}, which was very close to the substrate doping of approximately 1.6×10^{19} cm^{-3}. Actual devices that were fabricated ended up as shorts after metallization, although diode characteristics were measured prior to metallization. These characteristics tended to be unstable and relatively soft. It is possible that some probe damage was occurring because of the shallower junctions.

Samples with Van der Pauw patterns,[5,6] on which four point measurements are made at the periphery of samples with arbitrary shapes, were also processed on .017 Ωcm material for sheet resistance measurements. The implanted arsenic dose used for this phase ranged from 1.0×10^{15} cm^{-2} to 5.0×10^{15} cm^{-2} at 50 KeV. The purpose was to determine if the use of a lower arsenic dose was feasible for application to the 10 volt diode.

Both 1200°C and 1270°C drive-in temperatures were investigated. Two different gas flows were also investigated: 100 percent nitrogen and a 50 percent nitrogen,

50 percent oxygen mixture. In Figures 4 and 5 are given the results for sheet resistance and junction depth as a function of arsenic dose for both a 4-hour 1200°C and 2-hour 1270°C drive-in process. The sheet resistance was measured on 20 Van der Pauw patterns on each sample across the center of the wafer, 10 from the top to bottom and 10 from left to right. Junction depth was measured through angle lap and staining techniques. Measurements of ρ_S obtained on each sample were very uniform. With decreasing arsenic dose, the breakdown voltage increased slightly (approximately 1.0 volt for a range of arsenic of 5.0×10^{15} cm^{-2} to 2.0×10^{15} cm^{-2} for the 1270°C drive-in of 2 hours), while ρ_S increased quite rapidly as is shown in Figure 4. Consequently, the surface concentration decreased as indicated in Figure 6. It was decided to use an arsenic dose of 5.0×10^{15} cm^{-2} for the fabrication of the 10 volt diode in order to insure a low ρ_S and a relatively high surface concentration. In addition, the 1270°C drive-in was done in 50 percent nitrogen and 50 percent oxygen since the 2000 to 2500 angstrom layer of silicon dioxide resulting from the drive-in acts as a cap to insure that the arsenic is retained on the surface. The arsenic profile that is obtained is discussed in a later section.

The number of samples that were run in the experiments were limited, and no statistical data was obtained to

indicate the range of variations due to the ion implant and drive-in processes. Previous studies[7] on arsenic implanted buried layers indicate that short-time variations (over a six-week period) in sheet resistance are relatively small, the standard deviation being less than 2 percent for the drive-in process and less than 1 percent for the arsenic implant. These results represent relatively low ρ_S measurements (<15 $\Omega/\square$) on high resistivity substances (2 to 4 Ωcm). However, it is expected that control in ρ_S for the diode process may approach this degree of tightness. Experiments are planned in the future in order to determine what type variations in ρ_S can be expected.

VII. Arsenic Implanted Junction

The arsenic implant was done at 50 keV with a dose of 5×10^{15} cm^{-2} in the Reading BTL ion pre-deposit machine. In this machine, the substrate (wafer) is located on a carousel which is tilted at approximately an 8° angle toward the ion beam to obtain a random orientation of the crystal lattice to minimize channeling.[8] The drive-in diffusion was done at 1270°C in a 50 percent oxygen, 50 percent nitrogen gas mixture for 100 minutes, resulting in an approximately 2400 angstrom thermally grown silicon dioxide layer.

Figure 7 contains the profile information on the implanted arsenic junction which was determined from

differential conductivity measurements,[9] a method of measuring the conductivity of a sample in discrete steps while removing layers of silicon by controlled anodization and secondary ion mass spectrometry (SIMS) measurements. In addition, a calculated Gaussian profile[10] is included. In the determination of the calculated profile, the initial implant dose was assumed to be a Gaussian with projected range, R_p=.0324 μm, and standard deviation, ΔR_p=.0120 μm.[11] The diffusion constant was assumed to be concentration independent and was calculated from the equation:[12]

$$D_i = 22.9 \exp\left(\frac{-4.1eV}{kT}\right) = 9.39x10^{-13} \text{ cm}^2/\text{sec}$$

It can be noted in Figure 7 that the measured differential conductivity data agrees very closely with the upper portion of the calculated Gaussian profile. This agrees with theory since the surface concentration C_S approaches the intrinsic carrier concentration n_i ($2.5x10^{19}$ at 1270°C)[12,13] and the diffusion constant for arsenic can be assumed to be concentration independent. At the surface, the measured differential conductivity profile shows a higher concentration than the calculated profile which can be attributed to arsenic "pile up" due to reoxidation during drive in.[11] Secondary ion mass spectrometry (SIMS) measurements of the arsenic profile do not agree with the differential conductivity measurements or the calculated Gaussian profile. However, the junction depth indicated

from the SIMS profile agrees with the value obtained from angle lap and stain techniques (2.8 μm). More samples will be measured in the future to resolve this discrepancy. The background boron profile was also determined from secondary ion mass spectrometry[9] (SIMS). The profile indicates a dip (depletion) in the concentration (to approximately 6.4×10^{18} cm^{-3}) in the vicinity of the junction, indicating that there may be some interaction between the boron and the arsenic during the drive in diffusion.[14,15] In addition, the boron concentration at the surface was slightly higher (approximately 8×10^{18} cm^{-3}) than the initial substrate doping level of 7.4×10^{18} cm^{-3}, indicating that there may have been some diffusion of the boron toward the surface because of the electric field present due to the arsenic profile gradient.

VIII. Fabrication Process

A. Material Requirements

The starting material consists of a P-type <111> oriented boron doped bulk material with a resistivity range from .014 to .018 ohm cm. The slices include a reference flat cut on the <211> plane. Wafer diameter is approximately 1.5 inches and wafer thickness ranges from 9 to 11 mils.

B. Initial Oxidation and N^+ Contact Window

An 8000Å silicon dioxide layer is thermally grown on the slice in a 1050°C steam ambient. Positive resist

photolithography is utilized to define a 160 μm N^+ contact window (Figure 1), and buffered hydrofluoric acid to remove the oxide from the window.

C. Arsenic Implant and Drive In

The N^+ arsenic junction is obtained through the use of ion implantation techniques. A dose of 5.0×10^{15} As cm^{-2} is implanted at an energy of 50 keV. All devices that were processed were implanted in the Reading BTL ion pre-deposit machine. Details of the implant process are included in the previous section. The wafers are then cleaned using oxygen plasma techniques to remove any organic contaminant that may have been deposited during the ion implant process. The wafers are etched for a relatively short time (30 sec.) in buffered hydrofluoric acid solution to remove approximately 500 angstroms of arsenic doped SiO_2 from the surface. Drive-in of the arsenic is done at 1270°C for approximately 100 minutes in 50% N_2 and 50% O_2. This cycle results in a sheet resistance of approximately 20 Ω/□ and a junction depth of approximately 2.8 μm. In addition, approximately 2400 angstroms of silicon dioxide is thermally grown in the N^+ window. The P^+ contact window (horseshoe) is then opened utilizing positive photoresist as shown in Figure 1.

D. Silicon Nitride Deposition

After a 900°C dry oxidation for 30 minutes (approximately 200 angstroms), a layer of silicon nitride 2000

angstroms thick is deposited in a Nitrox facility for the purpose of providing a sodium ion barrier. An additional 2000 angstrom layer of silicon dioxide is deposited in the same Nitrox facility on top of the nitride. Positive photoresist is utilized to open the contact areas in the deposited SiO_2. The photoresist is removed and the wafers are placed in a solution of hot phosphoric acid to remove the Si_3N_4 from the contact areas, with the SiO_2 pattern providing the mask. A short buffered hydrofluoric acid (approximately 2 minutes) etch is used to remove the deposited SiO_2 mask pattern and oxide present in the N^+ window.

E. Metallization

After the wafer is thoroughly cleaned, it is placed in a vacuum station and a 100Å layer of platinum is RF sputtered onto the surface. The wafer is then sintered for 15 minutes at 500°C in a vacuum. It is important at this step that the contact areas be completely free of residual contaminants and oxides in order for a uniform layer of platinum silicide to form in the contact area without voids. The unreacted platinum is removed and the wafer is again placed in a vacuum station, and a 1000Å of titanium, 150Å of titanium nitride and 1000Å of platinum are RF sputtered on the surface. The slices are removed from the station and the platinum overlay pattern

is defined utilizing a positive photoresist mask. The titanium remains on the surface of the wafer after this process step to provide a conductive layer for gold plating purposes. Positive photoresist is utilized to define the areas of the pattern to be plated. Gold is plated to a thickness of 12 μm over the entire pattern as shown in Figure 1. Finally the titanium is removed and the wafer is ready for a sample front probe.

F. Separation

After a pattern of laser holes has been drilled into the pattern side of the wafer for back alignment purposes, the wafers are mounted face down with a suitable mounting media on a 100 mil thick, 2.25 inch diameter magnetic carrier and ground to a final wafer thickness of 2.5 $\pm$ .1 mils. After a suitable surface preparation, the back of the slice is plated with nickel and permalloy for magnetic handling purposes. Negative photoresist is utilized to define the chip pattern, and the devices are separated using silicon etching techniques. Buffered hydrofluoric acid is used to remove the silicon dioxide, and a plasma etching technique is used to remove the silicon nitride from the back of the beams. Finally, titanium is also removed from the back of the beams.

G. Testing

The DC electrical characteristics of the devices are back probed (probed on the back of the beams) using an

automatic test system, and bad devices are marked with ink. The devices are demounted from the mounting media, and the good ones are transferred to another magnetic carrier in a matrix array for further testing and shipping.

IX. Device Characterization

A. Breakdown Voltage and Temperature Coefficient

A plot of breakdown voltage as a function of the reverse current is given in Figure 8. Heating effects were kept to a minimum since the test time that was used on the AAI test set was on the order of 100 milliseconds. The breakdown voltage is primarily due to avalanche effects having a positive temperature coefficient (TCBV) as indicated by Figure 9. The calculated value of TCBV is 5.84 mV/°C. In addition, TCBV is current independent with the self-heating effects removed. The temperature coefficient[17] can be defined as

$$TCBV = \frac{\partial V_B}{\partial T} \Big|_{I = \text{const.}}$$

Since the curve is linear

$$TCBV = \frac{\Delta V_B}{\Delta T} \quad \left(\frac{mV}{°C}\right)$$

B. Leakage Current

Leakage current (I_R) was measured and plotted as a function of voltage at a number of temperatures (Figure 10). The leakage current consists of two components, the

current due to the generation of electron hole pairs in the depletion region given by the equation[18]

$$I_{gen} = \frac{1}{2} q \frac{n_i}{\tau_o} WA_j$$

where

n_i = the intrinsic carrier concentration

τ_o = the effective lifetime of carriers

A_j = the area of the junction

W = the depletion width

and the diffusion current given by the equation[18]

$$I_{diff} = q n_i^2 A_j \left[\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p}\right]$$

where

D_n and D_p = the diffusivity of electrons and holes

L_n and L_V = the diffusion lengths for electrons and holes

N_A and N_D = the impurity concentrations of acceptors and donors

The diffusion current component is primarily temperature dependent and dominates as temperature is increased, as indicated in Figure 10. The generation current is less temperature sensitive but is voltage dependent and dominates more at lower temperatures as indicated in the figure at the lower temperatures.

The devices exhibited very low leakage currents (<.2nA) when measured at reverse voltages less than 4.0

volts at ambients of 50°C or less. These values were difficult to measure accurately with the existing test equipment.

C. Small Signal Breakdown Impedance

The impedance in breakdown, Z_{br}, is defined as the small signal AC impedance of a diode measured at a DC reverse bias condition and is given by the equation[17]

$$Z_{br} = \frac{dV_R}{dI_R} \Big|_{I_R = \text{constant}}$$

The frequency used in the measurements was 1 KHz. The level of the AC component was made equal or less than 0.1 I_R.

Z_{br} as a function of current is plotted in Figure 11. The curve is essentially linear, but at the higher currents levels off slightly. This is due to the series resistance of the diode contributing a significant component to the total value of Z_{br}. Temperature effects on Z_{br} were found to be negligible.

D. Capacitance

The capacitance is defined by the equation[18]

$$C = C_T + C_S$$

where

$$C_T = \frac{K_S \varepsilon_o A_j}{W} \quad \text{(junction capacitance)}$$

and

$$C_S = \frac{K_o \varepsilon_o}{W_o} A_{overlay} \quad \text{(overlay stray capacitance)}$$

and where

K_S and K_o = the dielectric constants of the silicon and silicon dioxide

W and W_o = the depletion layer width for the silicon and thickness of the oxide

A_j = the area of the junction

$A_{overlay}$ = the area of the metallized pattern over the oxide for the active junction contact

The capacitance is plotted as a function of reverse voltage in Figure 12. Capacitance is defined as[18]

$$C_T = \left[\frac{qa K_S^2 \varepsilon_o^2}{12(V_R+\phi_B)}\right]^{1/3}$$

where

ϕ_B = the built-in voltage

a = impurity concentration gradient at the junction

The capacitance voltage characteristic indicates that the junction is approximately linear for $V_R > 2.0$ volts.

E. Forward Characteristics

Figure 13 is a typical forward characteristic as a function of temperature. The theoretical expression for the forward current[18] is

$$I_F(V_A) = I_o \left(\exp \frac{qV_A}{nkT} - 1\right)$$

where

I_o = the saturation current

V_A = the applied junction voltage

$n \tilde{} 1$ = an experimental constant

for values of $\exp\left(\frac{qV_A}{nkT}\right) >> 1$

$$\frac{d\ (\ln\ I)}{dV_A} = \frac{q}{nkT}$$

The value of n was calculated at three temperatures and is given in the table below.

TABLE I

Temperature °C	n	Series Resistance (Ω)
-51	1.22	.88
25	1.15	.82
150	1.11	.86

The decrease in n at high temperatures is because of the increase in the diffusion current component discussed earlier in the section on leakage current (Section VIII, Part B). Series resistance was also calculated from the curves for three temperatures and is included in the table above. There was no significant difference noted for the three measurements.

F. Avalanche Noise[3]

Small changes in reverse bias current while the diode is biased in the region of the knee will cause variations

in the breakdown voltage which appear as a noise voltage. This noise voltage is observed in the form of very fast erratic pulses and is primarily a function of the avalanche mechanism. It is caused by the switching on and off of microplasmas or small areas of the junction breaking down initially in the region of the knee. As the current is increased, additional microplasmas are formed. These microplasmas generally occur in steps of 50 to 100 μA and also emit localized light. When the current reaches a certain level, the whole junction is in breakdown and the erratic conditions diminish. Figure 14 is a sample plot of the avalanche noise as a function of reverse current. The highest peak in noise occurs at a current level of 30 μA with other lower peaks at approximately 40 μA intervals.

G. Thermal Characteristics

Figure 3 includes a plot of temperature rise as a function of dissipated power. Also included are the results of a thermal analysis based on the model in Figure 2. The measurements on the device were taken on the back of a chip bonded to a ceramic substrate in a free air ambient. The measurements were made with a radiometric microscope with the diode biased in the reverse direction. Results indicate a linear characteristic (temperature vs. power) up to nearly 200 mW. Above this power level, the

curve is slightly nonlinear. This nonlinearity may be attributed to a non-uniform current density occurring at high current levels that may be causing localized hot spots. However, this is well above the normal range of the expected operating level of the device. The thermal impedance (θ_J) calculated in the linear portion of the curve is 366°C/W.

X. Yields and Distributions

Distributions of various device characteristics are summarized in Figures 15 to 19. This data represents a random sample taken from a single slice. In all, three good slices have been finished, and all exhibited similar characteristics. Potential yields ranged from 56% to 69% for the three slices. As indicated in the distribution of the breakdown voltage, approximately 90% of the good devices would meet a 1% matching requirement at I_R=10mA.

XI. Reliability

Reliability studies for the beam-leaded silicon 10 volt regulator diode are being initiated. However, some indication of the reliability can be obtained from results on packaged devices. Figure 20 represents life regression curves of a standard low voltage packaged device with no silicon nitride passivation. It is anticipated that the beam-leaded regulator diode would show improve reliability as compared to the packaged device because of silicon

nitride passivation. In addition, since the operating point (100 mW) for the device would tend to raise the junction temperature only 36.5°C above the ambient, excellent reliability can be expected.

XII. Summary

The design and fabrication of a beam-leaded 10 volt silicon regulator diode using arsenic implant technology was described. Typical device characteristics and sample distributions were presented and discussed. Initial results indicate that the device will have no problem in meeting the one percent matching requirement of pairs for the level shifter circuit application.

The device is a prototype for a family of beam-leaded low voltage regulator diodes.

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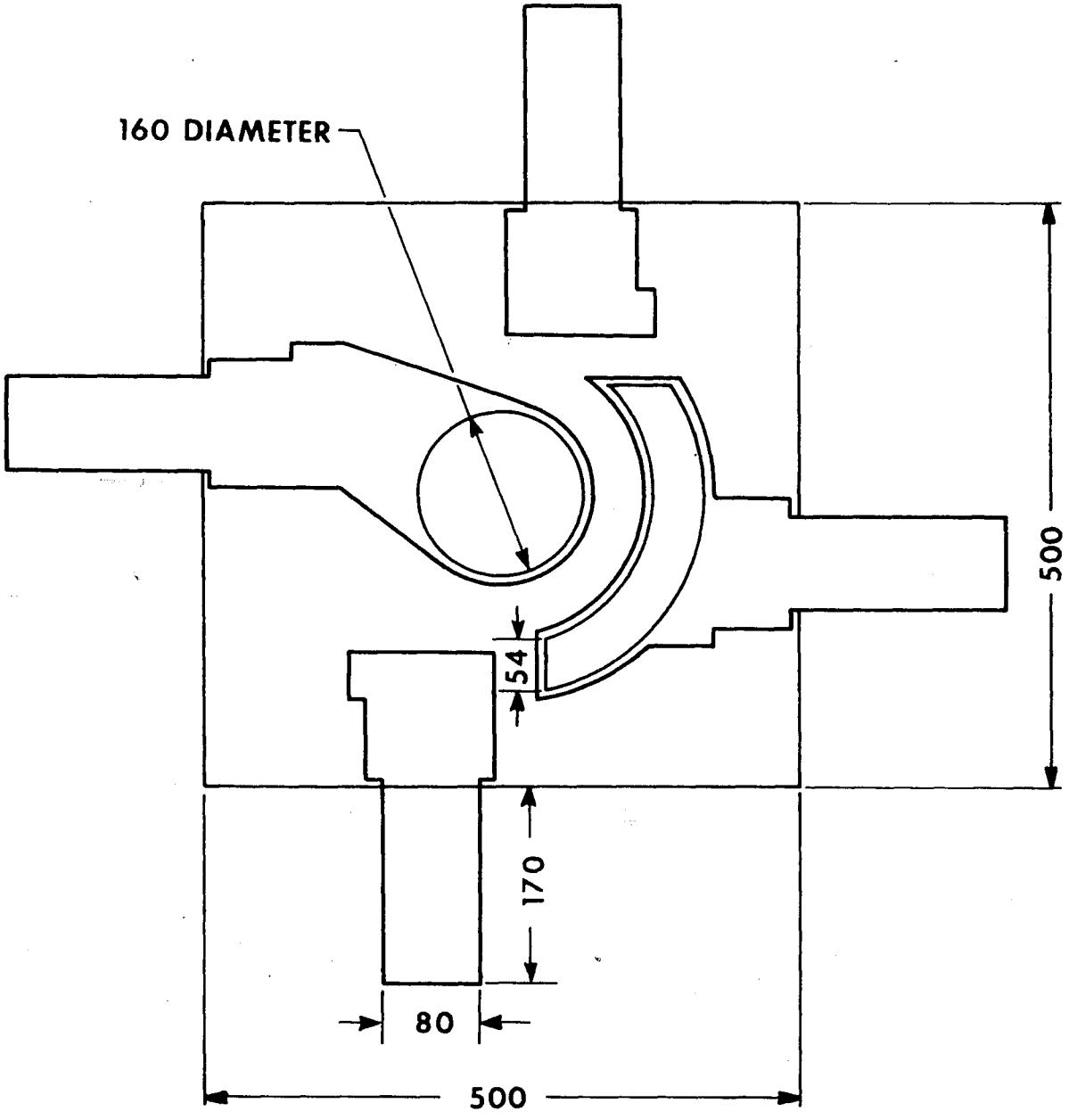
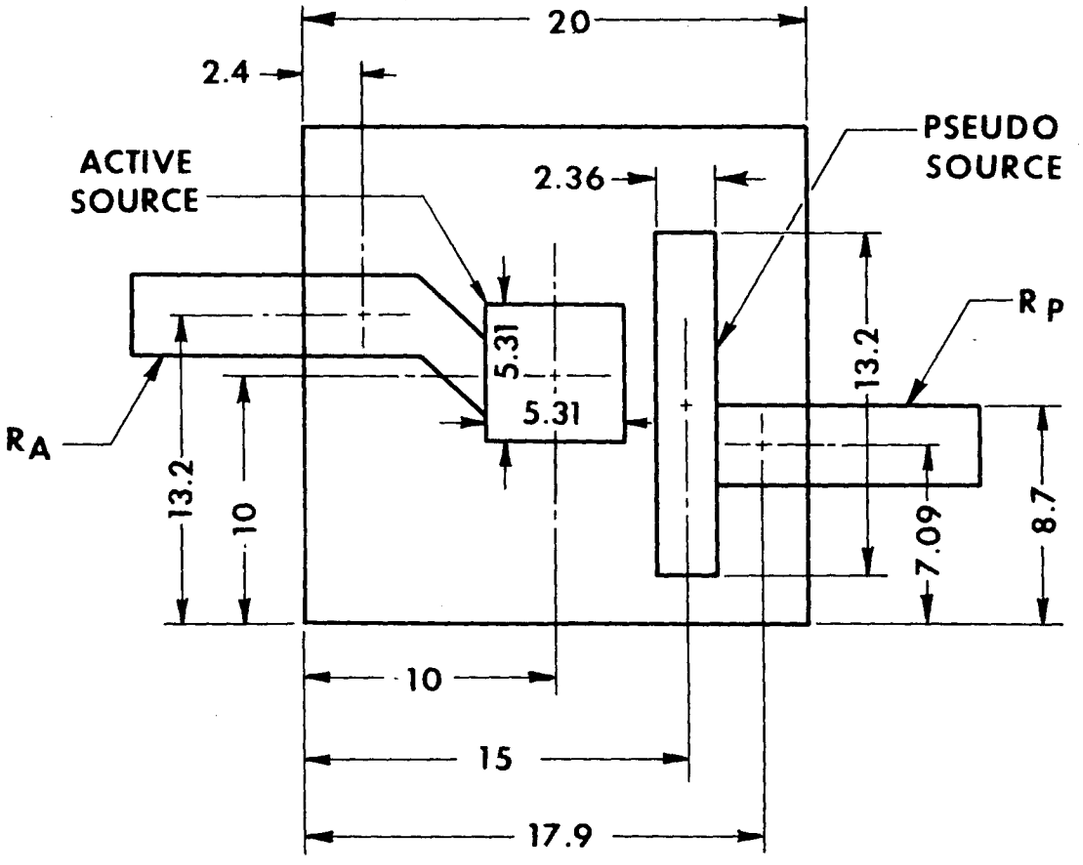
BEAM LEADED 10 VOLT DIODE



ALL DIMENSIONS ARE IN μm

FIGURE 1

MODEL FOR THERMAL ANALYSIS (TASIC)



ALL DIMENSIONS IN MILS

R_A=582.8 °C/W

Rp=443.7 °C/W

FIGURE 2

JUNCTION TEMPERATURE RISE AS A FUNCTION OF DISSIPATED POWER

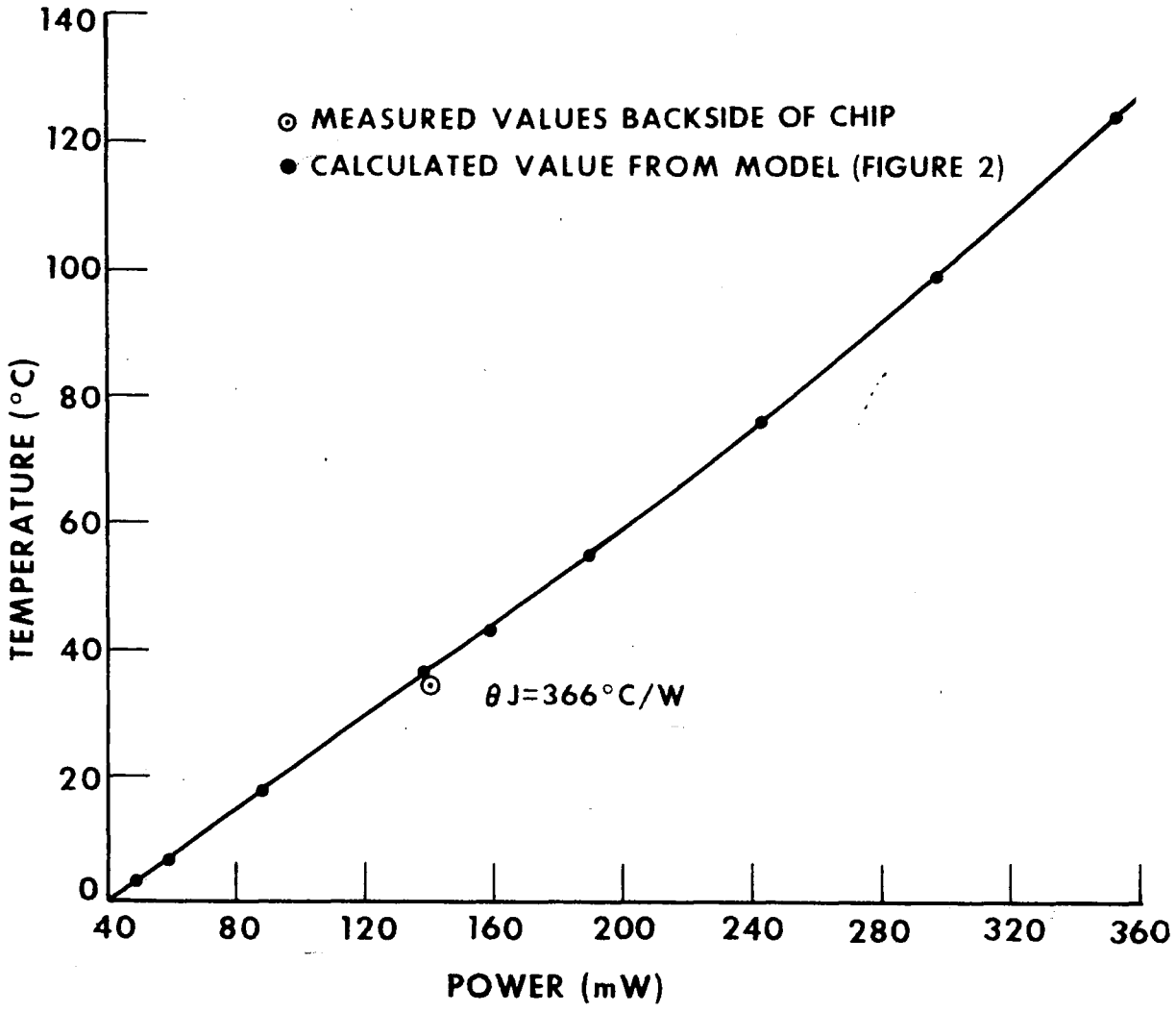


FIGURE 3

SHEET RESISTANCE (Rs) AS A FUNCTION OF ARSENIC IMPLANT DOSE (50KeV) SUBSTRATE RESISTIVITY = .017 cm

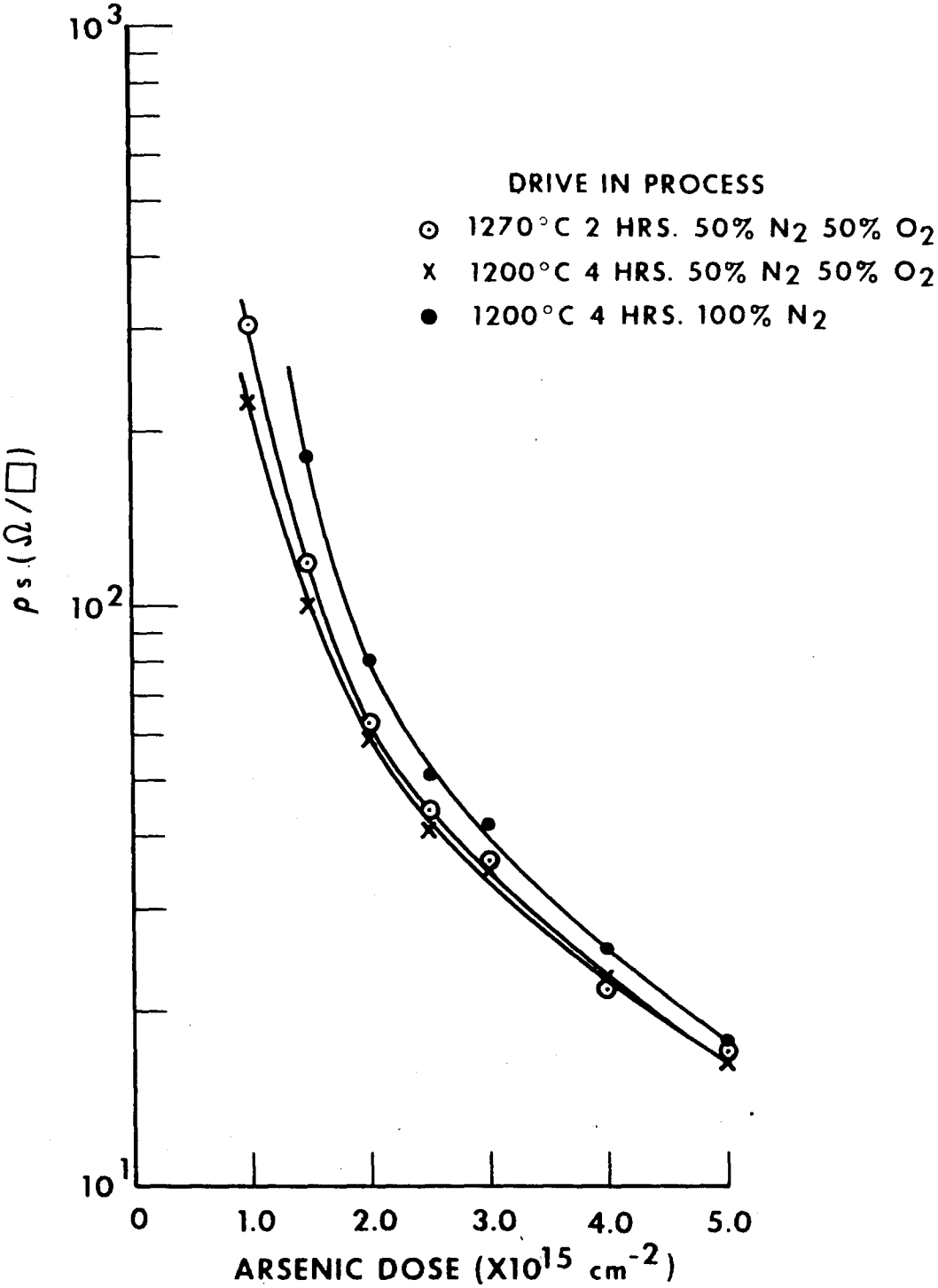


FIGURE 4

JUNCTION DEPTH AS A FUNCTION OF ARSENIC IMPLANT DOSE SUBSTRATE RESISTIVITY .017 cm

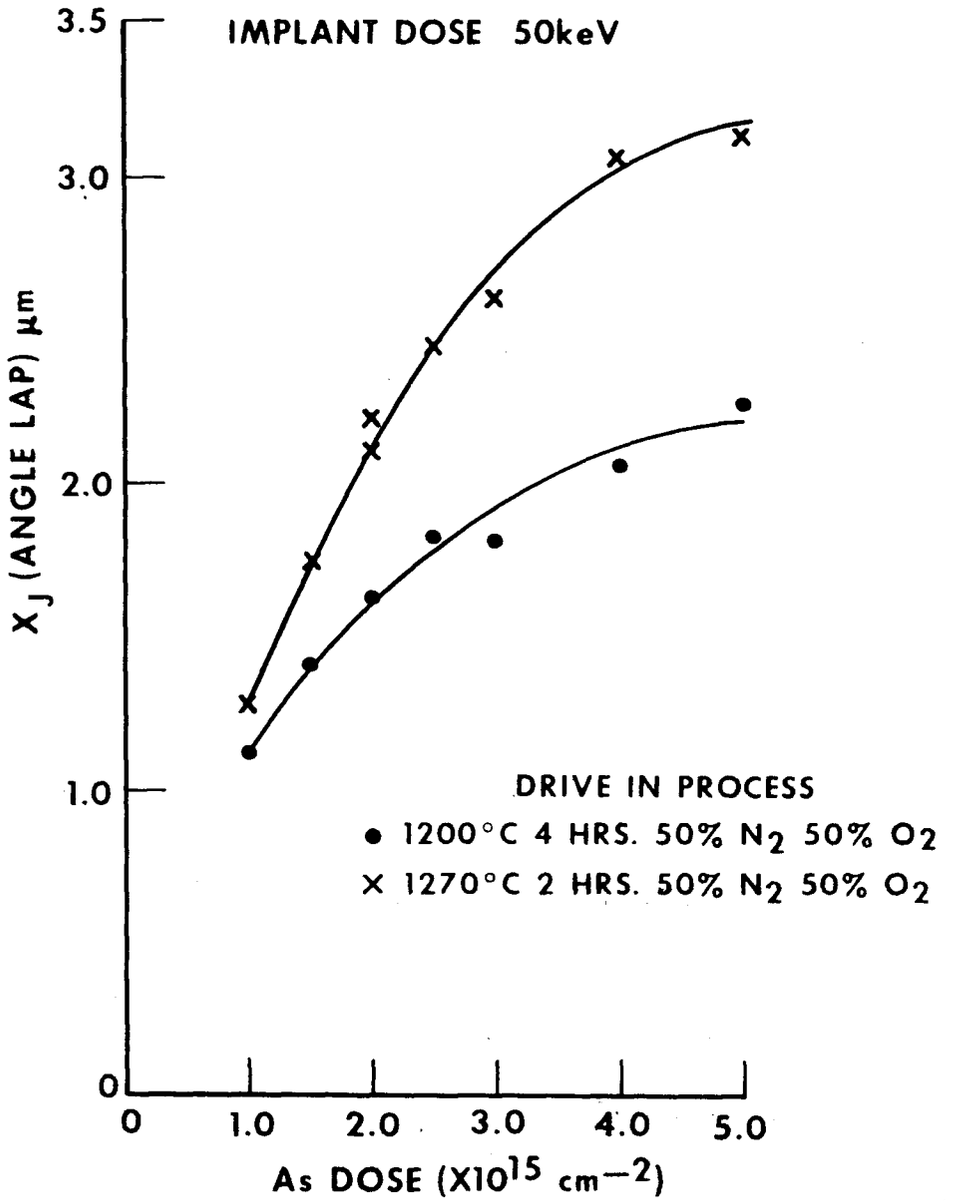


FIGURE 5

SURFACE CONCENTRATION (Cs) AS A FUNCTION OF ARSENIC DOSE (50 KeV) CALCULATED FROM GAUSSIAN PROFILE

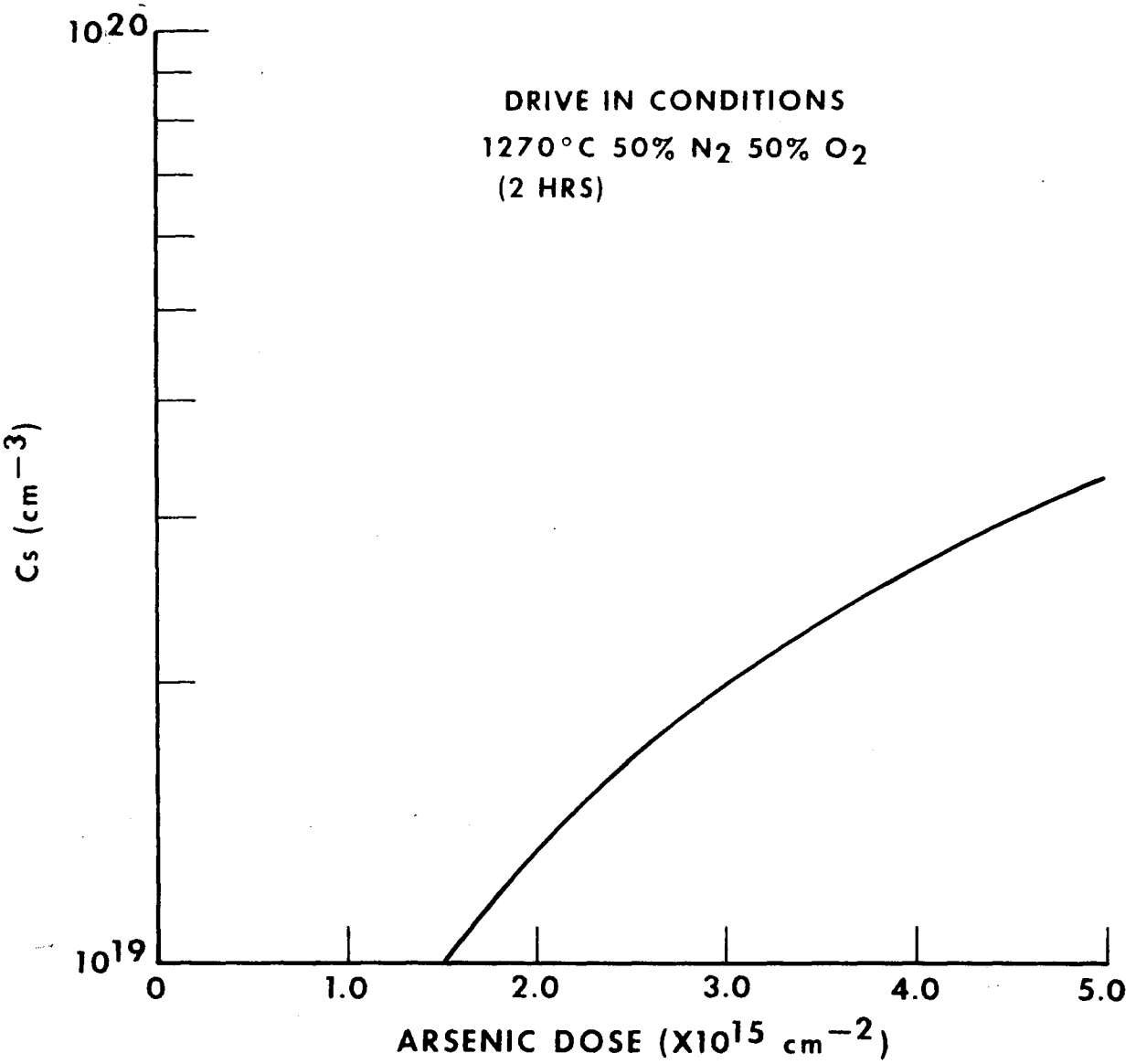


FIGURE 6

TOTAL ARSENIC CONCENTRATION (C) AS A FUNCTION OF DEPTH (X)

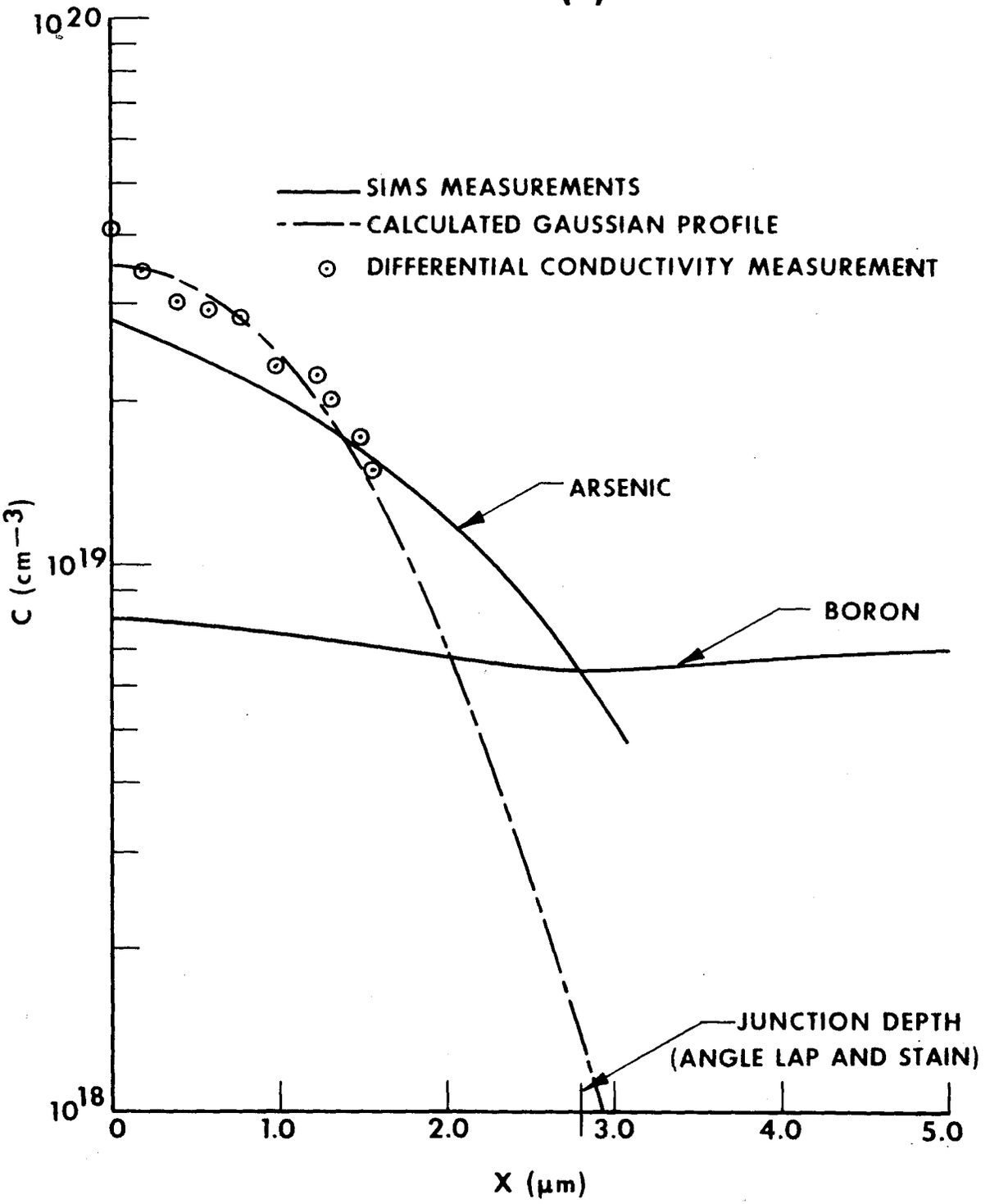


FIGURE 7

TYPICAL REVERSE BREAKDOWN CHARACTERISTIC

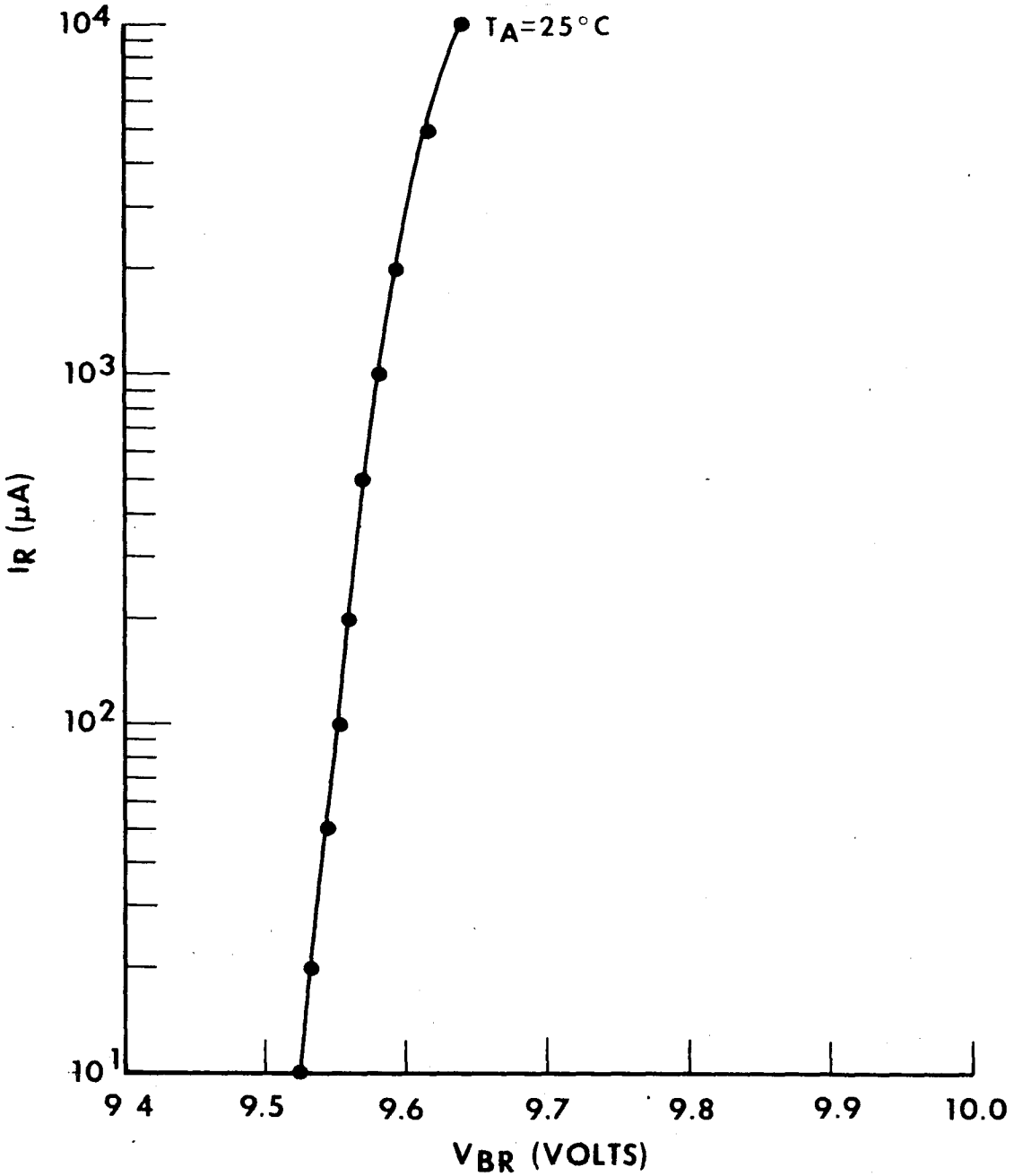


FIGURE 8

BREAKDOWN VOLTAGE AS A FUNCTION OF TEMPERATURE

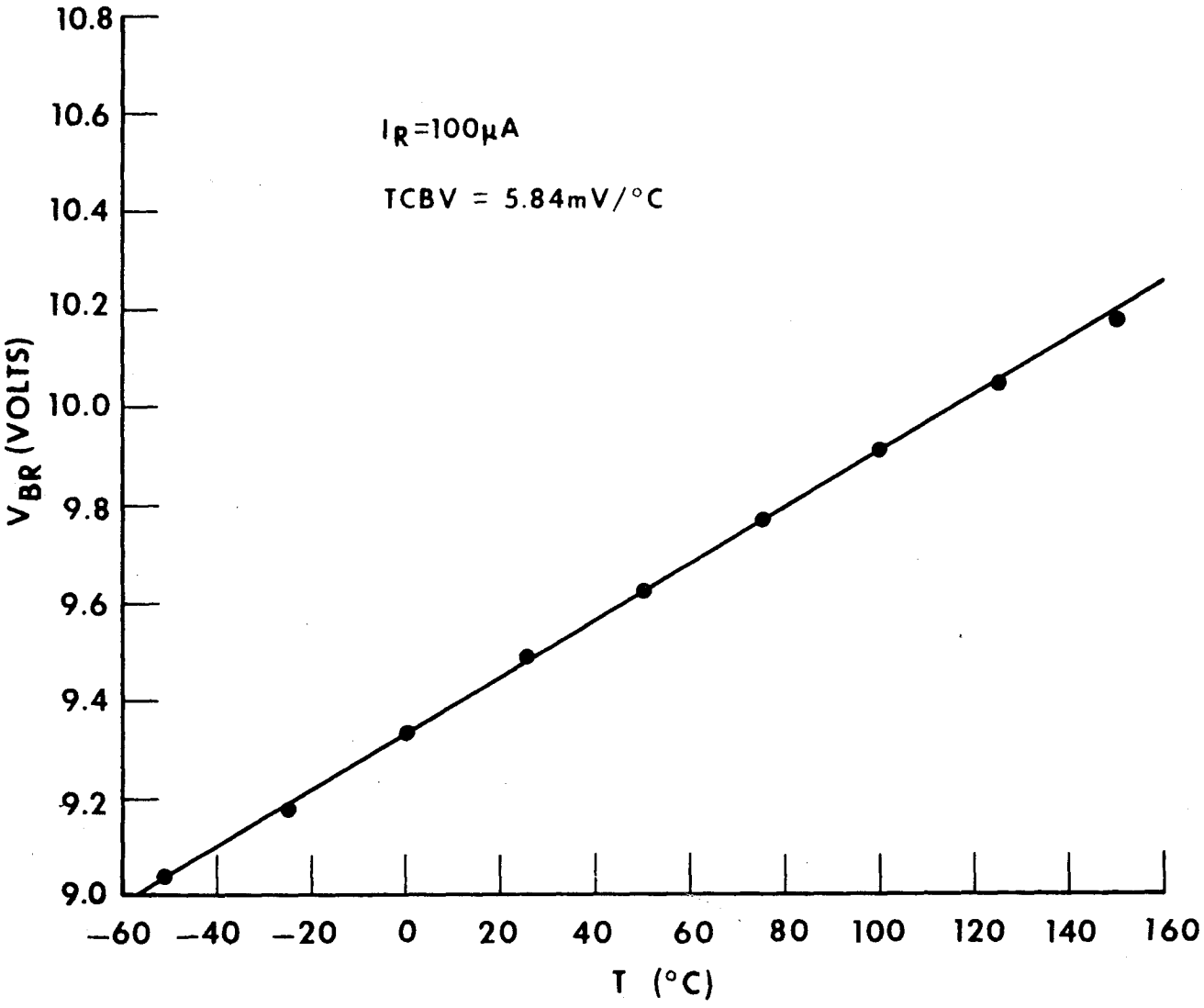


FIGURE 9

SATURATION CURRENT (I_S) AS A FUNCTION OF REVERSE VOLTAGE

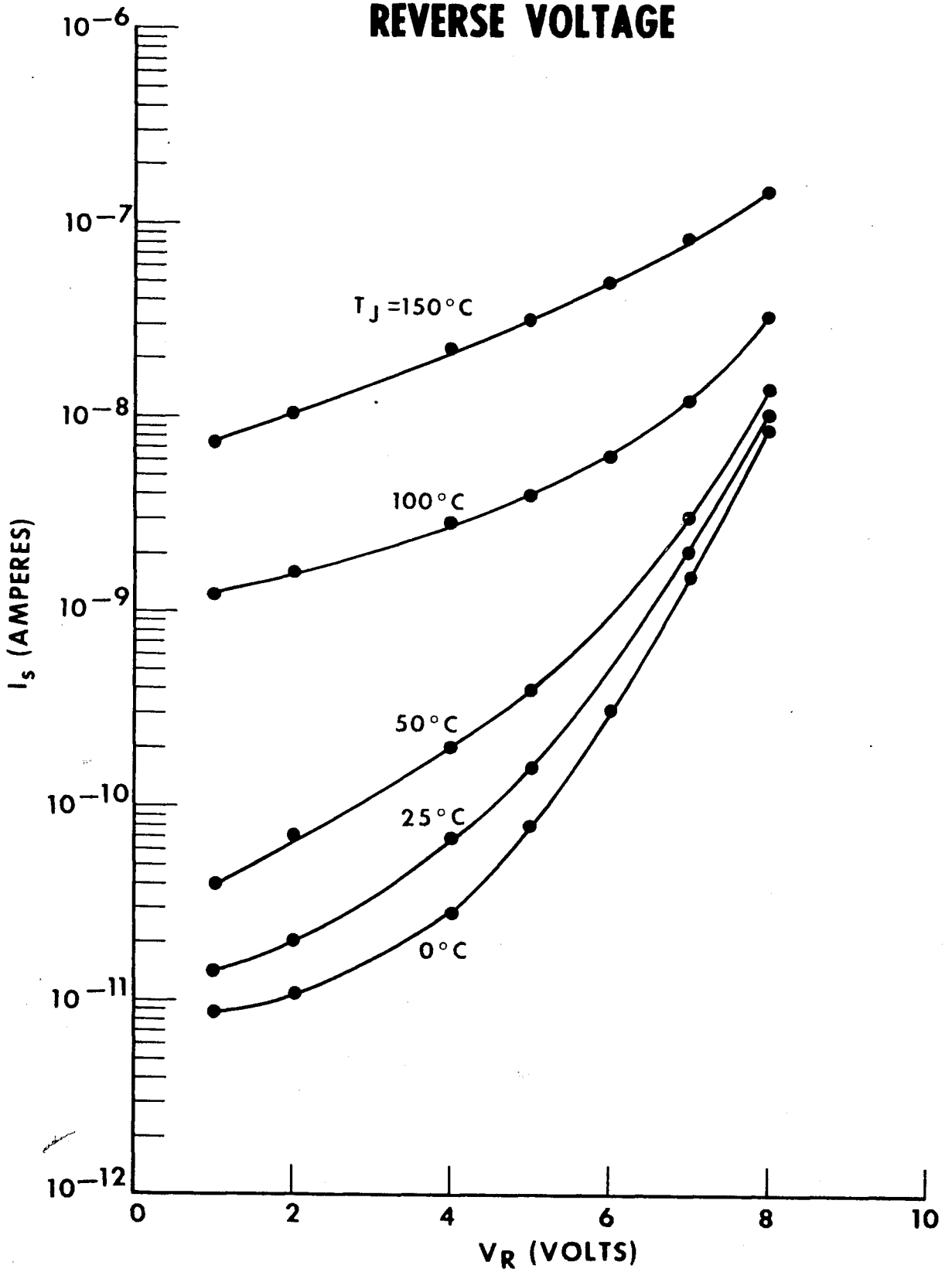


FIGURE 10

DYNAMIC BREAKDOWN IMPEDANCE AS A FUNCTION OF REVERSE BIAS CURRENT

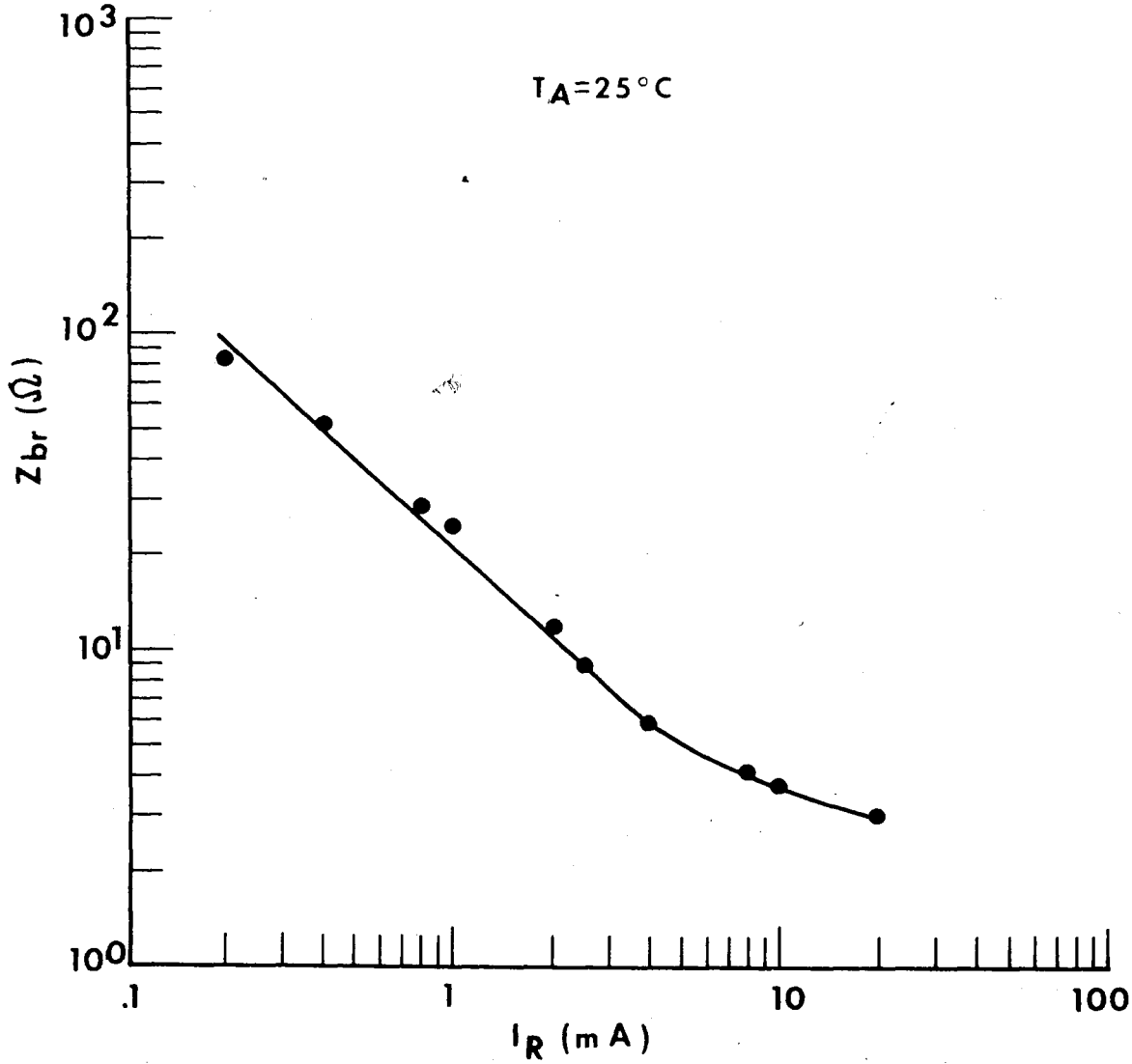


FIGURE 11

CAPACITANCE AS A FUNCTION OF REVERSE BIAS VOLTAGE

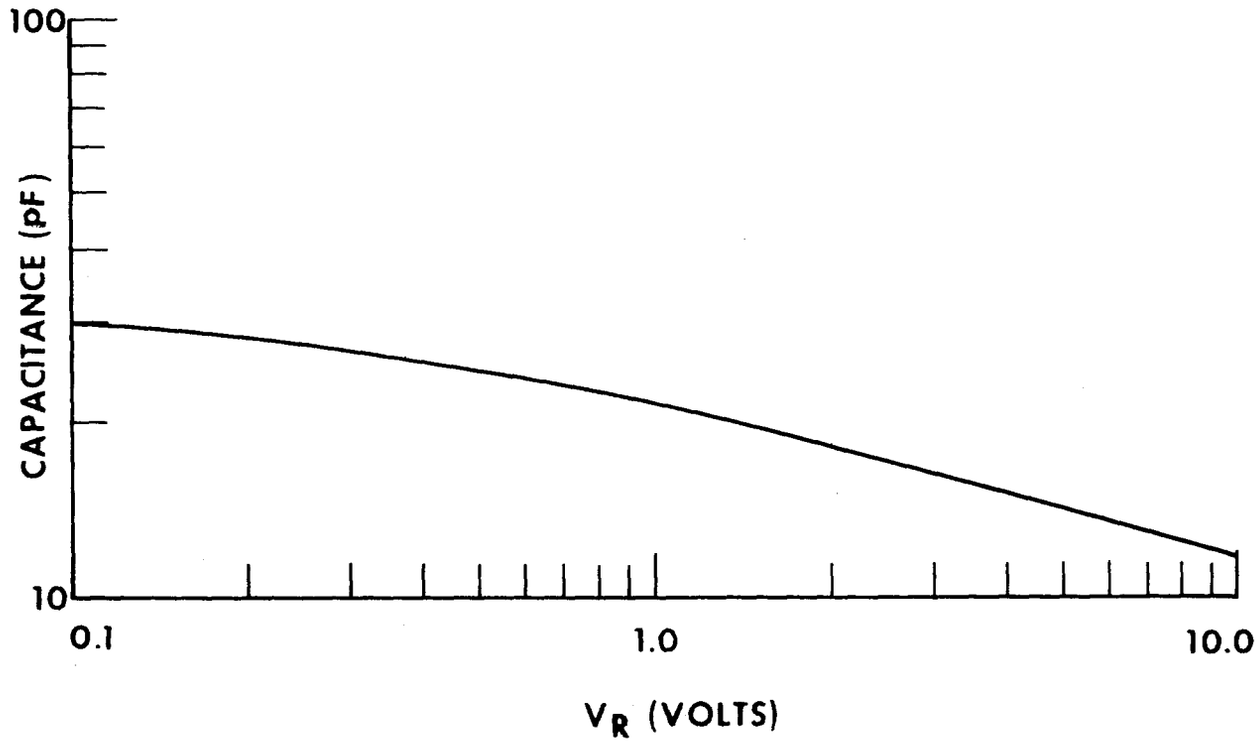


FIGURE 12

TYPICAL FORWARD CHARACTERISTIC

TC VF = 1.83 mV/°C (I_F=1mA)

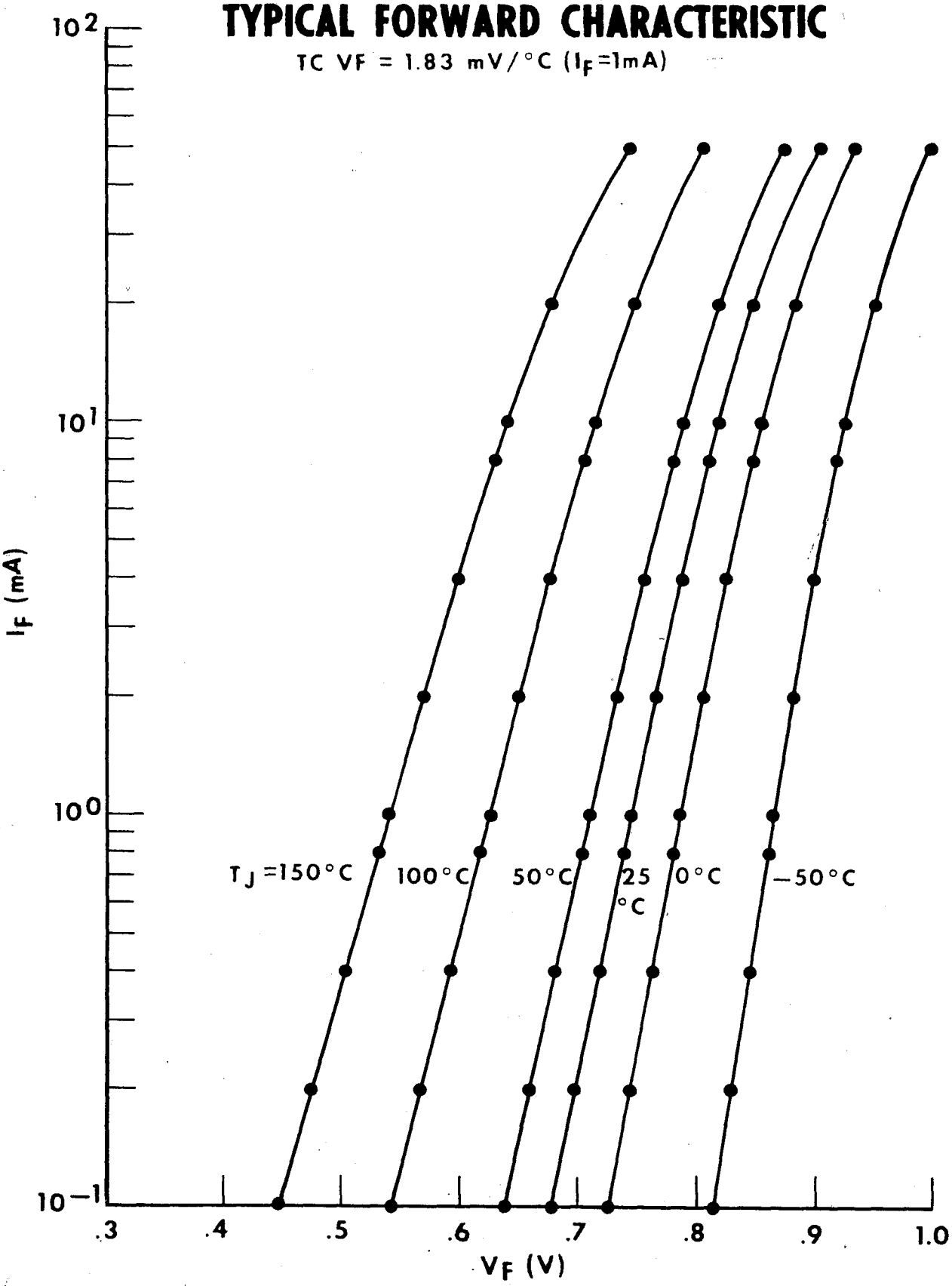


FIGURE 13

TYPICAL AVALANCHE NOISE uV/$\sqrt{BW}$ AS A FUNCTION OF REVERSE CURRENT (IR)

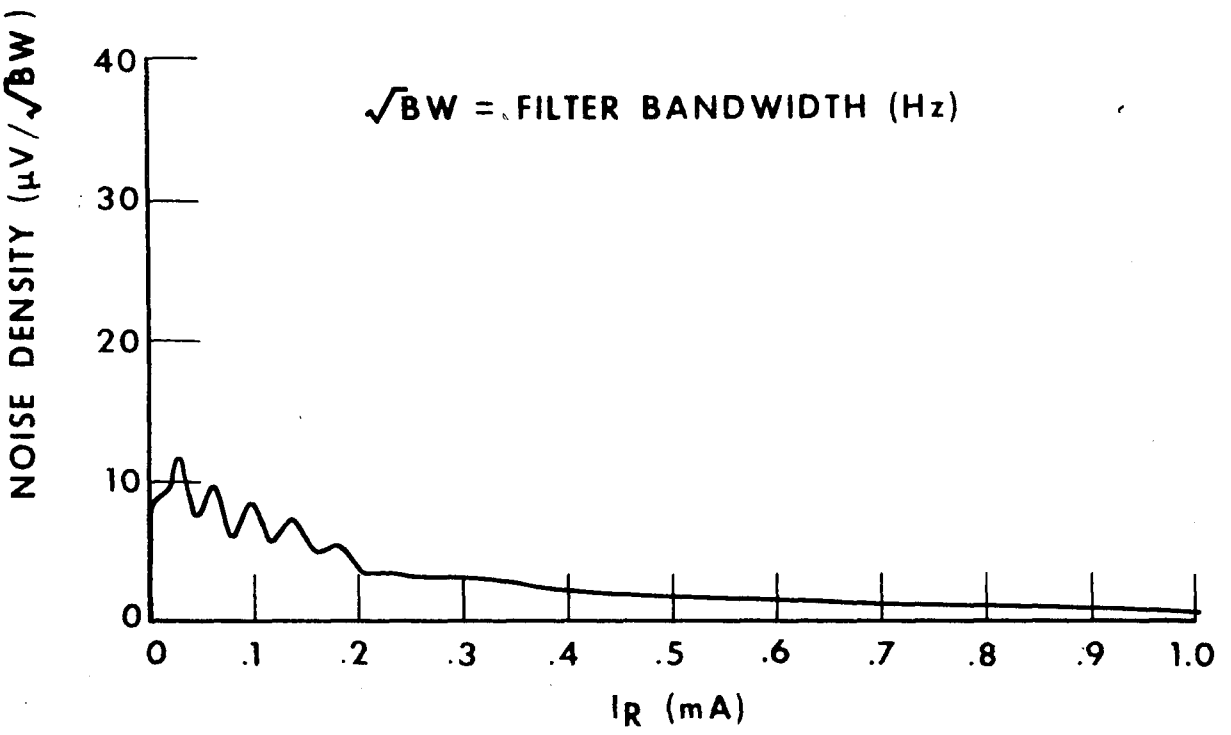


FIGURE 14

DISTRIBUTION OF BREAKDOWN VOLTAGE (V_{BR})

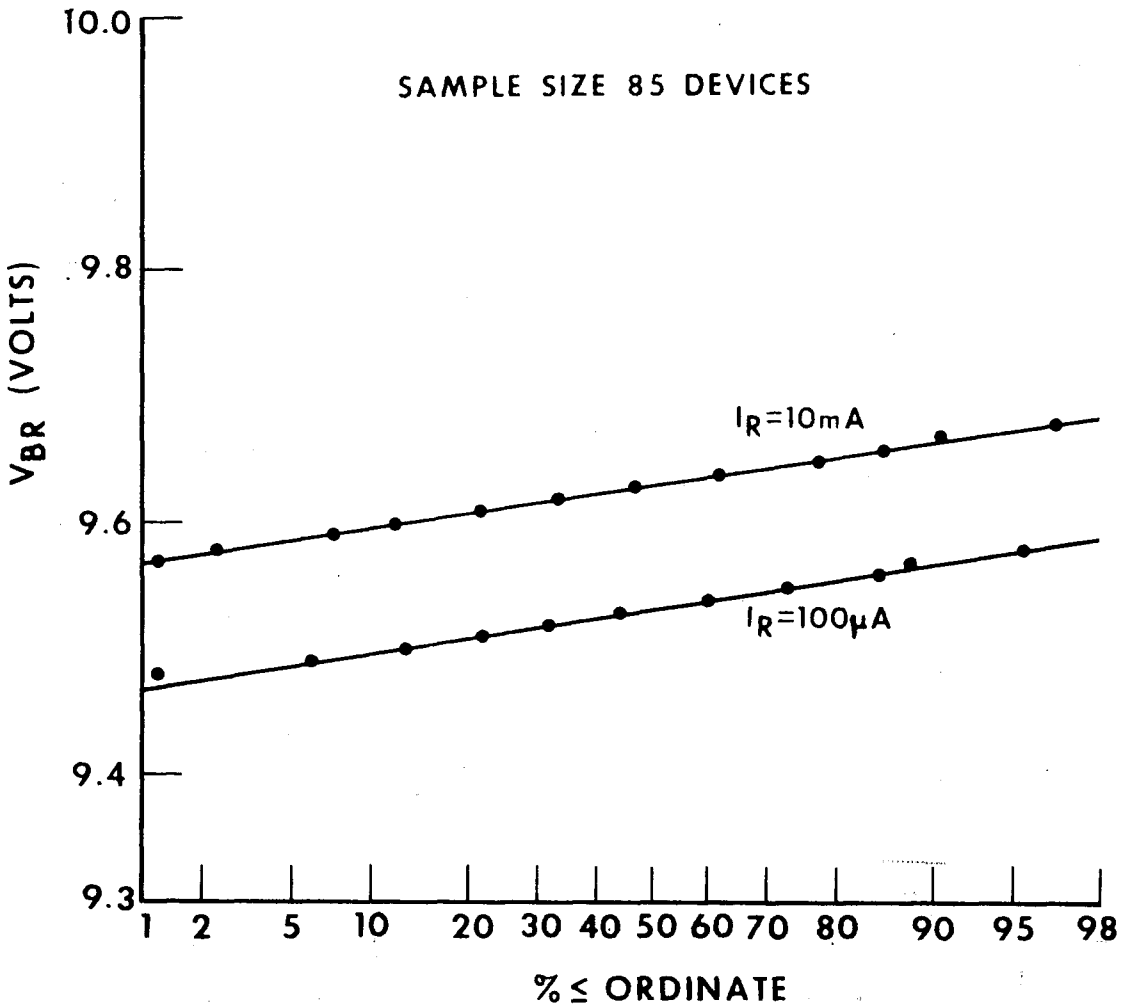


FIGURE 15

DISTRIBUTION OF SATURATION CURRENT (I_S)
V_R=4.0VDC

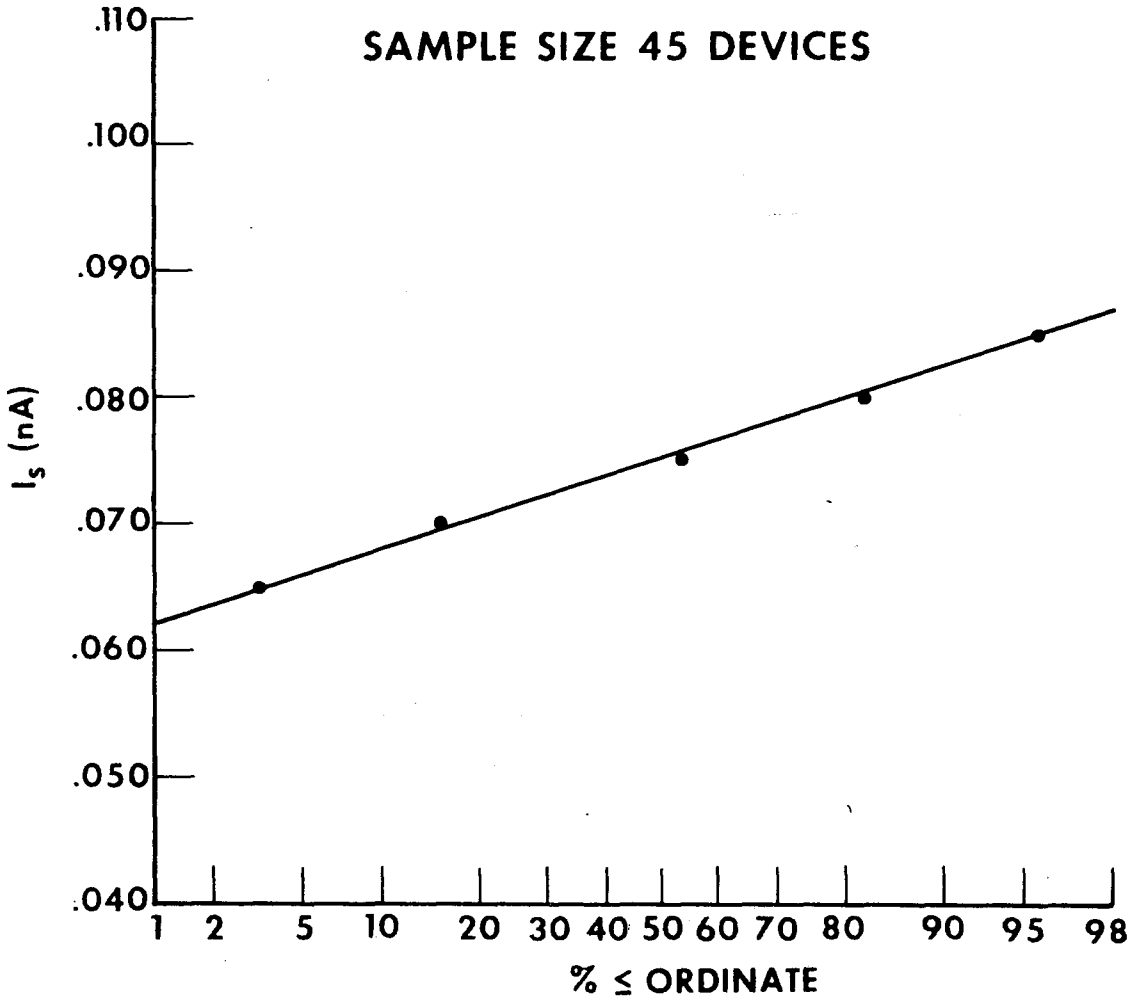


FIGURE 16

DISTRIBUTION OF FORWARD VOLTAGE (V_F)

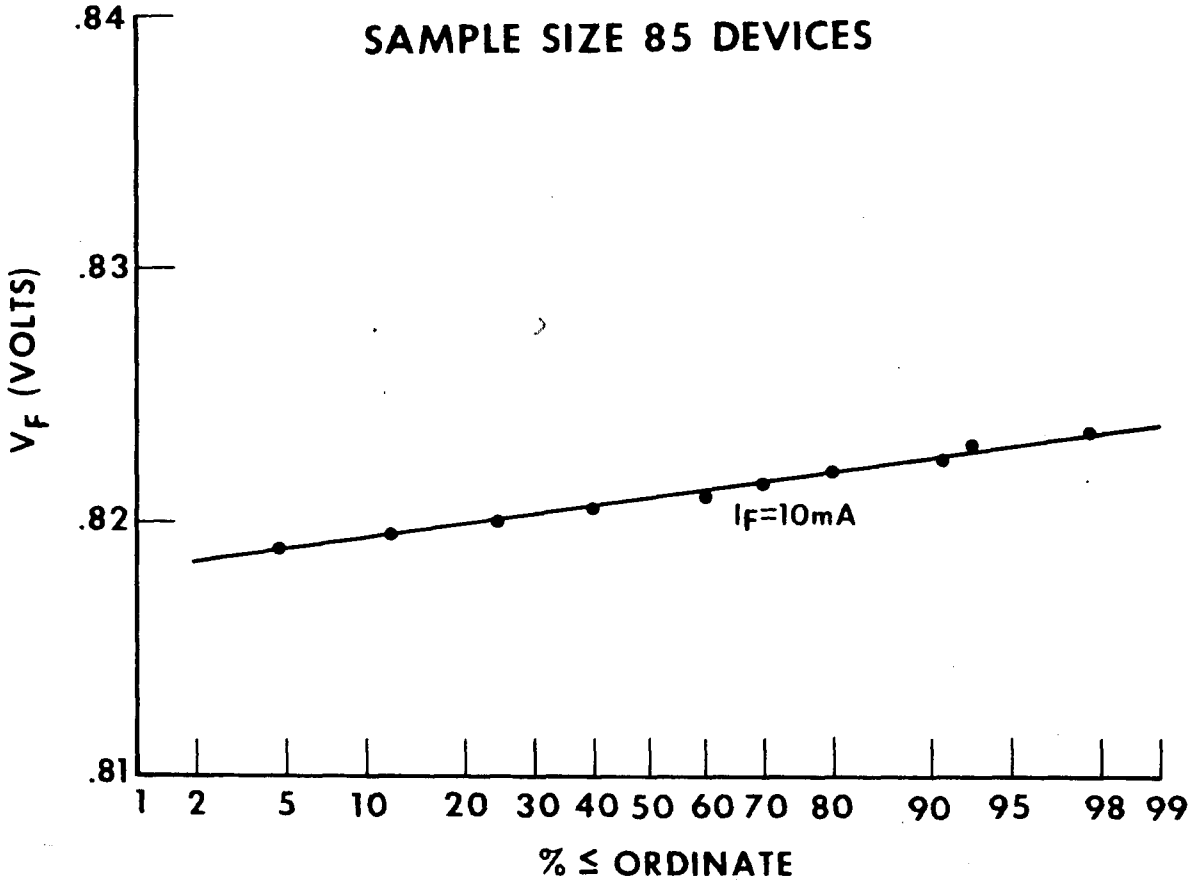


FIGURE 17

DISTRIBUTION OF BREAKDOWN IMPEDANCE (Z_{br})

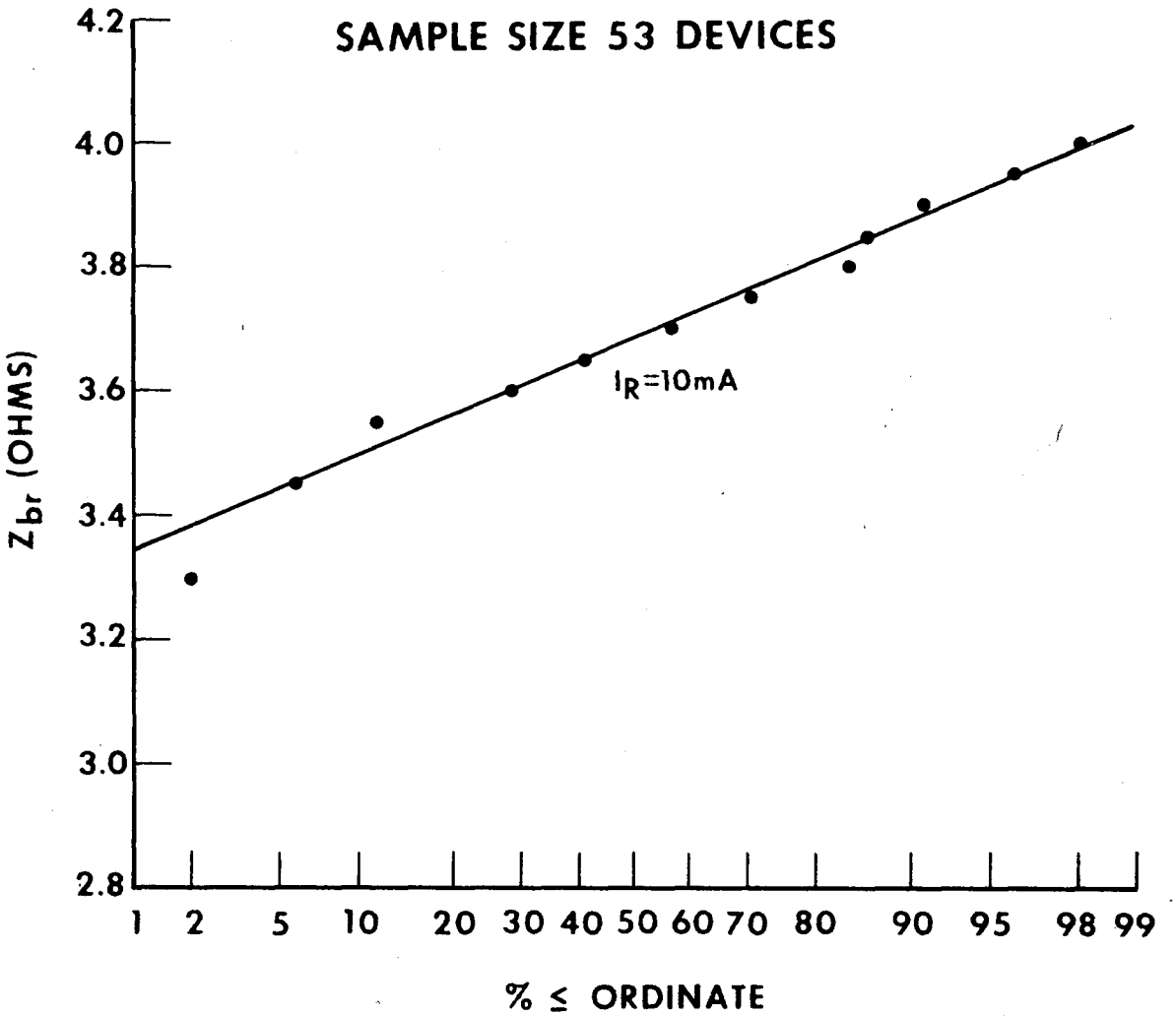


FIGURE 18

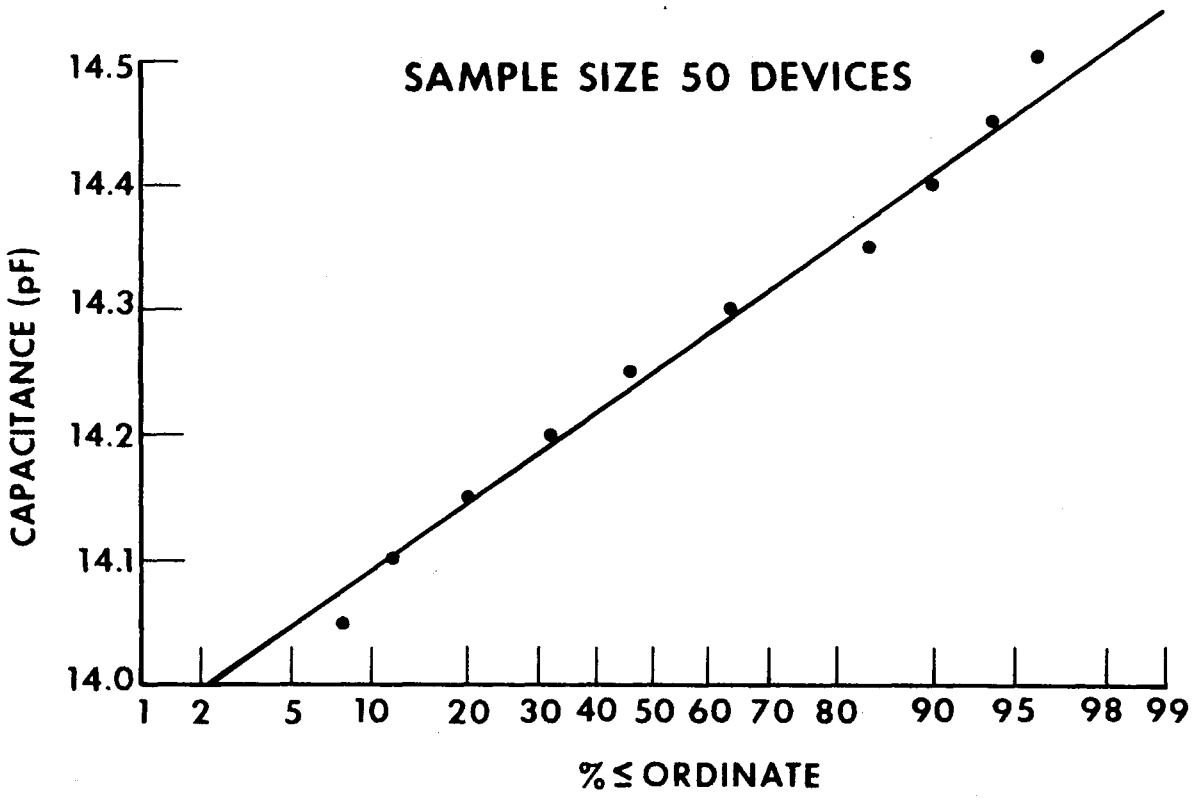

DISTRIBUTION OF CAPACITANCE VR=5V
SAMPLE SIZE 50 DEVICES
CAPACITANCE (pF)
14.5
14.4
14.3
14.2
14.1
14.0
1 2 5 10 20 30 40 50 60 70 80 90 95 98 99
% ≤ ORDINATE

FIGURE 19

LIFE REGRESSION CURVES OF STANDARD 8.2 VOLT PACKAGED REGULATOR DIODE

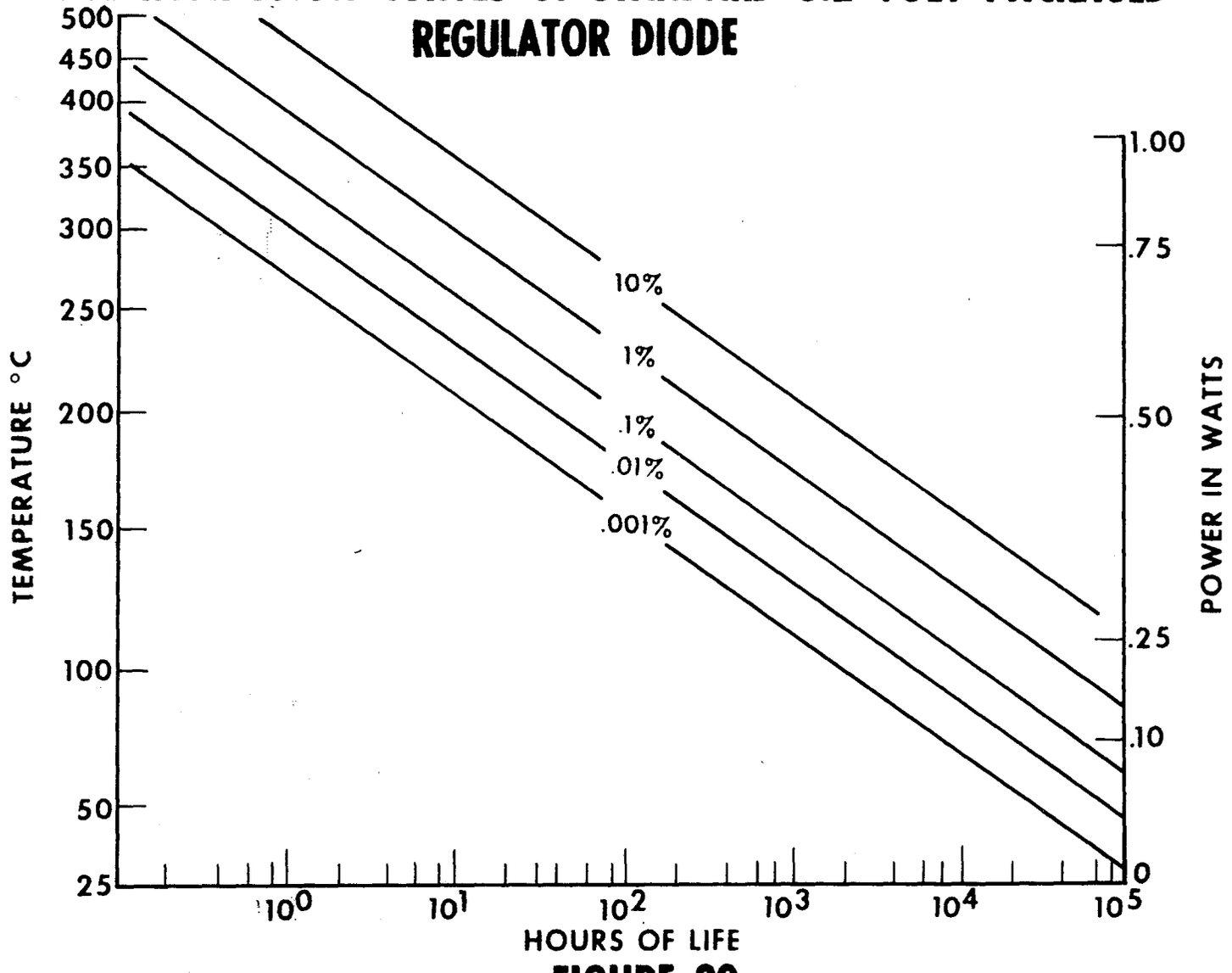


FIGURE 20

XIV. Vita

Mr. Frank M. Ogureck was born in Baltimore, Maryland on March 5, 1936, the son of Mr. and Mrs. Frank J. Ogureck. He graduated from Hazle Township High School, Hazleton, Pennsylvania in June, 1953. He received a Certificate in Electronics Technology from Penn State University Campus, Hazleton, Pennsylvania in June, 1959, and the Bachelor of Science Degree in Physics from Albright College in June, 1971. From 1959 to the present time he has worked at the Bell Telephone Laboratories, Reading, Pennsylvania and is presently an Associate Member of the Technical Staff. His work at the Laboratories has been concerned with a number of projects including the development of transistor devices for submarine cable, microwave transistors and multiple diodes. He is currently a member of the Semiconductor Technology Department where his main responsibility is the development of multiple diodes and beam-leaded voltage regulators. He and his wife, the former Dolores Schrenkel, and two children, Patricia Anne and Sean Robert, reside in Wyomissing, Pennsylvania.