1997

A study of thermal oxides on 6H-SIC for power device applications

Vickram R. Vathulya
Lehigh University

Follow this and additional works at: http://preserve.lehigh.edu/etd

Recommended Citation

This Thesis is brought to you for free and open access by Lehigh Preserve. It has been accepted for inclusion in Theses and Dissertations by an authorized administrator of Lehigh Preserve. For more information, please contact preserve@lehigh.edu.
Vathulya, Vickram R.

A Study of Thermal Oxides on 6H-SIC for Power Device Applications

June 1, 1997
A STUDY OF THERMAL OXIDES ON 6H-SIC FOR POWER DEVICE APPLICATIONS

by

Vickram R. Vathulya

A Thesis
Presented to the Graduate And Research Committee of Lehigh University in Candidacy for the Degree of Master of Science in Electrical Engineering

Lehigh University
May 07, 1997
This thesis is accepted and approved in partial fulfillment of the requirements for the Master of Science.

_April 24, 1997_  
(date)

Dr. Marvijn H. White  
Thesis Advisor

Dr. Alastair D. McAulay  
Chairman of Department
I would like to first of all thank and acknowledge my advisor, Dr. Marvin H. White, for allowing me to join his research group and provide invaluable support and guidance in my thesis work and graduate study at Lehigh University. I would like to thank William E. Wagner, Dr. Floyd C. Miller and Ray Filozof for their efforts in getting me oriented in the processing lab and their endless patience in answering processing related questions. The financial support of the Sherman Fairchild Foundation and the Office of Naval Research for this research project is highly appreciated.

I would like to thank Matthew G. Martin and Y. Larry Yang for many helpful discussions regarding my thesis work. The work of DongNing Wang in performing XPS studies on my SiC samples is greatly appreciated. I would also like to acknowledge useful discussions with Dr. Anant K. Agarwal, Dr. Richard R. Siergiej and Dr. Jeff B. Cassidy of the Northrop-Grumman Science and Technology Center in Pittsburgh. Mrs. Linda Dreisbach deserves special thanks for providing administrative assistance to the research group.

Finally, I would like to say that this thesis is dedicated to Madhu, Sumithra and my parents Anuradha and K. V. Ravikumar for their love and endless emotional support.
Contents

Acknowledgements iii

List of Tables vii

List of Figures viii

List of Symbols x

Abstract 1

1 Introduction 2
  1.1 Historical Review ........................................... 2
  1.2 Scope of this Thesis ......................................... 6

2 A Survey of SiC Power Devices 7
  2.1 Comparison of SiC and silicon Power Devices ............... 7
    2.1.1 Power MOSFETS ........................................... 7
    2.1.2 1D-Analysis of Drift Region of DMOSFET ................ 10
    2.1.3 Power IGBT ................................................ 11
  2.2 Comparison of DMOS and IGBT Devices ....................... 13
  2.3 The Importance of Gate Oxide Quality for Power Devices ..... 16

3 Theory of Thermal Oxidation 17
  3.1 The Deal and Grove Oxidation Model ......................... 17
    3.1.1 Net flux at the gas-oxide interface, $F_1$ ............ 18
    3.1.2 Net Flux in the Bulk of the Oxide, $F_2$ ............... 19
    3.1.3 Net Flux at the Oxide-Silicon Interface, $F_3$ .......... 19
  3.2 The Oxidation Rate Equation ................................. 20
  3.3 Extraction of Oxidation Parameters .......................... 21
3.4 Comparison of Experimental Results with the Theory ............... 22
3.5 Growth Kinetics of Thin Oxide Films in Dry Oxygen ............... 22
3.6 SiC oxidation ........................................ 24

4 Experiments ........................................ 25
4.1 Experiments on SiC oxidation .................................. 25
   4.1.1 A Modified Deal-Grove model ................................. 27
4.2 X-ray Photoelectron Spectroscopy Studies ......................... 30
   4.2.1 Basic Theory of XPS Analysis ............................. 30
   4.2.2 Experiments and Results ................................ 32
4.3 Capacitance Measurements ....................................... 35
   4.3.1 Accumulation Region .................................... 37
   4.3.2 Depletion Region ...................................... 37
   4.3.3 Inversion Region ...................................... 38
   4.3.4 Deep-Depletion ...................................... 38
4.4 Non-Ideal MOS Capacitors ....................................... 40
   4.4.1 The Gate to Semiconductor Work Function Difference ($\phi_{GS}$) 40
   4.4.2 Fixed Oxide Charge ($Q_f$) ................................ 41
   4.4.3 Interface Trapped Charge ($Q_{it}$) ......................... 41
4.5 MOS Device Characterization Techniques .......................... 42
4.6 High-Frequency C-V Technique .................................. 42
   4.6.1 Experimental Results .................................. 44
4.7 Electrical Breakdown Measurements ............................... 46
   4.7.1 Experimental Results .................................. 47

5 Conclusions ........................................ 49
5.1 Conclusions ........................................ 49
   5.1.1 6H-SiC Oxidation ...................................... 49
   5.1.2 Electrical Measurements ................................ 50
5.2 Recommendations ........................................ 50
References

Appendices

A SEMICAD: DEVICE SIMULATOR

A.1 Introduction to SEMICAD ................. 55
A.2 SEMICAD Installation .................. 55
A.3 Setting Up a SEMICAD Simulation ......... 56
   A.3.1 Specifying the Device ............... 56
   A.3.2 dmost.dev ......................... 57
   A.3.3 Specifying the Device Run File ........ 59
   A.3.4 dmosfet.run ....................... 60
A.4 Viewing of Simulation Results ........... 61
   A.4.1 FLEXVISION ....................... 61
   A.4.2 Doping, Potential and Current Density Profiles in the DMOS-FET .......... 62

B SiC Library File

B.1 SiC Library File for SEMICAD .......... 66
   B.1.1 SiC.lib ......................... 66

Vitae

vi
List of Tables

1.1 Comparison of important semiconductor properties for high-temperature electronics .................................................. 3

2.1 Comparison of design parameters for DMOSFET on silicon and 6H-SiC 10
## List of Figures

2.1 DMOSFET Structure ........................................... 8
2.2 Insulated Gate Bipolar Transistor Structure .................. 12
2.3 ON-state current density versus breakdown voltage at $V_F = 5V$ .... 14
2.4 ON-state current density versus breakdown voltage at $V_F = 6V$ .... 14
2.5 ON-state current density versus breakdown voltage at $V_F = 7V$ .... 15

3.1 Basic model for thermal oxidation of silicon ................. 18

4.1 Oxidation of 6H-SiC at 1150 °C .................................. 26
4.2 Theoretical fit to the oxidation curves of 6H-SiC at 1150°C .... 30
4.3 Basic Model for the XPS technique ............................ 31
4.4 Depth profile of the RCA cleaned p-type 6H-SiC sample .......... 32
4.5 Depth profile of the oxidized p-type 6H-SiC sample (argon carrier gas).
   The silicon:carbon ratio is 1:1 for this case and is an indication of
   excess carbon left behind in the SiC lattice. .................... 33
4.6 Depth profile of the oxidized p-type 6H-SiC sample (oxygen carrier gas).
   The removal of carbon from the SiC lattice by the excess oxygen
   is apparent in the ratio of silicon:carbon which is 3:1 ........ 33
4.7 Energy band diagram of the MOS structure to illustrate the concept
   of surface potential ............................................. 36
4.8 Ideal SiC CV curves for low and high frequencies ............. 39
4.9 High frequency CV curves for the argon carrier gas case .... 44
4.10 High frequency CV curves for the oxygen carrier gas case .... 45
4.11 Breakdown measurement on p-type capacitors ................. 47
4.12 Fowler-Nordheim plot of hole tunneling for an accumulated surface
   on p-type SiC MOS capacitors .................................. 48

A.1 DMOSFET Layout .............................................. 63
A.2 DMOSFET Potential Profile for $V_{ds} = 3$ Volts, $V_{gs} = 10$ Volts . . . . 64

A.3 DMOSFET Current Density Contours for $V_{ds} = 3$ Volts, $V_{gs} = 10$ Volts. The plot clearly shows the bottleneck effect of the JFET region and the subsequent current spreading towards the drain . . . . . . . . 65
List of Symbols

\[ R_{n^+} \] specific resistance of source (ohm-cm²)
\[ R_c \] specific resistance of channel (ohm-cm²)
\[ R_A \] specific resistance of accumulation layer (ohm-cm²)
\[ R_J \] specific resistance of JFET region (ohm-cm²)
\[ R_D \] specific resistance of drift region (ohm-cm²)
\[ R_S \] specific resistance of substrate (ohm-cm²)
\[ V_B \] Blocking Voltage (V)
\[ E_C \] Critical Electric Field for 6H-SiC (V/cm)
\[ h \] Planck's constant
\[ \hbar \] Reduced Plank's constant \( (\hbar/2\pi) \)
\[ m^* \] effective hole mass
\[ m_e \] rest electron mass
\[ n_i \] intrinsic density of electrons (cm⁻³)
\[ N_B \] Bulk concentration in drift layer (cm⁻³)
\[ \varepsilon_s \] dielectric permittivity of 6H-SiC (F/cm)
\[ W \] Thickness of the drift layer (cm)
\[ \mu_n \] electron bulk mobility in 6H-SiC (cm²/Vs)
\[ H \] Henry's constant
\[ C_s \] Concentration of oxidizing species at the gas-oxide interface (cm⁻³)
\[ C_i \] Concentration of oxidizing species at the semiconductor-oxide interface (cm⁻³)
\[ N_i \] number of oxidizing species to form a unit volume of oxide (cm⁻³)
\[ k_s \] surface reaction rate constant for oxidation (cm/s)
\[ k_b \] bulk reaction rate constant for oxidation (cm/s)
\[ D \] diffusion constant for the oxidizing species (cm²/s)
\[ L \] characteristic oxide thickness for oxidation model (cm)
$E_b$  electron binding energy (eV)
$q$  electron charge (1.602x10^{-19} C)
$t$  time (seconds)
$E_{ib}$  Intrinsic Fermi-energy level in the bulk (eV)
$E_c$  conduction band energy level (eV)
$E_g$  energy band gap for 6H-SiC (eV)
$E_v$  valence band energy level (eV)
$E_{is}$  Intrinsic Fermi-energy level at the surface (eV)
$E_{CP}$  Polysilicon Conduction Band Energy Level (eV)
$E_{FP}$  Polysilicon Fermi-level (eV)
$E_{VAC}$  Vacuum Energy level (eV)
$\chi_s$  semiconductor electron affinity (eV)
$\chi_P$  Polysilicon electron affinity (eV)
$\phi(x)$  potential in semiconductor (V)
$\phi_f$  fermi level in semiconductor (V)
$\phi_s$  surface potential in semiconductor (V)
$\phi_M$  Metal Work Function (eV)
$T$  temperature (K)
$k$  Boltzmann's constant (1.28x10^{-5} eV/deg K)
$X_o$  oxide thickness (cm)
$Q_{it}$  interface trap charge (C)
$C_{ox}$  oxide capacitance (F/cm²)
$D_{it}$  density of interface traps (cm^{-2}eV^{-1})
$Q_G$  charge on the Gate (C)
$Q_S$  semiconductor charge (C)
$V_{FB}$  flatband voltage (V)
$V_{GB}$  applied gate to substrate voltage (V)
$V_T$  threshold voltage for strong inversion (V)
$\epsilon_o$  permittivity of free space (8.85x10^{-19} F/cm)
$K_o$  oxide dielectric constant = 3.9
$\phi_b$  barrier height for hole tunneling through the oxide (V)

$E$  Electric field across the oxide (V/cm)
Abstract

Silicon Carbide (SiC) has become a subject of recent research due to its potential capability of creating high power and high frequency devices that operate at elevated temperatures. As the industry is driving towards power semiconductor devices, for which SiC is an excellent candidate, there is a necessity to provide thin high quality thermal gate oxides in these devices to limit threshold voltages to low values and provide oxide interfaces with low interface trap and oxide charge densities. Key applications such as the 'all electric car' and HDTV transmitters are part of the driving factors for companies to invest in SiC power semiconductor devices. Since these devices are expected to operate at high temperatures, the reliability of the gate dielectric is one of the most important concerns.

In this thesis, the effect of the carrier gas on the oxidation rates of 6H-Silicon Carbide in a wet oxidation process has been studied using oxygen and argon as the carrier gases. A modified Deal-Grove model has been developed to account for the increased oxidation rate in the initial thin oxide growth phase when oxygen is used as the carrier gas. X-Ray Photoelectron Spectroscopy has been used to study the dependence of the oxidation kinetics of 6H-SiC on the carrier gas. The XPS analyses strongly suggest a basic difference in the mechanism of oxidation when oxygen and argon are used as the carrier gases.

Electrical C-V and Breakdown measurements have also been carried out on MOS capacitors fabricated on these oxides with aluminum as the gate metal. The extracted fixed charge is found to be higher when argon is used as the carrier gas as compared to when oxygen is used. These oxides have breakdown fields of 8.5 MV/cm and also exhibit Fowler-Nordheim tunneling before catastrophic breakdown.
Chapter 1

Introduction

1.1 Historical Review

One of the thrust areas in the semiconductor industry is the search for semiconductor materials for power device applications. Silicon Carbide (SiC) is rapidly maturing to be a leading contender for these applications. The large SiC bonding energy makes SiC resistant to chemical attack and radiation, and ensures its stability at high temperatures. In addition, SiC has a large avalanche breakdown field, excellent thermal conductivity and a high electron saturation velocity all of which make it ideal for high power and high temperature operation.

SiC is the most prominent of a family of close packed materials that exhibit a one-dimensional polymorphism called polytypism. The SiC polytypes are differentiated by the stacking sequence of the tetrahedrally bonded Si-C bilayers, such that the individual bonding lengths and local atomic environments are identical, while the overall symmetry of the crystal is determined by the stacking periodicity. Each SiC bilayer, while maintaining the tetrahedral bonding scheme of the crystal, can be situated in one of three possible positions with respect to the lattice. Based upon these locations there exist three polytypes in SiC. They are the 6H, 4H and the 3C polytypes. The different polytypes have widely ranging physical properties. 3C SiC has the highest electron mobility and saturation velocity because of reduced phonon scattering resulting from a higher symmetry. The bandgaps differ widely among the polytypes ranging from 2.3 eV for 3C SiC to 3.0 eV in 6H SiC. Among these 6H is the most easily prepared and best studied, while the 3C and 4H are attracting more attention due to their superior electronic properties.
CHAPTER 1. INTRODUCTION

Table 1.1: Comparison of important semiconductor properties for high-temperature electronics.

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>GaAs</th>
<th>6H-SiC (3C SiC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap (eV) at 300K</td>
<td>1.12</td>
<td>1.4</td>
<td>3.0 (2.3)</td>
</tr>
<tr>
<td>Maximum operating temperature (K)</td>
<td>600</td>
<td>760</td>
<td>1580 (1200)</td>
</tr>
<tr>
<td>Physical stability</td>
<td>Good</td>
<td>Fair</td>
<td>Excellent</td>
</tr>
<tr>
<td>Electron mobility RT, cm²/Vs</td>
<td>1400</td>
<td>8500</td>
<td>600 (1000)</td>
</tr>
<tr>
<td>Hole Mobility RT, cm²/Vs</td>
<td>600</td>
<td>400</td>
<td>40</td>
</tr>
<tr>
<td>Breakdown Field (E_b), MV/cm</td>
<td>0.3</td>
<td>0.4</td>
<td>4</td>
</tr>
<tr>
<td>Thermal conductivity (c_T), W/cm</td>
<td>1.5</td>
<td>0.5</td>
<td>5</td>
</tr>
<tr>
<td>Saturation drift velocity (v_sat), 10⁷ cm/s</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Dielectric constant, k_e</td>
<td>11.8</td>
<td>12.8</td>
<td>9.7</td>
</tr>
<tr>
<td>Intrinsic carrier concentration, n_i (cm⁻³)</td>
<td>1.4x10¹⁰</td>
<td>1.8x10⁶</td>
<td>10⁻⁷</td>
</tr>
</tbody>
</table>

A comparison of important semiconductor properties has been summarised in Table 1.1. It can be clearly seen that SiC holds much more promise in the area of high power and high temperature electronics over Si and GaAs.

One major advantage that SiC enjoys over other wide band gap semiconductors is an established, commercialized process for the growth of high quality substrate material. The sublimation growth technique [1] is presently used by Cree Research for the growth of commercial substrates and by Northrop-Grumman for defense applications respectively, in the form of 1 and 1 3/16 inch diameter wafers. In sublimation growth, SiC is transported in the vapor phase to a SiC seed crystal held at a lower temperature. Typical growth parameters are 1800 °C for the seed crystal compared with a source temperature in the 2000 °C range. A thermal gradient of 20 K/cm across the growing crystal results in a growth rate of 0.7 mm/hr.

A fundamental obstacle in the development of wide bandgap semiconductor process technology has been finding suitable shallow dopants. Fortunately ambipolar doping in SiC was achieved very quickly allowing workers to focus more on device research. Nitrogen is the most popular n-type dopant, whereas, both Aluminum and
CHAPTER 1. INTRODUCTION

Boron are used as p-type dopants. Nitrogen acts as a donor level approximately 100 meV below the conduction band, whereas, Aluminum is an acceptor level at about 220 meV and Boron has two acceptor levels at 330 and 700 meV, respectively [2]. Since these levels are considerably deeper impurity levels compared to those in Silicon, an issue in devices fabricated on SiC is incomplete impurity ionization at room temperature. Another issue is the extreme difficulty in diffusing dopants into SiC. Thus, implantation is almost the sole way to introduce dopants for well and junction formations. A number of studies have been carried out on ion-implantation in SiC to make it a fairly well understood phenomenon [3, 4]. Ion-implantation at room temperature tends to amorphize the Silicon Carbide and also limits activation to very low values[3]. Hence, the implants are done at elevated temperatures around 700 °C and the subsequent anneal is also carried out at temperatures around 1600 °C.

A very important issue with the discovery of all semiconductor materials is the existence of a suitable passivating layer to provide interfaces with low fixed charge and interface trap densities. Another feature to set SiC apart from other wide bandgap compound semiconductors is the ability to form a stable silicon dioxide layer when thermally oxidized as in the case of silicon which opens up the fabrication of the entire range of oxide based devices. The large bandgap of SiC reduces the minority-carrier generation rate to the point that charge retention in an MOS device is effectively infinite, potentially removing the necessity of refreshing stored information which is the chief limitation on chip longevity in silicon based devices. So a similar technology based on SiC can be expected to have a much longer life expectancy and increased reliability.

The oxidation of SiC has been studied by many investigators. The general consensus is that oxidation begins at 900 °C at atmospheric pressure and proceeds via diffusion in a surface limited process[5, 6]. It has also been noted that the oxidation of SiC is in agreement with the Deal-Grove model established for silicon[7]. So far oxides grown on both p and n-type SiC exhibit interface trap densities in the mid $10^{11}$ to $10^{12}$ cm$^{-2}$ eV$^{-1}$[8, 9, 10]. Oxides on p-type SiC exhibit huge flatband shifts
as compared to those on n-type samples. The issue still remains as to whether this is due to an out diffusion of aluminum during the oxidation into the oxide or a large amount of C-O bonds at the surface or simply a result of the amphoteric nature of interface traps with acceptor traps in the top half and donor traps in the lower half of the bandgap. As with all wide band gap semiconductors, SiC has too few minority carriers at room temperature to allow equilibrium to be reached. Hence for C-V measurements, in order to sweep from accumulation to inversion in real time, the measurements should be taken at 300 °C or higher. Capitalizing on the large band gap of SiC, capacitance transients can be used to measure the bulk and surface generation rates. Devices having variable periphery to area ratios allow the surface and bulk components to be differentiated[11]. Thermally stimulated currents arising from interface traps can be used to determine the distribution of interface traps in the bandgap of SiC. Also, three terminal MOS structures provide us with more capabilities for studying device physics as compared to two terminal structures.

In recent years, there has been considerable interest in the fabrication of vertical power devices using SiC that can sustain very high forward blocking voltages in the OFF-state while delivering high current densities in the ON-state at very low voltage drops. Although these devices have been fabricated successfully, they suffer from very low electron mobility values in inversion layers on p-type SiC. So an important concern arises in the fabrication of power devices as to the need for thin high quality gate oxides with low concentrations of fixed oxide charge and interface trap densities in order to achieve small and controllable threshold voltages and high electron mobilities in the underlying inversion layer.
CHAPTER 1. INTRODUCTION

1.2 Scope of this Thesis

The purpose of this thesis is to investigate oxidation procedures on 6H-SiC to provide better quality gate dielectrics for use in power devices. In Chapter 2 a brief review of power devices is given. Simulation results of device performance are also given for the DMOS and IGBT devices on 6H-SiC. Chapter 3 provides the basic theory of Deal-Grove oxidation model and also reviews the theories given for thin oxide growth in silicon. The experiments on oxidation of 6H-SiC and subsequent XPS analysis and electrical measurements on the MOS structures fabricated is given in Chapter 4. Conclusions and a few recommendations for further work in this area are given in Chapter 5. A brief introduction to two-dimensional device simulation using the SEMICAD package is given in Appendix A and the materials parameter library for 6H-SiC is given in Appendix B.
Chapter 2

A Survey of SiC Power Devices

Power devices based upon silicon technology are approaching their theoretical limits of performance. Consequently, it will be necessary to develop devices from other materials in the future in order to reduce power losses in high frequency systems and to achieve high operating efficiencies. Out of a wide range of new materials, SiC seems to hold much promise due to its superior breakdown field strength, large saturated electron drift velocity and high thermal conductivity. Therefore it is extremely important to evaluate SiC as a candidate to replace silicon in high power and high temperature electronic applications. As discussed in the Introduction, SiC with its intrinsic advantages over silicon can help achieve integration of devices with higher packing densities thereby achieving improved current handling capabilities.

2.1 Comparison of SiC and silicon Power Devices

2.1.1 Power MOSFETS

Due to inherently high switching speeds power MOSFETS have several advantages over power bipolar devices for high frequency applications where switching power losses are dominant[12]. MOSFETS have a high input impedance which makes the gate drive circuitry very simple. Additionally, compared with power bipolar transistors they show an excellent safe operating area and better output characteristics suitable for operation of devices in parallel. These characteristics of power MOSFETS make them ideal candidates for high frequency applications like inverters and switched mode power supplies. However, these advantages are offset by the high
CHAPTER 2. A SURVEY OF SiC POWER DEVICES

specific on-resistance $R_{on,sp}$ associated with Si power MOSFETS for high breakdown voltages. Consequently, the use of Si power MOSFETS has been limited to breakdown voltages below 1000 V[13].

![Diagram of DMOSFET Structure]

**Figure 2.1: DMOSFET Structure**

Figure (2.1) shows a cross section of a power DMOS structure. The DMOS structure is fabricated by using planar diffusion technology with polysilicon gate electrodes. Since dopants diffuse extremely slowly into SiC they are ion-implanted and hence these power MOSFETS in SiC are sometimes called DIMOS (Double Implanted MOSFETS)[14]. In these devices the forward blocking capability is achieved by the p-n junction between the p-base region and the n-drift region. During device operation, a fixed potential is established for the p-base region by connecting it to the n+ source region. By connecting the gate to the source and applying a positive
voltage to the drain, the p-base/n-drift region becomes reverse biased and supports the applied drain voltage. Since the p-base is higher doped, most of the depletion layer to support this voltage would be in the n-drift layer. On applying a positive bias to the gate electrode, a conductive path extending between the n+-source region and the n-drift region is formed. The application of a positive drain voltage results in a current flow between drain and source through the n-drift region and the inversion layer. The conductivity of the channel is modulated by the gate bias voltage and the current flow is determined by the resistance of the various resistive components as shown in Figure (2.1).

The total $R_{on,sp}$ is determined as

$$R_{on,sp} = R_{n+} + R_C + R_A + R_J + R_D + R_S \quad (2.1)$$

where $R_{n+}$ is the contribution from the n+-source, $R_C$ is the channel resistance, $R_A$ is the accumulation layer resistance, $R_J$ is the resistance of the drift region between the p-base regions, which resembles a JFET region, $R_D$ is the resistance of the remaining drift region and $R_S$ is the substrate resistance.

In a power MOSFET, since the blocking voltage is mainly supported across the drift layer, the drift region resistance is considered to be the minimum possible theoretical limit for the on-resistance of a MOSFET. For an ideal DMOSFET, all resistances, other than the resistance of the drift region, are negligible and the specific on-resistance is determined by the drift region resistance only at high blocking voltages. Figure (2.1) shows, for a given gate bias, as the blocking voltage capability is increased, the specific on-resistance also increases and therefore the current density for a given on-voltage drops. At low blocking voltages other resistances also influence the specific on-resistance. It is also important to note, irrespective of the blocking voltage capability, as the cell pitch becomes smaller the JFET resistance is the dominating resistance governing the device operation.
CHAPTER 2. A SURVEY OF SiC POWER DEVICES

2.1.2 1D-Analysis of Drift Region of DMOSFET

This analysis can be performed by assuming uniform doping in the drift \( (N_B) \) and base regions. Assuming a triangular one-sided field distribution at forward blocking voltage \( (V_B) \) we can write the following:

\[
V_B = \frac{1}{2} E_C W \tag{2.2}
\]

\[
E_C = qN_B W / \varepsilon_s \tag{2.3}
\]

where \( W \) is the width of the drift region, \( E_C \) the critical breakdown field and \( \varepsilon_s \) the dielectric constant of the semiconductor. From equations (2.2) and (2.3) we can derive expressions for the doping density of the drift region and the specific on-resistance for the DMOSFET.

\[
N_B = \varepsilon_s E_C^2 / (2qV_B) \tag{2.4}
\]

\[
R_{on,sp} = W / qN_B \mu_n = 4V_B^2 / (\varepsilon_s E_C^3 \mu_n) \tag{2.5}
\]

where \( \mu_n \) is the electron mobility. It is essential to compare the design parameters for given device specifications for both the silicon and the 6H-SiC materials to see where the advantages of using 6H-SiC lie. If we assume best case mobilities for both silicon and 6H-SiC (1400 cm\(^2\)/Vs and 400 cm\(^2\)/Vs, respectively) and use published values of the breakdown field \( E_C \) for silicon and 6H-SiC (0.3 MV/cm and 4 MV/cm, respectively), then the design parameters of the drift layer for a 5000V DMOSFET to first order are shown in Table 2.1.

<table>
<thead>
<tr>
<th>Material</th>
<th>Concentration (cm(^{-3}))</th>
<th>Thickness ((\mu m))</th>
<th>( R_{on,sp} ) (ohm-cm(^2))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>( 5.9 \times 10^{13} )</td>
<td>330</td>
<td>2.5</td>
</tr>
<tr>
<td>6H-SiC</td>
<td>( 8.6 \times 10^{15} )</td>
<td>25</td>
<td>( 4.6 \times 10^{-3} )</td>
</tr>
</tbody>
</table>

Table 2.1: Comparison of design parameters for DMOSFET on silicon and 6H-SiC

We see the drift layer thickness is much higher for silicon and the specific on-resistance of the silicon DMOSFET is about 550 times that of the 6H-SiC DMOSFET. Combined with the ability to dissipate heat more effectively than silicon,
CHAPTER 2. A SURVEY OF SiC POWER DEVICES

6H-SiC holds much promise in the field of high power electronics over silicon in terms of higher operating temperatures and packing densities in ICs.

2.1.3 Power IGBT

The power MOSFET is a voltage controlled device with high input impedance that makes the gate circuitry simple. Also, the on-resistance of power MOSFETS is very small when designed to block low voltages. These features have led to the replacements of power bipolar transistors by power MOSFETS. However, the on-resistance of power MOSFETS increases rapidly when its breakdown voltage is increased. This makes the on-state power losses unacceptable for applications where high DC supply voltages are used.

Since bipolar conduction allows operation at high on-state current densities with a low on-state voltage drop and MOS gate structures provide ease of gate control, it is advantageous to develop devices where bipolar current transport is controlled via an MOS gate structure. Among these devices, the insulated gate bipolar transistor (IGBT) has become commercially successful due to its superior on-state characteristics, reasonable switching speeds and excellent safe-operating area. It is also the ideal device for applications that need very high blocking voltages. The IGBT is shown in Figure (2.2) along with the I-V characteristics for varying drift layer thicknesses. When a positive voltage is applied to the collector with the gate and emitter at ground potential, the upper junction (J2) becomes reverse biased and the device operates in its forward blocking mode just as in the case of the DMOSFET. If a positive gate bias is applied with sufficient magnitude to invert the surface of the p-base region under the gate, then the device is switched into its ON-state. In the ON-state, electrons flowing from the n+-emitter to the n-drift region via the inversion layer form the base drive current for the vertical PNP transistor in the IGBT structure. Since the emitter junction (J1) for this transistor is forward biased, the p+ region injects holes into the base region. As the collector bias is increased, the
CHAPTER 2. A SURVEY OF SiC POWER DEVICES

injected hole concentration increases until it exceeds the background doping concentration in the drift layer. In this regime, therefore, the I-V characteristics of the IGBT resemble that of a PiN diode. So this device can be operated at high on-state current densities even when designed to support high breakdown voltages.

Figure 2.2: Insulated Gate Bipolar Transistor Structure

In commercial IGBT devices, an n+ buffer layer is utilised to improve on-state characteristics at the cost of losing reverse blocking capability. It can be seen that by using an n+ buffer layer, we can design IGBT devices for a particular forward blocking voltage by using a thinner drift layer and thereby improving the specific on-resistance of the device. From the mode of operation of the IGBT, we observe the I-V characteristics of the IGBT will exhibit a knee voltage equal to the built-in voltage of the p⁺-n diode. For silicon this voltage is around 0.6 volts whereas for
CHAPTER 2. A SURVEY OF SiC POWER DEVICES

6H-SiC it is around 2.8 volts. Therefore, for low forward blocking voltages and room temperature operation silicon is the preferred semiconductor to build IGBT devices and if very high blocking voltages and operating temperatures are used then 6H-SiC needs to be used.

2.2 Comparison of DMOS and IGBT Devices

From the discussion in the previous section, we observe the specific on-resistance of power devices in silicon becomes intolerably high as the blocking voltage capability of the devices are increased. Hence, power devices capable of handling blocking voltages in excess of 400 Volts have to be fabricated on 6H-SiC. At this point there are a variety of power devices that can be fabricated and it becomes essential to figure out the trade-offs involved in choosing any particular device. Of particular interest is the comparison between the DMOS (a minority carrier device with inherently high switching speeds) and the IGBT (a bipolar device with a MOS gate that supplies the base current drive via the inversion layer beneath the electrode, thereby, combining the aspects of both the bipolar and MOS devices).

In this thesis two dimensional device simulations have been carried out on DMOS and IGBT structures, using the SEMICAD software from DAWN Technologies Inc., where the drift layer thickness has been varied and the on-state current density ($J_F$) plotted as a function of the breakdown voltage ($V_{BD}$) that the structure supports for different on-state voltage drops ($V_F$).
CHAPTER 2. A SURVEY OF SIC POWER DEVICES

Figure 2.3: ON-state current density versus breakdown voltage at $V_F = 5V$

Figure 2.4: ON-state current density versus breakdown voltage at $V_F = 6V$
CHAPTER 2. A SURVEY OF SiC POWER DEVICES

Figure 2.5: ON-state current density versus breakdown voltage at \( V_F = 7V \)

From these figures, we see for room temperature operation at forward voltages less than 7 Volts using 6H-SiC material, the DMOS device is capable of supplying higher on-state current densities for higher breakdown voltages than the IGBT device. So the DMOS is the more appropriate power device for operating at room temperature with very low ON-state voltage drops and power consumption while being capable of supporting high forward blocking voltages when not in the conduction mode.

However, it is worth mentioning, that as the operation temperature is increased, minority carrier injection into the drift layer is substantially increased in the IGBT and the threshold voltage is lowered. This leads to much higher current densities in the IGBT for the same forward voltage drop as compared to the DMOS structure. So if high temperature operation is necessary, the IGBT becomes the device of choice.
2.3 The Importance of Gate Oxide Quality for Power Devices

Regardless of the power device selected, one of the most important concerns in the fabrication procedure is the need to provide high quality gate oxides for these devices. An important driving force behind high quality gate oxides is to obtain high oxide breakdown voltages and minimal trapping effects due to charge injection into the oxide at elevated temperatures. In order to optimize the power device performance, the gate oxide quality has to be improved as it governs the ultimate performance limits of the power device regardless of the semiconductor used. Hence, it becomes essential to develop well-controlled oxidation recipes to provide thin gate oxides with very low densities of fixed oxide charge (less than $2 \times 10^{11} \text{cm}^{-2}$) and interface trap densities (less than $10^{11} \text{cm}^{-2}\text{eV}^{-1}$). Thin oxides help achieve lower threshold voltages which are directly related to the supply voltages used. New oxidation techniques to grow good quality thin oxides are described in the next section and a modified Deal-Grove oxidation model is developed for thin oxide growth on 6H-SiC.
Chapter 3

Theory of Thermal Oxidation

The oxidation of silicon is necessary during the entire process of fabricating modern integrated circuits. The production of high quality ICs requires not only an understanding of the basic oxidation mechanism, but the ability to form, in a controlled and repeatable manner, a high quality oxide. In addition, to ensure the reliability of the ICs, the electrical properties of the oxide must be understood. Thermal oxidation is the preferred technique to grow oxide layers when the interface between oxide and the semiconductor is required to have a low charge density level. In the following section the basic oxidation mechanism by Deal and Grove for silicon is discussed.

3.1 The Deal and Grove Oxidation Model

Deal and Grove made the basic hypothesis that the oxidizing species (O$_2$ or H$_2$O) are dissolved in silica in interstitial positions and migrate to the Si-SiO$_2$ interface during thermal growth, even if they react with the silica network[7]. With this hypothesis they were able to derive growth kinetics equations that are widely used today. The theory of Deal and Grove agrees well with the experimental results found for dry oxidation, for oxides thicker than 400 Å, and with the experimental results of wet oxidation for all oxide thicknesses.

Figure (3.1) shows the silicon substrate covered by an oxide layer in contact with the gas phase. The basic oxidation mechanism can be broken up into three stages. The oxidizing species are transported from the gas phase to the gas-oxide interface with flux F1, are transported across the existing oxide toward the silicon with flux F2, and react at the Si-SiO$_2$ interface with the silicon with flux F3.
Figure 3.1: Basic model for thermal oxidation of silicon

At steady state, all three fluxes are equal,

\[ F_1 = F_2 = F_3 = F \]  \hspace{1cm} (3.1)

3.1.1 Net flux at the gas-oxide interface, \( F_1 \)

The gas phase flux, \( F_1 \), can be expressed as

\[ F_1 = J_E - J_S \]  \hspace{1cm} (3.2)

where \( J_E \) and \( J_S \) are the in-going and out-going fluxes, respectively. If \( C_S \) is the concentration of the oxidizing species in the oxide beneath the gas/oxide interface and if we assume a first order proportionality (given by \( H \), Henry’s constant) between surface concentration \( C_S \) and the out-going flux, then we can write,

\[ J_S = HC_S \]  \hspace{1cm} (3.3)
CHAPTER 3. THEORY OF THERMAL OXIDATION

and when oxidation stops, \( F_1 = 0 \) and \( C_S = C^* \). \( C^* \) is the solubility limit of the species in the oxide. The equilibrium conditions \( F_1 = 0 \) and \( C_S = C^* \) introduced in Equation (3.2) and (3.3) lead to,

\[
F_1 = H(C^* - C_S) \quad (3.4)
\]

3.1.2 Net Flux in the Bulk of the Oxide, \( F_2 \)

Since transport in the oxide bulk occurs by diffusion we invoke Fick's law,

\[
F_2 = -D \frac{dC}{dX} \quad (3.5)
\]

In the Deal and Grove model the concentration gradient is assumed to be a constant. Thus \( F_2 \) can be written as,

\[
F_2 = D \frac{(C_S - C_i)}{X_o} \quad (3.6)
\]

where \( D \) is the diffusion coefficient, \( X_o \) is the oxide thickness and \( C_i \) is the concentration of the oxidizing species at the SiO\(_2\)-Si interface.

3.1.3 Net Flux at the Oxide-Silicon Interface, \( F_3 \)

Assuming a first order reaction (e.g. \( \text{Si} + \text{O}_2 \rightarrow \text{SiO}_2 \)) we can write,

\[
F_3 = k_s C_i \quad (3.7)
\]

where \( k_s \) is the reaction rate constant. Using equations (3.4), (3.6), (3.7) and (3.1), we obtain in the steady state,

\[
H(C^* - C_S) = D \frac{C_S - C_i}{X_o} = k_s C_i \quad (3.8)
\]

Equation (3.8) can be solved for the equilibrium concentrations in the oxide at the Si-SiO\(_2\) interface \( (C_i) \) and at the outer surface \( (C_S) \),

\[
C_i = \frac{C^*}{\left(1 + \frac{k_s}{H} + \frac{k_s X_o}{D}\right)} \quad (3.9)
\]
CHAPTER 3. THEORY OF THERMAL OXIDATION

\[ G_s = \frac{(1 + k_s X_o) C^*}{D} \left(1 + \frac{k_s}{H} + \frac{k_s X_o}{D}\right) \]  

(3.10)

From equations (3.1), (3.8), (3.9) and (3.10) we obtain,

\[ F = \frac{k_s C^*}{(1 + \frac{k_s}{H} + \frac{k_s X_o}{D})} = \frac{C^*}{\left(\frac{1}{k_s} + \frac{1}{H} + \frac{X_o}{D}\right)} \]  

(3.11)

and with \( \frac{1}{k_e} = \frac{1}{k_s} + \frac{1}{H} \) in equation (3.11) we have,

\[ F = \frac{C^*}{\left(\frac{1}{k_e} + \frac{X_o}{D}\right)} \]  

(3.12)

3.2 The Oxidation Rate Equation

The growth rate of the oxide is then given as

\[ \frac{dX_o}{dt} = \frac{F}{N_i} = \frac{C^*}{N_i \left(\frac{1}{k_e} + \frac{X_o}{D}\right)} \]  

(3.13)

where \( N_i \) is the number of oxidizing species needed to form a unit volume of oxide. Upon integrating equation (3.13) we find,

\[ X_o^2 + \frac{2D}{k_e} X_o = \frac{2DC^*}{N_i} t + \text{constant} \]  

(3.14)

Using the initial condition \( X_o = X_o(0) \) at \( t = 0 \) (where \( X_o(0) \) is the native oxide thickness) we have,

\[ X_o^2 + \frac{2D}{k_e} X_o = 2 \frac{D}{N_i} C^* t + X_o(0)^2 + \frac{2D}{k_e} X_o(0) \]  

(3.15)

Equation (3.15) can be written in a compact form as follows:

\[ X_o^2 + AX_o = B(t + \tau) \]  

(3.16)

where \( A = \frac{2D}{k_e}, B = \frac{2D}{N_i} C^* \) and \( \tau = \frac{X_o(0)^2 + AX_o(0)}{B} \).
CHAPTER 3. THEORY OF THERMAL OXIDATION

The solution of equation (3.16) is,

\[ X_o = \frac{A}{2} \left[ \sqrt{1 + \frac{4B}{A^2}(t + \tau)} - 1 \right] \quad (3.17) \]

Two limiting cases can be identified from the solution to the growth rate equation,

i) For short durations of time, i.e. when \( (t + \tau) \ll t_c = \frac{A^2}{4B} \), the oxide growth equation yields

\[ X_o = \frac{B}{A}(t + \tau) = k_L(t + \tau) \quad (3.18) \]

where \( k_L = \frac{B}{A} = \frac{k_c C^*}{N_i} \) is the linear rate constant. The oxide thickness \( X_o \) follows a linear growth law and is controlled by the reaction rate \( k_c \) and by the solubility \( C^* \).

ii) For long durations of time, i.e. when \( (t + \tau) \gg t_c = \frac{A^2}{4B} \), the oxide growth equation yields

\[ X_o^2 = B(t + \tau) = k_P(t + \tau) \quad (3.19) \]

where \( k_P = B = \frac{2DC^*}{N_i} \) is the parabolic rate constant. The oxide thickness \( X_o \) follows a parabolic growth law and is controlled by the diffusion in the oxide and by the solubility \( C^* \). 'A = \frac{k_P}{k_L} \) is a critical thickness below which the kinetics are linear and above which the kinetics is parabolic.

3.3 Extraction of Oxidation Parameters

By differentiating equation (3.16) once we obtain,

\[ 2X_o \frac{dX_o}{dt} + A \frac{dX_o}{dt} = B \quad (3.20) \]

which gives

\[ \frac{dt}{dX_o} = \frac{A}{B} + \frac{2}{B} X_o = \frac{1}{k_L} + \frac{2}{k_P} X_o \quad (3.21) \]
CHAPTER 3. THEORY OF THERMAL OXIDATION

From the experimental values of thickness $X_o$ as a function of time $t$, $\frac{dt}{dX_o}$ can be determined and plotted as a function of $X_o$. The slope of this curve will give $\frac{2}{k_P}$ and the intercept at $X_o = 0$ will be equal to $\frac{1}{k_L}$. Another way of determining the rate constants is to write Equation (3.16) as,

$$X_o = \frac{B(t + \tau)}{X_o} - A$$

(3.22)

where $\tau$ is determined by extrapolating the $X_o$ versus $t$ graph to $X_o = 0$. By plotting experimental values of $X_o$ as a function of $(\frac{t + \tau}{X_o})$, $B$ and $A$ can be determined.

### 3.4 Comparison of Experimental Results with the Theory

The linear parabolic law of Deal and Grove explains satisfactorily the results obtained in the following cases for the oxidation of silicon,

a) In the case of wet oxidation for all thicknesses.

b) In the case of dry oxidation for thicknesses above 20-30 nm (for smaller thicknesses, this growth mode is preceded by faster kinetics).

Hence for practical purposes and to a first approximation, we can use the results given by the theory of Deal and Grove.

### 3.5 Growth Kinetics of Thin Oxide Films in Dry Oxygen

As explained earlier, while the Deal-Grove theory accounts for wet oxidations at all thicknesses, it cannot accurately model dry oxidations for thicknesses below 20-30 nm. Considering the experimental data, available today, pertaining to dry growth of SiO$_2$ and the difficulty in ensuring that the early stages of dry growth are really
dry, it is difficult to reach conclusions on the growth kinetics of thin films. However, the growth rate of thin films is consistently greater than that of thick films. There have been various theories that have been formulated to explain the higher initial dry oxidation rates observed in silicon.

Deal and Grove suggested the transport of the oxidizing species is faster for thinner films because of the presence of a larger electric field\[7\]. Revesz\[15\] proposed oxygen diffuses faster in channels when films are thin. These channels form as the oxide begins to grow. As the oxide thickens, the channels become increasingly distorted and the oxidation decreases. The above two models are not satisfactory. It is found experimentally that after the early stages, growth becomes linear (i.e limited by the rate of reaction at the interface)\[16\]. This has been explained by assuming that the reaction rate $k_\tau$ is higher for thinner films than for thicker films. This hypothesis serves to explain the observed difference in growth rates.

Hopper et al.\[17\] observed below 30 nm the slope of $\frac{dt}{dX_o}$ is approximately twice what it is above 30 nm. To interpret this observation, they assumed the oxidation proceeds by two parallel paths. One of them has a parabolic coefficient that contributes only when the oxide films are thin. Fargeix et al. and Tiller\[18, 19\] attributed the slowing down of the oxidation rates as due to a blocking layer in the oxide, a few hundred Å thick near the interface through which diffusion is slowed down. As can be seen a lot of theoretical models have been proposed over the years. So far none of these models have been able to explain all the experimental results obtained. To date a good model of growth kinetics when the oxide is thin ($X_o < 30$ nm) has not yet been devised. As devices are being scaled down constantly and the demand for thin gate oxides to help achieve low threshold voltages and control voltages, it is becoming increasingly important to understand thin oxide growth and consistently fabricate thin oxides with good interface characteristics to ensure interface trap densities in the low $10^{11}$ cm$^{-2}$eV$^{-1}$ and fixed charge densities in the low $10^{11}$ cm$^{-2}$eV$^{-1}$ ranges respectively.
3.6 SiC oxidation

SiC is perhaps the only semiconductor other than silicon for which a stable thermal oxide may be grown. The present development of these oxides is still in its infancy, although becoming a rather lively area of research of late. The advantages of 6H-SiC over silicon for reducing the on-resistance of power MOSFETS has been well documented in the literature[13]. Minimizing the interface states and fixed charge in the dielectric is essential for the successful operations of these MOSFETS. In all of the studies done so far, oxides grown on n-type 6H-SiC have excellent dielectric properties with interface state densities as low as $5 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ and fixed oxide charge of about $1 \times 10^{11} \text{ cm}^{-2}$ whereas oxides on p-type 6H-SiC have very high fixed charge around $8 \times 10^{12} \text{ cm}^{-2}$ and interface trap densities an order of magnitude higher than n-type 6H-SiC[9]. Baliga et al.[20] have been able to grow good quality gate oxides on p-type 6H-SiC using RPCVD techniques. Cooper et al.[14] have developed some good recipes for growing high quality gate oxides on 6H-SiC in which the formation of graphitic carbon at the surface of SiC is avoided by introducing the samples into the furnace in an oxygen ambient and ramping up the furnace temperature slowly before the oxidation.

Although several studies have been done on the oxidation of p-type 6H-SiC, very little research has been performed on growth of thin oxides on p-type 6H-SiC. As the trend in the semiconductor industry is towards lower gate control voltages that minimise the field across the gate insulator and smaller device geometries, it is necessary to grow high quality thin gate oxides in order to achieve smaller threshold voltages in these devices and also to accomplish low effective charge densities in these oxides. This thesis focuses on the first step to develop techniques for thin oxide growth on 6H-SiC to fabricate power devices with high switching speeds and low control voltages for operation.
Chapter 4
Experiments

4.1 Experiments on SiC oxidation

In the case of silicon the carrier gas has little or no effect on the wet oxidation rates\cite{7}. In this thesis wet oxidation of 6H-SiC has been carried out at 1150 °C for a variety of times at atmospheric pressure with two different carrier gases, namely oxygen and argon, to observe the effect of carrier gas on the oxidation rates. The 5mm x 5mm SiC substrates are 6H-SiC n/n+ and p/p+ substrate material with an epitaxial doping of $4 \times 10^{16}$/cm$^3$. The samples are given a standard RCA clean and a dilute HF dip immediately prior to loading inside the oxidation furnace. Since SiC is translucent, standard ellipsometry methods cannot be employed for thickness measurements. Instead, the oxidized wafers were selectively etched with a grid mask to form a stepped oxide pattern. The oxide thicknesses is determined subsequently with Atomic Force Microscopy (AFM) technique. The experimental results are summarized in Figure (4.1).

Figure (4.1) clearly shows the marked difference in the experiments with the two carrier gases. The oxidation rates of 6H-SiC are much higher in the initial phases of oxidation when oxygen is used as the carrier gas as compared to when argon is used as the carrier gas. This is a rather surprising result since this is not the case with silicon. The higher oxidation rates observed with oxygen as the carrier gas cannot be attributed to the excess oxygen present due to two reasons. The primary reason is that, if the excess oxygen were the cause, then there should be an observed dependence in silicon oxidation as well. Experiments, conducted in our lab, do not show any increase in oxidation rates for silicon when oxygen is used as the carrier gas instead of argon. Secondly, dry oxidation of 6H-SiC is a very slow process compared
CHAPTER 4. EXPERIMENTS

with wet oxidation and cannot explain such a huge increase in thickness of the oxide grown. Since in silicon wet oxidation follows Deal-Grove kinetics for all oxide thicknesses[16], we have attempted to use the Deal-Grove model to fit the observed time dependence of oxide growth. We find the Deal-Grove model fits the case when argon is used as the carrier gas but is insufficient in describing the initial oxidation phase when oxygen is used as the carrier gas. Therefore, the experiments suggest a different oxidation process when oxygen is used as the carrier gas as compared to when argon is used. In this thesis an alternate mechanism of oxidation is proposed to explain the excess oxidation in the initial phase when oxygen is used as the carrier gas.

Figure 4.1: Oxidation of 6H-SiC at 1150 °C
4.1.1 A Modified Deal-Grove model

A possible explanation for the higher oxidation rates with oxygen as the carrier gas is the availability of oxygen to remove carbon from the SiC lattice. We propose oxygen diffuses through the oxide, reacts with the carbon and removes it from the lattice, whereas, the inert gas argon is not able to perform the same function. This process creates channels for the hydroxyl ions (the oxidation species in a wet oxidation process) to initiate oxidation at the surface and in a small volume beneath the surface. As the hydroxyl ions come in contact with an increased supply of silicon atoms the oxidation rate is higher in the early phases as compared to the case where argon is used. As the oxidation time increases, the rate of oxidation when oxygen is used as the carrier gas, approaches the argon case of 1.2 Å /min after a time of approximately 150 minutes. This is expected since as the thickness of the oxide grown increases the ability of oxygen to diffuse to the interface decreases. Thus, the oxygen becomes progressively less effective in removing carbon from the SiC lattice and the oxidation rate decreases and approaches the argon case.

To model the case of oxidation with an oxygen carrier gas an extra term is added to the flux at the oxide-SiC interface \( F_3 \) in the original Deal-Grove model to describe the oxidation process in the bulk of SiC[21]. This extra term is modeled as a decaying exponential function of the oxide thickness. So the modified set of fluxes required to describe the oxidation of SiC are as follows:

\[
F_1 = H(C^* - C_S) \tag{4.1}
\]
\[
F_2 = D \left( \frac{C_S - C_i}{X_o} \right) \tag{4.2}
\]
\[
F_3 = (k_s + k_b \exp(-X_o/L)) \cdot C_i \tag{4.3}
\]

where \( H \) is Henry's constant, \( C^* \) is the equilibrium solubility limit of the oxidizing species in the oxide and \( C_S \) is the concentration of the oxidant in the oxide, \( D \) is the diffusion coefficient, \( C_i \) is the concentration of the oxidizing species at the oxide-SiC interface, \( X_o \) is the thickness of the oxide present, \( k_s \) is the surface reaction rate...
constant for oxidation, $k_b$ is the bulk reaction rate constant for oxidation with an exponential decay with the thickness of the oxide grown and $L$ is a characteristic oxide thickness.

At steady state the three fluxes must be equal.

$$F = F_1 = F_2 = F_3$$ (4.4)

Solving the above relation for $C_S$ and $C^*$ we find,

$$C_S = C_i (1 + \frac{X_o P}{D})$$ (4.5)

$$C^* = C_i (1 + \frac{P}{H} + \frac{X_o P}{D})$$ (4.6)

where $P = k_s + k_b \exp(-X_o/L)$. Therefore, the flux $F$ is given by,

$$F = \frac{C^*}{\left(\frac{1}{H} + \frac{X_o}{D} + \frac{1}{P}\right)}$$ (4.7)

We also know the rate of oxide growth is given by,

$$\frac{dX_o}{dt} = \frac{F}{N_i}$$ (4.8)

where $N_i$ is the number of oxidizing species required to form a unit volume of oxide. Combining equations (4.7) and (4.8) we find the first order differential equation for the rate of oxide growth,

$$\frac{dX_o}{dt} = \frac{C^*}{N_i} \left(\frac{1}{H} + \frac{X_o}{D} + \frac{1}{P}\right)$$ (4.9)

and the integral form of this equation becomes,

$$\int_{X_o(0)}^{X_o} (\frac{1}{H} + \frac{X_o}{D} + \frac{1}{P}) dX_o = \frac{C^*}{N_i} \int_0^t dt$$ (4.10)

Integrating out equation (4.10) we have,

$$\left(X_o - X_o(0)\right)[\frac{1}{H} + \frac{1}{k_s}] + \frac{X_o^2 - X_o(0)^2}{2D} + \frac{L}{k_s} \ln\left[\frac{k_s + k_b \exp(-X_o/L)}{k_s + k_b \exp(-X_o(0)/L)}\right] = \frac{C^*}{N_i} t$$ (4.11)
CHAPTER 4. EXPERIMENTS

In equation (4.11) the first two terms are in the original Deal-Grove model and the extra third term models the rapid oxide growth in the early stages of oxidation.

If we account for the initial thickness with an additional time \( \tau \), then we can write the final oxidation equation as,

\[
X_o^2 + AX_o + \frac{2DL}{k_s} \ln\left[\frac{k_s + k_b \exp(-X_o/L)}{k_s + k_b \exp(-X_o(0)/L)}\right] = B(t + \tau)
\]

where \( A = 2D\left(\frac{1}{H} + \frac{1}{k_s}\right) \), \( B = \frac{2DC^*}{N_t} \) and \( \tau = \frac{N_t}{2DC^*}[X_o(0)^2 + 2DX_o(0)(\frac{1}{H} + \frac{1}{k_s})] \).

Differentiating equation (4.12) we obtain,

\[
\frac{dt}{dX_o} = \frac{A}{B} - \frac{2Dk_b}{Bk_s[k_s \exp(X_o/L) + k_b]}
\]

Since all the experiments have been performed in the linear regime, we can neglect contributions to the slope from the parabolic term. Hence, we have

\[
\frac{dt}{dX_o} = \frac{A}{B} - \frac{2Dk_b}{Bk_s[k_s \exp(X_o/L) + k_b]}
\]

Equation (4.13) describes oxide growth where oxygen is used as the carrier gas. A very good fit has been obtained to the experimental values for the oxygen carrier gas case. Figure (4.2) shows both the experimental data and the theoretical fit. The argon curve has been modeled with the original Deal-Grove model. The value of \( B/A \) obtained from the argon carrier gas case has been used for the oxygen carrier gas case to model the growth.

A theoretical model has been presented along with a possible reaction mechanism to explain the higher growth rates of silicon dioxide on 6H-SiC when oxygen is used as the carrier gas as compared to when argon is used. The model also fits the observed experimental data very well. This additional growth term decays with the thickness of the oxide grown and after a time of about 150 minutes a linear growth rate of 2.2 Å per minute is observed for wet oxidation of 6H-SiC in the case of both carrier gases.
Chapter 4. Experiments

4.2 X-ray Photoelectron Spectroscopy Studies

4.2.1 Basic Theory of XPS Analysis

XPS in principle is the application of energy analysis to electrons emitted from the atomic core level of atoms by X-rays. The XPS as is used today on surfaces illuminated with X-rays is a direct result of pioneering work done by Siegbahn and his group at Uppsala University in Sweden[22].

The physical basis of the XPS technique is shown in Figure (4.3)[23, 24]. In the Figure (4.3) $E_b$ represents the binding energy of the electron to the core level (in this case the 2p(3/2)), $\phi$ is the work function of the element and $\nu$ is the frequency of the emitted electron.

Figure 4.2: Theoretical fit to the oxidation curves of 6H-SiC at 1150°C
The energy carried by an incoming X-ray photon is absorbed by the target atom, raising it into an excited state from which it relaxes by the emission of a photoelectron. Photoelectrons are emitted from all energy levels of the target atom and hence the electron energy spectrum is characteristic of the emitting atom type and may be thought of as its XPS "fingerprint". Lines in the spectrum are labelled according to the energy level from which they originated. The energy scale may be labeled as the binding energy of the level or in terms of the kinetic energy of the emitted electrons. By varying the angle at which the X-rays hit the surface of the sample, we can probe into different depths below the surface and from the electron energy spectrum obtained we can establish the composition of the material as a function of depth. A study of the concentration profiles as a function of depth into oxides formed on the 6H-SiC surfaces provides an understanding of the oxidation
CHAPTER 4. EXPERIMENTS

process on 6H-SiC.

4.2.2 Experiments and Results

6H-SiC p-type samples are RCA cleaned and a depth profile of silicon, carbon and oxygen performed with the XPS technique. A survey curve is obtained to determine the various elements present on the surface. This analysis on the bare SiC samples helps to establish a reference curve for further data obtained on processed samples.

After the calibration curve is established, oxidation is performed on the p-type samples at 1150°C for 10 minutes at atmospheric pressure. Two of the samples have been oxidized with oxygen as the carrier gas and two with argon as the carrier gas. Figure (4.4) shows the concentration profiles as a function of depth into the SiC surface which has been RCA cleaned. In this figure the Take-Off angle is the angle between the incident X-ray beam and the surface of the samples. So for a Take-Off angle of zero degrees, the beam is at grazing incidence. As the Take-Off angle increases, the beam probes deeper into the sample.

![Figure 4.4: Depth profile of the RCA cleaned p-type 6H-SiC sample](image)
CHAPTER 4. EXPERIMENTS

Figure 4.5: Depth profile of the oxidized p-type 6H-SiC sample (argon carrier gas). The silicon:carbon ratio is 1:1 for this case and is an indication of excess carbon left behind in the SiC lattice.

Figure 4.6: Depth profile of the oxidized p-type 6H-SiC sample (oxygen carrier gas). The removal of carbon from the SiC lattice by the excess oxygen is apparent in the ratio of silicon:carbon which is 3:1.

From Figure (4.4) we observe the main elements present are carbon, silicon and
oxygen. There is a large amount of carbon build up at the surface of the 6H-SiC samples. This profiling serves as a calibration standard for the processed samples.

Figures (4.5) and (4.6) show the concentration profiles as a function of depth into the oxide after the samples have been oxidized for the oxygen and argon carrier gas cases, respectively. We observe in the case of both argon and oxygen carrier gases the silicon:oxygen ratio is 1:2 indicating stoichiometric silicon dioxide. Also the silicon:carbon ratios are 1:1 and 3:1 in the argon and oxygen carrier gas cases respectively indicating much higher amounts of carbon in the oxide in the case of argon carrier as compared to the oxygen carrier case. This is to be expected based on the proposed mechanism of oxidation. Since oxygen is capable of removing the carbon from the SiC lattice more effectively than argon, less carbon will be left behind in the oxide and the lattice. Also, since oxygen removes the carbon from the interface, it is reasonable to expect oxides of better quality when oxygen instead of argon is used as the carrier gas. To see if this is really the case, electrical capacitance measurements have been performed on p-type 6H-SiC MOS capacitors fabricated with these oxides.
4.3 Capacitance Measurements

SiC power devices, as we have discussed in the introduction, have much to offer over their silicon counterparts. The fabrication of SiC power devices require electrical measurements to understand the oxide-SiC interface and the oxide quality on these devices. The SiC power devices are n-channel devices because hole mobilities are too low and lead to high on-resistances in these devices. Thus, in this thesis, all the electrical measurements were performed on MOS capacitors fabricated on p/p+ substrates of 6H-SiC.

The metal-oxide-semiconductor (MOS) capacitor is a useful test structure to characterize devices. It is very simple to fabricate when compared with MOSFETs and device parameters may be extracted which are useful for MOSFET transistor development. The C-V measurement is a common measurement to be performed on the MOS structure. With the help of the C-V measurements we can obtain device parameters like oxide thickness, doping profile, threshold voltage, oxide charge and interface trap densities.

To perform a C-V measurement, the semiconductor bulk is grounded while an AC signal of very small amplitude is superimposed on a slowly ramped DC voltage applied to the gate[25, 26]. The small AC signal causes the gate charge to fluctuate resulting in fluctuations of semiconductor charge around an equilibrium value to preserve charge neutrality. These fluctuations give rise to a differential capacitance between the gate and the substrate. Depending upon the DC bias value the semiconductor will be in one of four distinct regions: namely, accumulation, depletion, inversion or deep-depletion. In order to examine these four regions it is helpful to define a term called the surface potential in the semiconductor. To maintain consistency all potentials in the semiconductor will be referenced to the intrinsic Fermi level in the bulk.
Defining $x=0$ at the oxide-semiconductor interface, the potential at any distance $x$ into the semiconductor is defined as

$$\phi(x) = \frac{(E_{ib} - E_i(x))}{q} \quad (4.15)$$

where $E_{ib}$ is the intrinsic Fermi level in the semiconductor bulk and $E_i(x)$ is the intrinsic Fermi level at a distance $x$ from the interface. The surface potential is defined as the potential at $x=0$. This is shown in figure (4.7)

$$\phi_s = \frac{(E_{ib} - E_{is})}{q} \quad (4.16)$$

where $E_{is}$ is the intrinsic Fermi level at the surface and $\phi(x)$ is positive when the bands bend down. $E_{VAC}$ is the vacuum energy level.
CHAPTER 4. EXPERIMENTS

4.3.1 Accumulation Region

When a negative DC bias voltage is applied to the gate, holes (majority carriers) are attracted to the surface to balance the negative charge on the gate. The surface is said to be accumulated when the surface potential condition \(-\frac{E_g}{2q} - \phi_F \leq \phi_s \leq 0\) is satisfied where \(\phi_F\) is the Fermi potential and \(E_g\) is the energy-gap of the semiconductor. The Fermi potential is also referenced to the intrinsic energy in the bulk

\[
\phi_F = \frac{E_{ib} - E_F}{q} = \frac{kT}{q} \ln \left( \frac{N_B}{n_i} \right)
\]

(4.17)

where \(N_B\) is the bulk doping density and \(n_i\) the intrinsic carrier concentration. There is no change in the Fermi potential in an MOS structure when thermal equilibrium is established in the measurements of accumulation region. All the electric field lines in this structure originate from the accumulation layer at the interface and terminate on the gate. Assuming negligible series resistance, the capacitance between the gate and the substrate in accumulation is simply the oxide capacitance whose area is equal to the area of the gate electrode neglecting edge effects for a large area gate. The measured capacitance is simply the oxide capacitance, \(C_{ox}\). The capacitance for a parallel plate capacitor is

\[
C_{ox} = \frac{K_{ox} \varepsilon_o}{X_o}
\]

(4.18)

where \(X_o\) is the dielectric thickness, \(K_{ox}\) is the relative dielectric constant, and \(\varepsilon_o\) is the permittivity of free space.

A special condition known as flatband arises when the intrinsic bulk energy equals the intrinsic surface energy \((\phi_s = 0)\). For an ideal MOS structure this condition is established when the gate bias is zero volts.

4.3.2 Depletion Region

As the gate bias increases and tends to go positive the holes experience an electric field to propel them towards the substrate contact thereby depleting the surface of holes. This ‘depletion’ width increases as more holes are repelled from the surface.
CHAPTER 4. EXPERIMENTS

Depletion occurs when the condition $0 \leq \phi_s \leq \phi_F$ holds. When this condition occurs, the insulating depletion region causes the effective parallel capacitor plates to move further apart and the overall capacitance consists of oxide and semiconductor capacitance ($C_s$) connected in series. A reduction in measured capacitance is observed as the depletion region widens.

4.3.3 Inversion Region

A surface potential of $\phi_F \leq \phi_s \leq (E_g/2q + \phi_F)$ results in an abundance of electrons (minority carriers) at the semiconductor surface since the surface potential is below the Fermi potential in the semiconductor. The surface is said to be inverted due to the high minority carrier concentration. When the gate voltage establishes a surface potential of $\phi_s = 2\phi_F$ the surface is as concentrated with electrons as the bulk is with holes. The gate voltage that achieves this condition is known as the threshold voltage, $V_T$, and marks the onset of 'strong' inversion. The threshold voltage is generally a good reference point for sufficient channel conduction in MOSFETs. In very strong inversion as $\phi_s$ approaches $E_g/2q + \phi_F$, a parallel plate capacitor exists similar to accumulation between the positive gate charge and the inversion layer of negative surface charge separated by the gate dielectric. The measured capacitance approaches the oxide capacitance, $C_{ox}$. In traversing between the limits of strong accumulation and strong inversion the total band bending is equal to $E_g$, the bandgap of the semiconductor.

4.3.4 Deep-Depletion

In a two terminal MOS capacitor test structure there are no external minority carrier sources. If the minority carrier generation rate is very low, then to balance the charge on the gate, then the depletion region keeps on widening with increase in the gate bias to increase the semiconductor charge. As the depletion region widens, the semiconductor depletion capacitance decreases. Since the semiconductor capacitance and the oxide capacitance are in series the measured capacitance between the
CHAPTER 4. EXPERIMENTS

gate and the substrate keeps on decreasing in the "inversion" region. This effect is called deep-depletion.

In a capacitor structure, the lack of source/drain minority carrier regions can make it difficult for surface inversion to occur and establish an equilibrium condition. Minority carrier generation by thermal excitation is extremely difficult at room temperature in wide band-gap semiconductors such as SiC. Therefore, it is often desirable to generate excess minority carriers by illuminating the device or using an n+ junction, as a source of minority carriers, underneath the gate (i.e. a gated diode structure).

In the low frequency case we assume the AC measurement signal is at a sufficiently low frequency (LF) so the generation-recombination of electrons have time to respond to the small signal voltage fluctuations. At higher frequencies (HF), the inversion layer can no longer respond to the quickly changing charge variations and the C-V curve will not rise back to $C_{ox}$.

An ideal theoretical SiC C-V curve has been plotted in Figure (4.8).

![Figure 4.8: Ideal SiC CV curves for low and high frequencies](image)

Figure 4.8: Ideal SiC CV curves for low and high frequencies
4.4 Non-Ideal MOS Capacitors

The previous analysis assumed an ideal insulator and interface and also no work function difference between the gate material and the semiconductor. Experimentally, however finite gate-semiconductor work function difference, charges in the oxide and traps at the interface introduce deviations to the ideal C-V curve and alter the performance of the device. Various types of charges can exist in the oxide in a MOS capacitor such as fixed charge, mobile charge, oxide trapped charge and interface trapped charge[26]. In an optimized process the main causes of non-ideal C-V curves are the gate-semiconductor work function difference, the fixed charge and the interface trapped charge. These factors will be discussed in terms of their origin and effect upon the C-V measurement.

4.4.1 The Gate to Semiconductor Work Function Difference ($\phi_{GS}$)

The gate to semiconductor work function difference is the difference between the Fermi-levels of the gate and the semiconductor. For a metal gate $\phi_{GS}$ is given by,

$$\phi_{GS} = \phi_M - (\chi_s + \frac{E_G}{2q} + \phi_F)$$  \hspace{1cm} (4.19)

where $\phi_M$ is the metal work function, $\chi_s$ the electron affinity of the semiconductor, $\phi_F$ the Fermi potential of the semiconductor and $q$ is the electronic charge.

In the case of a polysilicon gate, the gate to semiconductor work function difference is given by,

$$\phi_{GS} = (\chi_P + (E_{CP} - E_{FP})/q) - (\chi_s + (E_G - E_F)/q)$$  \hspace{1cm} (4.20)

which can be written as (assuming $\chi_P = \chi_s$),

$$\phi_{GS} = \phi_{FG} - \phi_F$$  \hspace{1cm} (4.21)

where $\chi_P$ is the polysilicon electron affinity, $E_{CP}$ and $E_{FP}$ are the polysilicon conduction band and Fermi energy levels respectively, $\phi_{FG}$ the Fermi potential of the
gate, $\chi$, the electron affinity of the semiconductor and $q$ is the electronic charge. The finite work function difference causes a shift in the C-V curves by an amount equal to the difference and has to be accounted for while extracting information from the C-V curves.

### 4.4.2 Fixed Oxide Charge ($Q_f$)

Fixed charge has been found to be always positive, due primarily to structural defects in the oxide layer less than 25Å from the oxide-semiconductor interface[26]. The density of this charge, whose origin is related to the oxidation process, depends on the oxidation ambient and temperature, on cooling conditions and on silicon orientation. The higher the oxidation temperature, the lower is the $Q_f$. However, if higher temperatures are not possible in a given set up, then $Q_f$ can also be lowered by annealing the oxidized wafer in an inert ambient immediately after the oxidation. Since this charge is fixed and not dependent upon surface potential, fixed charge will not contribute to the differential capacitance. However, fixed charge will cause the entire C-V curve to shift parallel to the left by an amount $\Delta V$. If we assume an amphoteric interface trap model where the traps in the upper half of the band-gap are acceptors and the traps that lie in the lower half of the band-gap are donors and are uniform in density throughout the band-gap, then at weak inversion the acceptor traps are empty and the donors in the bottom part of the gap are filled and hence $Q_{it}$ is zero. Therefore, the amount of fixed charge can be obtained by measuring the voltage shift between the experimental and theoretical C-V curves at weak inversion.

### 4.4.3 Interface Trapped Charge ($Q_{it}$)

The origin of interface traps has been attributed to the unsatisfied dangling bonds which result from the abrupt termination of the lattice at the semiconductor surface. These traps are treated as existing at or near the oxide-semiconductor interface with distributed energy levels within the band gap of the material. The interface trap
CHAPTER 4. EXPERIMENTS

occupancy is a function of the band bending in the semiconductor and is based on
the familiar Fermi-Dirac statistics. The changing of charge states of these traps as
a function of gate bias produces an additional capacitance to the MOS system. The
interface trap capacitance is modeled as being in parallel with the semiconductor
capacitance. In addition to an increased capacitance, interface traps also produce a
stretch-out in the C-V curves.

4.5 MOS Device Characterization Techniques

Over the years numerous techniques based on the high and low frequency C-V
measurements have been developed to characterize the charges present in the gate
dielectric and the interface traps. Some of the prominent ones are the Hi-Lo C-
V technique[27] used for determining the average density of interface traps, the
conductance method, devised by Nicollian and Goetzberger[28] which is the most
sensitive method and also the most tedious and time consuming, charge pumping[29],
gated diode measurements[30], thermally stimulated emission measurements and
subthreshold slope measurements in which the MOSFET is used as the test structure
and the High Frequency (Terman) method[31] which is the easiest of the above
methods to obtain interface trap densities.

Since MOS capacitors are easier to fabricate than MOSFETS, especially in SiC
devices, and interface trap densities in SiC devices are in the $10^{11}$cm$^{-2}$eV$^{-1}$ range
in which the Terman technique is accurate enough and the easiest of the methods
available, the HF C-V technique is used to characterise the SiC capacitors. This
method is described in a little more detail below.

4.6 High-Frequency C-V Technique

The HF C-V technique relies on a C-V measurement at a frequency high enough
that interface traps are assumed not to respond and thereby do not contribute any
extra capacitance to the measurement. Although interface traps do not respond
CHAPTER 4. EXPERIMENTS

to the ac probe frequency, they are capable of responding to the much slower DC voltage ramp and cause the C-V curve to stretch out along the gate voltage axis as the interface trap occupancy varies with gate bias and the charge induced by the gate bias shared between the semiconductor bulk charge, inversion charge, interface traps and fixed charge.

\[ Q_G = -(Q_S + Q_{it} + Q_f) \]  \hspace{1cm} (4.22)

where \( Q_S \) is the semiconductor charge and is the sum of the bulk charge and inversion layer charge, \( Q_f \) and \( Q_{it} \) are the fixed oxide charge and Interface trapped charge, respectively.

\[ V_{GB} = V_{FB} + \phi_s + V_OX = V_{FB} + \phi_s + \frac{-(Q_S + Q_{it})}{C_{OX}} \]  \hspace{1cm} (4.23)

From these equations we observe for a given surface potential, \( V_{GB} \) increases when acceptor interface traps are present and cause the stretch-out in the C-V curve. Interface traps distributed uniformly in the bandgap lead to a fairly smoothly varying but distorted C-V curve. Other distributions produce more abrupt distortions in the C-V curve. The interface trap capacitance is modeled as being in parallel with the semiconductor capacitance.

\[ C_{HF} = C_{ox}C_s/(C_{ox} + C_s) \]  \hspace{1cm} (4.24)

\( C_{HF} \) is the same as that of a device without interface traps for the same \( C_s \). The variation of \( C_s \) with surface potential is known for the ideal MOS system. The procedure for extracting \( D_{it} \) is as follows: From the ideal MOS C-V curve, the \( \phi_s \) value for a given \( C_{HF} \) is determined. Then, for the same \( C_{HF} \), the gate voltage \( V_{GB} \) is found from the experimental curve, thereby giving one point on the \( \phi_s - V_{GB} \) curve. By repeating this procedure for various \( C_{HF} \) values the total \( \phi_s - V_{GB} \) curve is obtained. This curve contains all the relevant interface trap information. The interface trap density is determined from this curve using,

\[ D_{it} = \frac{C_{ox}}{q} \left[ \frac{dV_{GB}}{d\phi_s} \right] - \frac{C_s}{q} \]  \hspace{1cm} (4.25)
CHAPTER 4. EXPERIMENTS

With careful measurements and analysis combined with a knowledge of the substrate doping density this method can be used for a good estimation of interface trap densities to the low $10^{10}\text{cm}^{-2}\text{eV}^{-1}$ range.

4.6.1 Experimental Results

Since 6H-SiC has a wide bandgap of 3.0 eV at 300K, the intrinsic carrier concentration turns out to be in the $10^{-7}\text{cm}^{-3}$ range. Therefore, at room temperature, to obtain equilibrium C-V measurements we must wait a very long time in Silicon Carbide. By carrying out the measurement at sufficiently high temperatures, the intrinsic carrier concentration is increased, thereby, facilitating faster measurements. The HF C-V measurements in this study were made at 600K by allowing 2 minutes per point with 0.5 V steps for attaining equilibrium. A UV lamp was used to initiate inversion in the 2 terminal MOS structures. Also, MOS structures on p-type 6H-SiC substrates have been used as they have higher fixed oxide charge values.

![Figure 4.9: High frequency CV curves for the argon carrier gas case](image)

Figure 4.9: High frequency CV curves for the argon carrier gas case
CHAPTER 4. EXPERIMENTS

Figure 4.10: High frequency CV curves for the oxygen carrier gas case

Figures 4.9 and 4.10 show measured C-V curves along with ideal C-V curves for the cases of argon and oxygen as carrier gases respectively. An analysis of these figures, as outlined in the previous section together with an accounting of the metal-semiconductor work function difference and fixed charge, indicates mid-gap interface trap densities \((D_{it})\) of \(5 \times 10^{11}\text{cm}^{-2}\text{eV}^{-1}\) for the argon carrier gas case and \(2.5 \times 10^{11}\text{cm}^{-2}\text{eV}^{-1}\) for the oxygen carrier gas case. Fixed oxide charge \((Q_f)\) is \(8 \times 10^{11}\text{cm}^{-2}\) and \(4 \times 10^{11}\text{cm}^{-2}\) in the argon and oxygen carrier gas cases, respectively.

The C-V measurements indicate a higher density of interface traps and fixed charge for the argon carrier gas as compared with the oxygen carrier gas. As explained earlier, XPS studies on the oxidized samples show oxygen is successful in removing the carbon from the interface in contrast with argon, which may be the cause for a reduction in interface traps and fixed charge in the MOS system. The above analysis suggests we should use oxygen as the carrier gas in a wet oxidation process as outlined earlier in order to provide better quality oxides on p-type 6H-SiC substrates. This will be very beneficial in improving the quality of power devices fabricated on 6H-SiC devices.
CHAPTER 4. EXPERIMENTS

4.7 Electrical Breakdown Measurements

Electrical conduction in thin insulating films has been the subject of numerous experimental investigations\[16, 32\]. The currents in these films can generally be classified as bulk limited or electrode limited. Since thermally grown SiO\(_2\) has an extremely wide bandgap and consequentially high energy barriers at its electrodes it is more likely to show electrode limited conduction. The MOS capacitor serves as a useful test vehicle to carry out tunneling current and breakdown measurements on insulators. In order to isolate the effect of the gate bias to the insulator only, tunneling and breakdown tests on MOS capacitors are always carried out under the accumulation condition.

In this work, all electrical measurements were carried out on MOS capacitors fabricated on p-type substrates for reasons specified earlier. From the energy band diagram of the metal-silicon dioxide-SiC (MOS) system it can be seen that the barrier energy for holes (\(\phi_b\)) is around 2.0 eV. Under negative bias on the gate electrode, Fowler-Nordheim tunneling (the dominating mechanism at room temperature) of holes from the SiC valence band to the oxide valence band can be observed.

The theory of Fowler-Nordheim emission has been worked out to various degrees of sophistication\[32\]. In the simplest case of emission into vacuum, a triangular barrier, free electron gas model and the WKB approximation for the tunneling probability the following expression is obtained for the Fowler-Nordheim tunnel current,

\[
J = J_0 (E/E_o)^2 \exp \left( -\frac{E_o}{E} \right)
\]

(4.26)

where \(E_o = \frac{4\sqrt{(2q(m^*)^2)}(\phi_b)^{1.5}}{3h}\) is a characteristic tunneling electric field, \(h\) is Planck's constant, \(q\) the electronic charge, \(E\) the electric field across the insulator, \(\phi_b\) is the barrier height for holes and \(m^*\) is the effective mass of holes in the tunneling process. A plot of \(J/E^2\) versus \(1/E\) will yield a straight line whose slope provides the ratio of the barrier height to the effective hole mass (\(\phi_b/m^*\)).
CHAPTER 4. EXPERIMENTS

4.7.1 Experimental Results

Since oxides on p-type 6H-SiC substrates is of most interest as pointed out earlier, Aluminum was evaporated on the oxidized p-type samples and patterned to form the gates of MOS capacitors on p-type 6H-SiC. Electrical breakdown measurements were carried out on these MOS capacitors at room temperature by biasing the capacitor in accumulation, so that most of the applied gate voltage falls across the silicon dioxide layer, and measuring the substrate to gate current. The gate voltage was increased and the gate to substrate currents measured until the oxides broke down.

A plot of the current density versus the field across the oxide is shown in Figure (4.11). The flatband voltage was subtracted from the applied gate voltage and the result divided by the oxide thickness to calculate the field across the oxide. Figure (4.11) illustrates the breakdown behaviour of oxides grown on 6H-SiC substrates. The breakdown field strength observed in these oxides is about 8.5 MV/cm for both carrier gas cases. The soft breakdown region between 6 MV/cm and 8 MV/cm is indicative of Fowler-Nordheim tunneling through the oxide. A Fowler-Nordheim plot as described earlier is shown in Figure (4.12).

![Figure 4.11: Breakdown measurement on p-type capacitors](image.png)
CHAPTER 4. EXPERIMENTS

Figure 4.12: Fowler-Nordheim plot of hole tunneling for an accumulated surface on p-type SiC MOS capacitors

From the Fowler-Nordheim plot the barrier height for hole injection can be extracted for the MOS system. To find the barrier height for holes the effective mass of holes should be known. In the present work since hole mobility is very small in 6H-SiC, the effective tunneling mass for holes (m*) was taken to be the rest electron mass (m_e). A value of 2.0 eV was obtained for the barrier height (\phi_b) for hole tunneling. The extracted barrier height will be lower than the actual barrier height due to image force induced barrier lowering under high gate bias. From the MOS system for 6H-SiC the energy difference between the valence bands of the oxide and 6H-SiC is about 2.0 eV. So a very good agreement is obtained for the extracted hole tunneling barrier height. In fact, this also indicates the effective mass used for the holes is probably very close to the actual value.
Chapter 5

Conclusions

5.1 Conclusions

From the work performed in this thesis we see, power devices, like the DMOS and IGBT structures fabricated on 6H-SiC, have significant advantages over their silicon counterparts in terms of improved breakdown voltages, lower specific on-resistances, higher current densities and higher operating temperatures. The importance of a good gate oxide has also been stressed upon for the power devices to be efficient in operation.

5.1.1 6H-SiC Oxidation

The dependence of wet oxidation rates on 6H-SiC upon the carrier gas used has been investigated for the growth of thin oxides. Wet oxidation with an inert gas like argon follows the ideal Deal-Grove oxidation model whereas oxidation with oxygen as the carrier gas does not. A modified Deal-Grove model based upon surface and bulk reaction rate constants has been developed to model the wet oxidation rates when oxygen is used as the carrier gas. XPS studies done on the oxidized p-type samples indicate carbon build up on RCA cleaned 6H-SiC surfaces. XPS analysis of oxidized samples indicates lesser amounts of carbon in the oxide when oxygen is used as the carrier gas as opposed to argon. This lends support to the mechanism suggested in the thesis to account for the higher oxidation rates and better oxide quality obtained when oxygen is used as the carrier gas.
CHAPTER 5. CONCLUSIONS

5.1.2 Electrical Measurements

Electrical C-V and breakdown measurements have been done on MOS capacitors fabricated on the oxidized p-type 6H-SiC samples for the case of both carrier gases. Both samples indicate breakdown field strengths of 8.5 MV/cm. The sample obtained by oxidizing using oxygen as the carrier gas exhibits less fixed charge and interface trap densities (4 x \(10^{11}\) cm\(^{-2}\) and 2.5 x \(10^{11}\) cm\(^{-2}\)eV\(^{-1}\) respectively) as compared to the argon carrier gas case (8 x \(10^{11}\) cm\(^{-2}\) and 5 x \(10^{11}\) cm\(^{-2}\)eV\(^{-1}\) respectively) based on values obtained from the C-V curves for both cases. Both oxides exhibit Fowler-Nordheim tunneling with a tunneling barrier height for holes of 2.0 eV.

In conclusion an oxidation procedure has been developed to grow good quality thermal oxides on 6H-SiC. This will aid in the fabrication of high quality power devices which rely on electron transport in inversion layers beneath the surface.

5.2 Recommendations

To further aid in the development of good growth techniques for thin gate oxides for use in 6H-SiC power devices, it would be worthwhile to study the temperature dependence of oxidation rates of 6H-SiC using both the carrier gases. From this study one can extract the activation energies for the oxidation process in the two cases and see how they compare to the Si-C bond energy and the Si-Si bond energy. This would then help in further understanding the oxidation kinetics of 6H-SiC and may lead to the development of better oxidation techniques. Another area of study would be to do the oxidation at different pressures to observe any effect on the electrical properties of the oxides grown.
References


REFERENCES


REFERENCES


REFERENCES


Appendix A

SEMICAD:DEVICE SIMULATOR

A.1 Introduction to SEMICAD

SEMICAD DEVICE by DAWN Technologies is a general purpose two-dimensional device simulator capable of simulating a wide range of devices such as diodes, FETs, BJT's, Thyristors, IGBTs and CCDs. SEMICAD incorporates advanced physics models for mobility, recombination-generation effects, tunneling and band-gap narrowing. It is also quite flexible in the sense the user may specify his/her own physics models and perform simulations.

To simulate a device, the user needs to specify the device geometry, physical parameters for the device and various physics models that govern the operation of the device. SEMICAD has built in library files which allow the user to choose from a variety of semiconductors, insulators and metals for the device to be simulated. SEMICAD also allows the user to manipulate the various parameters specified for each of these materials in their respective library files. In the present version of SEMICAD there is no library file for Silicon Carbide. So we created our own SiC library file by gathering data from the literature [2]. This library file is given in Appendix B. The SIM-C language, which bears a resemblance to the regular C language with a few modifications, is used as the means of communication with the device simulator.

A.2 SEMICAD Installation

Initially, SEMICAD was installed on the SUN workstations in our lab at the Sherman Fairchild Center. But, we discovered it takes unacceptably long times to finish
simulating our device structures because of the limited capabilities of the workstations in our lab. So, we shifted the software from our lab to the SOLARIS work environment in Packard Lab which offers giga-op facilities. The decrease in simulation time due to this switch is over two orders of magnitude which definitely justifies the transfer of the software to Packard lab. The SEMICAD package is currently installed on an UltraSPARC 20 machine called “pixie” in the SOLARIS environment at Packard Lab.

A.3 Setting Up a SEMICAD Simulation

A.3.1 Specifying the Device

For specifying the device geometry, doping profiles for various regions, interfaces, boundaries etc. a SIM-C code has to be written and the file saved with the extension .dev.

Every device file starts with a list of the libraries to be included in the device simulation. SEMICAD is flexible in the sense the user can develop his own material libraries and use them in the simulations. Also, SEMICAD permits the user to choose his criteria for convergence of the simulation. The device is then given a name and certain geometric dimensions and gridding parameters. Then all the regions in the device are individually defined along with all their relevant parameters and coordinates. Once the device regions have been specified, the metal regions in the device are specified followed by the boundary type of the electrodes(Ohmic/Schottky) and electrode coordinates. An example code that specifies a DMOSFET device is given for illustration purposes. The name of the device file is “dmost.dev”.

56
A.3.2 dmost.dev

/* This is a Device file that is used to construct a */
/* DMOSFET device cross-section that is subsequently used */
/* for all the simulations */
/* File Name : dmost.dev (note: the extension has to be .dev) */

******* Libraries included for the simulation *******
#library "~/home/benson4/viv2/semicad/sic1.lib"
#library "Conductor.lib"
#library "Insulator.lib"

/* The device object has been named "mosfet" for this simulation */
device mosfet {
    width = 40;
    orders = 10;
    minSpacing=0.1;

    /* Defining the n-plus drain region */
    region dnplus {
        material = &SiC;
        temperature=473;
        coordinates = {{0,11},{12,11},{12,10},{0,10}};

        profile dnplus_doping {
            species = &N_Si;
            field uniform {
                multiplier = 1e19;
            }
        }
    }

    /* n-minus "drift" region definition */
    region dnminus {
        material = &SiC;
        temperature=473;
        coordinates = {{0,10},{12,10},{12,1},{5,1},{5,0},{0,0}};

        profile dnminus_doping {
            species = &N_Si;
            field uniform {
                multiplier = 5e14;
            }
        }
    }

    /* p-well region definition */
    region psub {
        material = &SiC;
        temperature=473;
        coordinates = {5,0},{5,1},{12,1},{12,0},{10,0},{10,0.25},
                      {7,0.25},{7,0};

        profile psub_doping {
            species = &Al_Si;
        }
    }
}

57
APPENDIX A. SEMICAD: DEVICE SIMULATOR

field uniform {
  multiplier = 1e17;
}
}

/***********************************************************/
/* n-plus source region definition */
region nplus {
  material = &SiC;
  temperature=473;
  coordinates = {{7,0.25},{10,0.25},{10,0},{7,0}};
  profile nplus_doping {
    species = &N_Si;
    field uniform {
      multiplier = 1e18;
    }
  }
}

/***********************************************************/
/* Gate oxide region definition */
region oxide {
  material = &SiO2;
  simulate="false";
  coordinates = {{0,0},{8,0},{8,-0.04},{0,-0.04}};
}

/***********************************************************/
/* Definition of Metal regions */
region DrainMetal {
  material = &Al;
  simulate = "false";
  coordinates = {{0,11},{0,11.2},{12,11.2},{12,11}};
}

region SourceMetal {
  material = &Al;
  simulate = "false";
  coordinates = {{8.5,0},{9.5,0},{9.5,-0.5},{8.5,-0.5}};
}

region SubstrMetal {
  material = &Al;
  simulate = "false";
  coordinates = {{10.5,0},{11.5,0},{11.5,-0.5},{10.5,-0.5}};
}

/***********************************************************/
/*Definitions of Boundaries and Electrodes */
boundary source {
  type = "ohmic";
  coordinates = {{8.5,0},{9.5,0}};
}

boundary drain {
  type = "ohmic";
  coordinates = {{0,11},{12,11}};
APPENDIX A. SEMICAD:DEVICE SIMULATOR

boundary subs {
  type = "ohmic";
  coordinates = {10.5,0},{11.5,0};
}

boundary gate {
  metal = #Al;
  type = "insulator";
  epsi = 3.9;
  tin=40;
  coordinates = {0,0},{3,0},{6,0},{8,0};
}

Once the SIM-C code has been written to specify the device, the user can use a built-in sub-routine to view the device he has created.

The command is

simcc showdev <filename>.

This will bring up the device as specified in the device file onto the screen and can be checked for correctness. The output from running the device file is shown in Figure (A.1).

A.3.3 Specifying the Device Run File

Once the device file has been specified correctly, the next step is to write the SIM-C code that would perform the required simulations. The SIM-C language is very easy to use and is an interpreted language which simplifies the programming a great deal. The simulation file has to have the extension .run.

An example run file for the device file with the filename “dmost.dev” specified earlier is given for illustration purposes.
APPENDIX A. SEMICAD: DEVICE SIMULATOR

A.3.4 dmosfet.run

/* --------------------------------------------------------------
 * file : dmosfet.run
 * purpose : simulate the Id-Vds characteristics of the DMOS for
 * Vgs = 10 Volts, Vds = 0..8 Volts, Drift layer d,(10..100)
 * date : 02/26/97
 * --------------------------------------------------------------
 */
#include "dmost.dev"

main()
{
/* Open a file into which all simulation results necessary will be put */
    ShowProgress = "true";
    outfile = "dmos.dat";
    rewrite(outfile);
******************************************************************************
/* Loop for varying the drift layer thickness */
for (d=10;d<100;d+=10){
    di=d+0.5;
    d2=d+1.0;
/* Reconfiguring the device structure every time the drift layer thickness */
/* is changed */
    mosfet.dnminus.coordinates={{0.dh{12.d}.{12.H
        {6.H.}{6.0}.0.0}};
    mosfet.dpplus.coordinates={{0.d2}.{12.d2}.{12.d}.0.d};
    mosfet.DrainMetal.coordinates={{0.d2}.0.d2+0.2}.12.d2+0.2].
        {12.d2}};
    mosfet.drain.coordinates={{0.d2}.12.d2}};
******************************************************************************
/* Setting up initial biases for the DMOSFET device */
    mosfet.gate.bias=0.0;
    mosfet.drain.bias=0.0;
    mosfet.subs.bias=0.0;
    mosfet.source.bias=0.0;
******************************************************************************
/* Obtaining initial convergence by solving the Poisson condition in device */
    id = mosfet.drain.current;
    fetsave = mosfet;
******************************************************************************
/* Loop to raise up gate voltage to 10 Volts in steps of 0.26 Volts for */
/* smoother convergence */
for (vgs=10.0; vgs<=10.0; vgs+=1)
{ mosfet = fetsave;
    vgs_old = mosfet.gate.bias;
    for (v=vgs_old; v<=vgs; v=v+0.26) /* adjusting Vgs */
    {
        mosfet.gate.bias = v;
        id = mosfet.drain.current;
    }
}
APPENDIX A. SEMICAD: DEVICE SIMULATOR

fetsave = mosfet;
/*-------------------------------------------------------------------------------------------*/
/* Ramp up the drain voltage in steps of 0.5 Volts and write the voltages and currents and drift layer thickness onto the file */
/* sweeping Vds */
for (vds=0; vds<=8; vds+=0.5) /* sweeping Vds */
{
    mosfet.drain.bias = vds;
    id = mosfet.drain.current;
    nprintf(outfile,"%f %6.3f %6.3f %12.3e\n",d,vgs ,vds,id);
} /*--------------------------------------------------------------------------------------------*/
/* If drain voltage = 3.0 volts save the simulation to a file that can be used to see potential, field and carrier distributions in the device */
if(vds==3.0) save("mosfet.obj.1",&mosfet);
}
printf("Execution Time %g (sec)\n", ExecTime);

The simulation file specified above simulates I-V characteristics for the DMOS-FET at a gate bias of 10 Volts, for drain voltages ranging from 0 to 8 Volts for various drift region thickness from 10 microns to 100 microns. The code is self-explanatory with a few syntaxes that need to be learned about the way device objects are addressed in SEMICAD.

A.4 Viewing of Simulation Results

A.4.1 FLEXVISION

FLEXVISION is a SIM-C application which provides an interactive graphical user interface for visualising and plotting data. The visualizer permits rapid visualization of data from the simulation. There are also built in templates in FLEXVISION that allow plotting of potentials, carrier concentrations electric fields and so on in the device. In this section some of the results from the simulation are shown for illustration purposes on how to use FLEXVISION.

A very useful capability of the FLEXVISION package is that it allows saving
APPENDIX A. SEMICAD:DEVICE SIMULATOR

of two dimensional plots in a postscript format which can be later imported into LaTeX documents. Also, FLEXVISION allows the user to look at slices of 2D plots thereby creating 1D plots along any direction in the 2D plane.

As seen in the simulation code, the device simulation results are stored in the file “mosfet.obj.1” under the conditions of \( V_{ds} = 3 \) Volts, \( V_{gs} = 10 \) Volts for a drift layer thickness of 10 microns.

A.4.2 Doping, Potential and Current Density Profiles in the DMOSFET

A plot of the doping and potential profiles in the device can be obtained by using the following commands:

1) Doping profile: flexvision -tmpl dope.tmpl -data “Dataset 1” dev mosfet.obj.1

2) Potential profile: flexvision -tmpl psi.tmpl -data “Dataset 1” dev mosfet.obj.1

The user can also make his/her plots within the FLEXVISION framework. The potential contour plot and current density plot for the bias condition specified are shown in Figures (A.2) and (A.3). In conclusion, FLEXVISION is a very powerful visualizer for simulation results from SEMICAD and serves to get meaningful insights into the operation of various semiconductor devices.
Figure A.1: DMOSFET Layout
Figure A.2: DMOSFET Potential Profile for $V_{ds} = 3$ Volts, $V_{gs} = 10$ Volts
Figure A.2: DMOSFET Potential Profile for $V_{ds} = 3$ Volts, $V_{gs} = 10$ Volts
Figure A.3: DMOSFET Current Density Contours for $V_{ds} = 3$ Volts, $V_{gs} = 10$ Volts. The plot clearly shows the bottleneck effect of the JFET region and the subsequent current spreading towards the drain.
Figure A.3: DMOSFET Current Density Contours for $V_{ds} = 3 \text{ Volts}, V_{gs} = 10 \text{ Volts}$. The plot clearly shows the bottleneck effect of the JFET region and the subsequent current spreading towards the drain.
Appendix B
SiC Library File

B.1 SiC Library File for SEMICAD

The Silicon Carbide library file with parameters for 6H-SiC is given below for reference purposes.

B.1.1 SiC.lib

/*
 *  >>>>>>>>>>>>>>>>>>>> SEMICAD(tm) LIBRARY FILE
 *  Copyright (c) 1991 Dawn Technologies, inc. All Rights Reserved
 *  PURPOSE: Standard Silicon Carbide Materials Library (1.11)
 *  SCCS: @(#)SiC.lib (1/30/97)
 */
semiconductor SiC
{
    eps = 9.66;
    eg = {0.0: 3.099, 300.0: 3}["temperature"];    
    chi = 4.0;    
    gn = 2;    
    gp = 4;    
    tn = 1.0e-9;    
    tp = 1.0e-9;    
    bgnType = bgn2;    
    bgnN0 = 4.5e17;    
    bgnV0 = 9e-3;    
    bgnAN = 10.23e-3;    
    bgnBN = 13.12e-3;    
    bgnCN = 2.93e-3;    
    bgnAP = 11.07e-3;    
    bgnBP = 15.17e-3;    
    bgnCP = 5.07e-3;    
    inherit = &silicon_BI;    
    NMobility = &mos_N_mob;    
    PMobility = &mos_P_mob;    
};

/*
 *  SILICON CARBIDE DOPANT SPECIES
 */
APPENDIX B. SIC LIBRARY FILE

#define SPECIES(NAME,TYPE,TRAP,EA,NC,PC) 
  species NAME 
  { 
    type = TYPE; 
    trapping = TRAP; 
    energy = EA; 
    ncross = NC; 
    pcross = PC; 
  };

  SPECIES( A1_Si_1 , acceptor , false , 0.2 , 1.0e-15 , 1.0e-15 )
  SPECIES( A1_Si_2 , acceptor , false , 0.220 , 1.0e-15 , 1.0e-15 )
  SPECIES( N_Si , donor , false , 0.095 , 1.0e-15 , 1.0e-15 )
  SPECIES( Al_Si , acceptor , false , 0.2 , 1.0e-15,1.0e-15 )

/*
 * MOBILITY MODELS
 */
momodel mos_N_mob 
{ 
  /*
  * Acoustic Phonon (bulk):
  *   MA = mu0 (T/300)^a(m*/m0)^b
  */
  apType = "ap1";
  apAlpha = -1.5;
  apBeta = 0.0;
  apMu0 = 400;

  /*
  * Optical Phonon (bulk)
  *   NO = mu0 (T/300.0)^a
  */
  opType = "false";
  opAlpha = -3.13;
  opMu0 = 600;

  /*
  * Ionized Impurity (bulk):
  *   Caughey-Thomas Equation
  */
  iiType = "false";
  iiNo = 4.5e17;
  iiMu0 = 20;
  iiAlpha = 0.45;
  iiBeta = 1;
  iiGamma = 1;

  /*
    * Surface Phonon Effect:
    */
  spType = "false";
  spAlpha = 1.75;
  spBeta = -0.26;
  spPo = 0.09;
  spPi = 0;
  spZo = 1.73e-5;

  /*
  * Surface Roughness:
  */

67
APPENDIX B. SIC LIBRARY FILE

* MSR = mu0 E eff\^2
* /srType = "sr1";
srAlpha = 0.0;
srMu0 = 50;
*/
Coulomb:
* MC = mu0 (t/300)\^-1.5/(Na*(ln(1+g^\^-2)-g^\^-2/(1+g^\^-2)))
* g=nu0*(t/300)\^-a/n
*/
scType = "false";
scMu0 = 1.5e19;
scAlpha = 2;
scMu0 = 2e19;
*/
Velocity Saturation:
* M = MTOT / [ 1 + ( MTOT |Epara| / Vsat )\^-a ] - 1/a
*/
vsType = "vs1";
vsAlpha = 1.0;
*/
Saturation Velocity:
*/
svType = "sv1";
svMu0 = 4.64e7;
svAlpha = 0.8;
};

model mos_P_mob {  
/* Acoustic Phonon (bulk):
*  NA = mu0 (T/300)\^-a(m* /m0)\^-b
*/
apType = "ap1";
apAlpha = -1.5;
apBeta = 0.0;
apMu0 = 100;
*/
Optical Phonon (bulk)
* MO = mu0 (T/300.0)\^-a
*/
opType = "false";
opAlpha = -3.25;
opMu0 = 200;
*/
Ionized Impurity (bulk):
* MI = mu0 [ 1 + ( NO/NI ) (T/300) ]
*/
iiType = "false";
iiNO = 1.2e18;
iiMu0 = 1.8;
*/
Surface Phonon:
* MSP =
*/
spType = "false";
APPENDIX B. SIC LIBRARY FILE

spAlpha = 1.5;
spBeta = -0.3;
spP0 = 0.334;
spP1 = 3.14e-7;
spZ0 = 1.51e-5;

/*
 * Surface Roughness:
 *  MSR = mu0 Eeff^a
 */
srType = "sr1";
srAlpha = 0.0;
srMu0 = 50;

/*
 * Coulomb:
 *  MC = mu0 (t/300)^1.5/(Na*(ln(1+g^2)-g^2/(1+g^2)))
 *  g=n0*(t/300)^a/n
 */
sCType = "false";
scMu0 = 1.4e18;
scAlpha = -3.4;
scN0 = 8.4e16;

/*
 * Velocity Saturation:
 *  M = MTOT / [ 1 + ( MTOT |Epar| / Vsat )^a ] ^ 1/a
 */
vSType = "vs1";
vSAlpha = 1.0;

/*
 * Saturation Velocity:
 */
vSType = "sv1";
vSV0 = 4.64e7;
vSVAlpha = 0.8;

};
Vitae

Vickram R. Vathulya was born May 25, 1974 in Vellore, India to Mr. K. V. Ravikumar and Mrs. Anuradha Ravikumar. He went to the Indian Institute of Technology, Madras, India from August 1991 to May 1995 and graduated with a Bachelor's Degree in Electrical Engineering. He received admission to Lehigh University in Fall 1995 to pursue a Master's Degree in Electrical Engineering. He has been awarded a Sherman Fairchild Fellowship to pursue his PhD degree in Microelectronics at Lehigh University. His academic interests include semiconductor device fabrication and modeling, semiconductor power devices and electronic communications. He is a member of the Phi Beta Delta and Sigma Chi honor societies. He also plays tennis and practices the piano.
END
OF
TITLE