1995

An electrochemical capacitance-voltage technique for the determination of pseudomorphic high electron mobility transistor material parameters

Robert E. Leoni
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An Electrochemical Capacitance-Voltage Technique for the Determination...

October 8, 1995
AN ELECTROCHEMICAL CAPACITANCE-VOLTAGE TECHNIQUE FOR
THE DETERMINATION OF PSEUDOMORPHIC HIGH ELECTRON
MOBILITY TRANSISTOR MATERIAL PARAMETERS

by

Robert E. Leoni III

A Thesis
Presented to the Graduate and Research Committee
of Lehigh University
in Candidacy for the Degree of
Master of Science
in
Electrical Engineering

Lehigh University
August 30, 1995
This thesis is accepted and approved in partial fulfillment of the requirements for the Master of Science in Electrical Engineering.

8/14/95

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Acknowledgements

I would like to thank my advisor, Dr. James C. M. Hwang for his support, valuable suggestions, and guidance. The other members of the Compound Semiconductor Technology Lab have also been an enormous resource with their knowledge, understanding, encouragement, and moral support.

I extend loving thanks to my parents and brother for their complete support and confidence in me, and to my grandparents who helped to make my studies in electrical engineering possible. I also would like to thank my friends outside of the lab who were always willing to lend an ear and lift a pint.
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Abstract

A novel technique for the extraction of pseudomorphic high electron mobility transistor material parameters has been developed. The technique is based on a reverse engineering technique to iteratively solve for the desired parameters using both simulated and measured electrochemical capacitance-voltage data. Using this technique, the active planar doping efficiency of a pseudomorphic high electron mobility transistor structure was determined for the first time.
Chapter 1

Introduction

Material qualification through post growth characterization is an important step in semiconductor processing. Characterization is accomplished mainly through optical and electrical measurements such as photoluminescence, Hall, capacitance-voltage, and current-voltage techniques. Within the tolerance of measurement error, these results are taken directly as the material parameter values.

Of the many parameters that may be obtained through these techniques, the doping profile is the most important. The location and concentration of electrically active dopants critically affects the performance of devices which are processed from the material. Doping profile characterization is possible through capacitance-voltage (CV), spreading resistance, and secondary ion mass spectroscopy (SIMS) measurements. Spreading resistance measurements involve a lot of sample preparation and are highly dependent on the skill of the operator. SIMS measurements return values of impurity concentrations, regardless whether they are electrically active or not.

In comparison, CV measurements are readily accomplished and have a high degree of reproducibility from operator to operator and apparatus to apparatus. The main limitation of this technique is reverse breakdown. In a pseudomorphic high electron mobility transistor (PHEMT), the active doping layer is typically sandwiched between a highly doped contact layer and a semi-insulating substrate. As such,
breakdown occurs before the profile depth reaches the active doping layer. Even if the active doping layer is reached, the parasitic series resistance increases very rapidly. Also, conventional analysis of the CV measurement data relies on a one dimensional analytical solution which is not valid for modern devices such as PHEMT's.

By using a variation of the CV technique known as electrochemical capacitance-voltage (ECV) [1], it is possible to overcome the profile depth limitation. The measurement setup is similar to that used in conventional CV except that the Schottky contact is made through an electrolyte which doubles as an etchant. This way the profile depth can be increased by etching through the material instead of increasing the bias voltage.

In the present study, the ECV technique is used to overcome the profile depth limitations while a two dimensional numerical simulation based on device physics is used to account for the effect of heterojunctions and of parasitic resistances. The measurement and simulation results are then iteratively compared, and the material structure for the simulation is adjusted accordingly. In this manner the doping levels and layer thicknesses of PHEMT materials can be obtained.
Chapter 2

Theory of ECV Measurements

The basics of a conventional CV measurement are first reviewed in Section 2.1. The dual role of the electrolyte as a Schottky contact and an etchant is described in Section 2.2. The application of the ECV profiler to PHEMT materials is then discussed in Section 2.3.

2.1 One Dimensional Analytical Solution of Conventional CV Measurements

By definition, capacitance can be expressed as:

\[ C = \frac{Q}{V} \]

where \( C \) is the capacitance, \( Q \) is the accumulated charge, and \( V \) is the voltage across the capacitor. Capacitance is highly dependent on the geometry and the material parameters of the capacitor. Therefore it is useful to have certain prior knowledge of the basic geometry and material parameters. The parallel plate capacitor is a classic example. In this case, the capacitance for an area, \( A \), is given by the following expression:

\[ C = \frac{A \varepsilon}{W} \]

where \( \varepsilon \) is the dielectric of the material and \( W \) is the distance between the plates.

Similarly, when a potential difference exists between a semiconductor surface and its bulk, a depletion region is created. The capacitance in this case is determined by the distance between the surface contact and the depletion edge, under the depletion approximation. A more precise definition of the depletion edge would be the centroid
of the change of free carrier distribution as a result of the applied voltage. This centroid can be arrived at by solving Poisson's equation (and if necessary, Schroedinger's equation) for the expected dopant distribution and band structure.

Using Gauss's Law along with the capacitance derived with the depletion approximation the solution for the doping density, \( N_d(x_d) \), is obtained:

\[
N_d(x_d) = \frac{1}{q\varepsilon(x_d)A^2} \cdot \frac{C^3}{dC/dV}
\]

at the depletion depth:

\[
x_d = \frac{\varepsilon(x_d)}{C}
\]

which gives us a method of measuring the doping density of a material at the depletion depth (see [2] for a more detailed derivation). What is actually being measured as the doping density in this case is the electron concentration around the depletion width, but as long as the doping density and conduction band are slowly varying the electron concentration and doping profiles should coincide.

In actual CV measurements, the capacitance is measured by the current response of an AC signal which is superimposed on the DC bias voltage. If the AC signal is small compared to the DC bias, the capacitance can be treated as being approximately constant since the change in depletion depth is negligible. Thus from the initial definition of capacitance:

\[
C = \frac{I}{dV/dt}
\]
2.2 Electrochemical CV Profiling

The ability of an electrolyte to etch a semiconductor depends on the presence of holes. The dissolution reaction of GaAs is:

\[ \text{GaAs} + 6\Theta = \text{Ga}^{3+} + \text{As}^{3+} \]

Since PHEMT material involves only n-type layers that cannot be inverted electrically, it is necessary to generate holes through photonic generation of electron hole pairs. In this case the etch rate is determined by the intensity of the incident light.

The ECV technique profiles the material at a depth equal to the sum of the depletion depth and the current etch depth, \( W_r \), in the same way as in conventional CV. From Faraday’s Law of electrolysis we have:

\[ W_r = \frac{M}{6F\rho A} \int_0^t I dt \]

where \( M \) is the combined mass of Ga and As, \( F \) is Faraday’s constant, \( \rho \) is the density of the material, \( I \) is the current measured during dissolution, \( t \) is time, and the factor of 6 is for the total charge of an ionized/dissolved III-V pair.

2.3 Heterojunction Effects of PHEMT’s

While GaAs based devices are more expensive to process than their silicon based counterparts, there is a significant demand for them. Speed is their main selling point. The relatively higher speed comes from much higher electron mobilities, as well as the semi-insulating GaAs substrates, which reduce parasitic capacitance. Further increases in speed come from the use of heterojunctions.
The electron mobility is higher still in a heterojunction field effect transistor, such as the PHEMT. In the PHEMT, the electrons are physically separated from their ionized donors. This reduces Coulomb scattering and therefore increases the electron mobility. To facilitate this spatial transfer of electrons, a heterojunction is formed by epitaxially growing an n-doped wide band gap material (e.g. AlGaAs) on an undoped narrower band gap material (e.g. InGaAs).

The material structure of most PHEMT's currently produced is an InGaAs pseudomorphic channel grown on a series of GaAs and AlGaAs buffer layers. On top of the channel an AlGaAs layer is grown which contains a fraction of a monolayer of n-type dopant, known as the planar doped layer, offset slightly from the AlGaAs-InGaAs interface. Above the planar doped layer, the AlGaAs is doped on the order of $10^{17}$ cm$^{-3}$ and is known as the Schottky layer since the gate electrode of the PHEMT is deposited on it. Finally, a highly doped GaAs cap is grown on top of the Schottky layer so that ohmic contact can be made for the source and drain electrodes. This highly doped cap makes ECV profiling necessary. Figure 1 displays the structure and conduction band diagram of a typical low noise PHEMT. The structure will be the topic of discussion in later chapters.

The InGaAs channel of a PHEMT is usually on the order of 100 Å thick. This ensures that the electrons are confined to a small region, for broad peak transconductance and abrupt pinch off of the PHEMT. These electrons form a two dimensional gas and have certain discrete energies in the direction of epitaxial growth. To calculate the electron distribution in this type of structure, Poisson's and
Schroedinger’s equations must be solved simultaneously.

As discussed in Chapter 1, the sheet resistance of PHEMT material increases very rapidly as the depletion edge reaches the channel. To properly account for the parasitic resistance effect, a distributed network analysis must be performed.

The n-type dopant in AlGaAs is typically Si, which tends to self-compensate, especially in highly doped layers. This in combination with heterojunction effects makes the measurement of planar doping efficiency in PHEMT’s very challenging. It is also an important quantity to determine. Free charge donated by the planar doping layer transfers to both the channel and the Schottky layer and therefore there is an optimal level of doping efficiency that provides the desired device characteristics and ease of processing. This will be described in more detail in Chapter 5.
ECV Measurement for PHEMT Profile Extraction

An ECV profiler commercially available from BIO-RAD Laboratories, Model Number PN4300 [3], is the core of the measurement setup used to obtain the required data. The profiler consists of an HP 86 computer, an HP inkjet printer, an electronics box, an optical chassis, and the electrochemical cell. An HP BASIC program is provided by the vendor for instrumentation control. All communications between the computer and the electronics box are carried out via the general purpose interface bus (GPIB) IEEE Standard 488. The ECV subroutine is written to display and print out the doping concentration as a function of total depth (depletion plus etch depths).

3.1 Modifications to the ECV Profiling Program

BIO-RAD’s ECV program calculates the doping concentration based on the one-dimensional analytical solution under the depletion approximation. As discussed in Chapter 2, this solution is not valid for PHEMT’s. Therefore, the program was modified to directly output the capacitance and conductance data instead.

In order to save the data to file, it is necessary to change the capacitance and conductance variables to arrays of suitably defined dimensions. To save the information correctly, the line writing the information to the file needs to include the capacitance and conductance arrays with the proper index variable. Similarly, to print out the desired information the capacitance and conductance arrays must be added to
the print line, and the print format line needs to be updated accordingly. The print
tout became the desired form of output due to the incompatibility between the HP data
and the ASCII format.

3.2 Measurement Procedure

3.2.1 Sample preparation and mounting

A typical measurement begins with sample preparation. A new wafer sample is
scribed into the appropriate size in order to facilitate the mounting of the sample.
The part to be measured is placed on the vacuum chuck of a spin coater and vacuum
is applied. The spin controller is ramped up to approximately thirty rotations per
minute and acetone is sprayed on the surface for a half minute. Methanol is then
sprayed for another half minute followed by de-ionized water for three quarters of a
minute. Finally, nitrogen gas is used to remove the bulk of the residual liquid from
the sample. Vacuum is removed, and the sample is more thoroughly dried with the
nitrogen gas.

Prior to mounting the sample, the electrochemical cell should be washed with de-
ionized water to make certain no residual electrolyte is present. Particular attention
should be paid to washing the cell contacts since both electrolyte solution and solid
can be a source of leakage currents. The cell is then dried with nitrogen gas, making
especially certain that there is no water remaining around the sealing ring. Finally
the cell is replaced making sure the cylinder on the back side of the cell is fit snugly
in the optical chassis. Figure 2 is an illustration of the electrochemical cell.

The sample is then mounted to the electrochemical cell by pulling back the
plunger of the back contact assembly, holding the sample between the plunger and the
sealing ring, and then slowly allowing the plunger to push the sample against the
sealing ring. To avoid damage and to have reproducible areas of electrolyte contact
the plunger should only be gently pushing the sample against the sealing ring, but not
so lightly that electrolyte leakage is allowed to occur. Once the sample is in contact,
the outer edge of the sealing ring/semiconductor interface should be inspected for any
electrolyte leakage. Any leakage should be absorbed using a piece of paper towel,
and if the leak continues the sample should be remounted at another location on the
wafer.

3.2.2 Parasitic measurement and ohmic contact formation

Once the sample is situated correctly, the cell contact assembly should be lightly
snapped on to the cell contacts. Make certain the stop cock of the cell is closed and
fill the cell with the appropriate electrolyte. A 0.1 molar solution of tiron is an
appropriate choice of electrolyte for GaAs based structures having Al$_y$Ga$_{1-y}$As layers
with $y < 0.25$. The saturated calomel electrode is then attached to the cell contact
and placed in its holder in the cell.

The information about the sample should be entered in the profiler program and
then the values of the cable and feedthrough capacitances as well as the electrolyte
resistance should be measured using the routine supplied in the program. The cable
and feedthrough capacitances should be around 1200 and 14 pF respectively and the
electrolyte resistance should be about 120 Ω. If the cable capacitance or the
electrolyte resistance is high, check the cell contact assembly making sure there is
good contact and that no electrolyte is present on or between the contacts. If neither of them are the cause, the counter electrode is suspect and may need to be replaced. High feedthrough capacitance is also an indication of electrolyte between the contacts. High electrolyte resistances by itself indicates that either the solution doesn’t have a large enough concentration of tiron or that the solution is past its shelf life. In either case a new solution should be made.

Bubbles at the electrolyte/semiconductor interface will decrease the area of the Schottky contact and keep the affected region from being etched. Therefore it is necessary to remove bubbles from the interface by using the debubble routine in the profiler program in conjunction with a bulbed pipette. Once the bubbles are removed the front contact wires are connected to the front contact assembly. The contact routine of the profiler is then run, making certain the program is set to measure resistance through the front contacts instead of the back ones. If the measured resistance is not appropriate for the structure, around 300 to 400 $\Omega$ in both directions for PHEMT’s, the blast routine should be used to alloy the front contacts to the semiconductor. If the resistance is still too large after using the blast routine, the contact positions should be adjusted and the blast routine attempted again. If poor contact persists, the contacts should be retinned.

3.2.3 IV and CV measurements

Once electrical contact is made to the sample, diode characteristics of the electrolyte semiconductor system are taken using the IV routine of the profiler program. The first measurement is made with the lamp intensity set to zero. Biases
at which the current is zero are the regions that are candidates for ECV measurements. The bias range is predominantly on the negative region of the graph and sometimes just falls short of including zero bias for PHEMT material. The conventions of electrochemistry are different from those of device physics, so the negative bias range of the IV characteristics actually corresponds to forward biasing of the semiconductor.

The lamp is then set to half the full intensity and another IV measurement is taken. The biases at which the current is constant are candidates for the etch bias. Typically n-type material needs no etch bias. For lowly doped material, the current reaches a constant level and remains there for the whole range of biases, but highly doped material shows considerable amounts of current in the positive bias region of the IV graph (reverse biasing) due to leakage. Figure 3 shows the results of typical dark and light IV curves.

The dark IV data only gives a range of biases for the ECV measurement voltage. The CV measurement better pinpoints the bias to use while obtaining the ECV data. The bias ranges at which the conductance is low and the capacitance varies slowly should be used for the measurement voltage. Typical CV curves are shown in Figure 4. For the case shown in Figure 4, the optimum measurement bias is 0.

3.2.4 Etch profile

With the correct measurement and etch voltages determined, the ECV measurement can proceed through the ECV routine of the program. The maximum profile depth and etch step are chosen based on the structure being measured. Since
the active region of PHEMT's are so thin, typically a total depth of 0.2 µm and a step of 25 or 50 Å are used. The etch current should be kept between 0.75 and 1.5 Ma/cm². Too low of a current can cause uneven etching while too large of a current can cause etch depth overshoot.

Once all the measurement parameters are set, the profiler measurement is made. The modified program will print the capacitance and conductance at each measurement depth along with the depletion depth, total depth, conventionally calculated doping level, the dissipation factor among other less relevant pieces of information. After the measurement is done, the data file should be saved. The cell with the sample still in place should be taken to the sink and flushed of electrolyte by opening the stopcock. De-ionized water is used to rinse out the cell and then sample is removed taking care to make certain the plunger does not come in contact with the sealing ring when released. The sample should be rinsed and both it and the ECV cell should be dried with nitrogen gas.

3.3 Description of Sample

The sample used for demonstration of this new characterization technique is a low noise PHEMT obtained from Quantum Epitaxial Designs, Inc., run number 1683c.03. It was rejected as a deliverable wafer due to excessive concentrations of particles on the surface. These particles have no effect on the outcome of ECV measurements but can interfere with metalization processes. The structure's target widths, doping levels, and mole fractions have been included in Figure 1. The PHEMT material is GaAs based, contains one planar doped layer, has an n+ cap and an n Schottky layer.
Simulation of ECV Measurement and PHEMT Parameter Extraction

Simulation of an ECV measurement of a PHEMT inherently necessitates analysis in all three dimensions since the electrochemical cell lacks symmetry around the center of the sealing ring and the material changes significantly as a function of depth. To be completely exact the simulation should simultaneously solve the Poisson, Schroedinger, and continuity equations in all three dimensions for the appropriate measurement conditions at each etch depth. This type of analysis is currently unavailable due to the excessive amount of computing hardware necessary for the task.

The problem can be simplified according to the large geometry of the measurement setup. Since the Schottky contact is made over a 3.5 mm diameter circle while the etch depth is of the order of 1 \( \mu \text{m} \), the simulation can be broken into two parts, a one dimensional analysis transverse to the surface and a two dimensional analysis of the surface. The two parts will be discussed in Sections 4.1 and 4.2, respectively.

In order to extract as grown parameters from the data, a reverse modeling approach similar to that used to determine the doping profile of GaAs MESFET’s [4] was used. The extraction routine is discussed in Section 4.3.

4.1 One Dimensional Simulation

To simulate an ECV measurement it is necessary to determine the capacitance and
the sheet resistance of the material as a function of depth. These parameters are dependent on the electron concentration profile of the material. Thus the electron concentration is obtained first by simultaneously solve Poisson’s and Schroedinger’s equations.

A commercially available program, POSES [5], running on a SUN SparcStation IPC under a UNIX environment was used to solve the fore mentioned equations. Up to two thousand grid points are allowed in the calculation of electron concentrations and the grid may be set up with constant or varied spacings. The program makes the approximation that it is only necessary to solve for the Bloch wave functions in and around the channel. This leads to some error in the simulated results.

The electron concentration profiles of the structure are solved for etch depths that correspond to the measurement, with both the maximum and minimum small signal biases applied during the measurement. This gives two times the number of concentration profiles as there are number of etch depth measurements. Thinking of the results as a continuous function instead of a three dimensional matrix, we can represent the table of data as \( n(x,W,V_{\text{app}}) \) where \( x \) is position perpendicular to the surface and \( V_{\text{app}} \) is the applied bias. Conveniently, the program outputs an ASCII file when plotting the data which facilitates handling of the information.

The calculations of the electron concentration profiles use the built in potentials used for metals. Since the barrier height of GaAs based systems is effectively independent of the material placed on it, this is a fair assumption. The default parameters for band offsets, dielectric constants, and donor energy offsets are used in
the calculations.

The small signal capacitance can be rewritten in terms of the electron concentration profiles for a particular etch depth as:

\[ C(W_r) = \frac{q}{V_+ - V_-} \int_{0}^{\infty} [n(x, W_r, V_+) - n(x, W_r, V_-)] dx \]

\( V_+ \) and \( V_- \) are the DC bias plus and minus the amplitude of the AC signal respectively. The integral of the electron concentration difference is taken from zero, the surface, to infinity, the bulk GaAs. The result is the net concentration difference due to the varying bias which is proportional to the change in charge.

Sheet resistance is one over the product of mobility and free charge carriers. The expression for this is:

\[ R(W_r) = \frac{1}{\frac{q}{2} \int_{0}^{\infty} \mu(x) [n(x, W_r, V_+) + n(x, W_r, V_-)] dx} \]

Each etch depth should be calculated using the concentration profile at the average voltage, but that would add fifty percent more to the number of profiles. Since only a small bias variation is used, substituting the average of \( n(x, W_r, V_+) \) and \( n(x, W_r, V_-) \) is sufficient.

A C program has been written to post process the electron concentration profiles output by POSES. The program uses discrete representations of the previous two equations to calculate the sheet resistance and per unit area capacitance as a function of etch depth. The mobility values used in the calculations are either taken directly or are linear interpolations of data in current literature. Results are output to screen, but
can easily be redirected to file.

4.2 Two Dimensional Simulation

The two dimensional analysis incorporates the results of the one dimensional analysis along with additional passive elements in order to simulate the effect of parasitic resistance. This is accomplished by creating a square mesh representing the physical layout of the measurement system and connecting the nodes with the appropriate resistances and capacitances.

PSPICE [6], a commercially available circuit simulator, is used for the two dimensional analysis due to the ease of interfacing with the post-processed one dimensional data and due to its availability. The interfacing between POSES and PSPICE is done through a circuit file which is in an ASCII format. A DOS Quick BASIC program was written to create the first circuit file which was then transported to the Sun Sparcstation. Later circuit files were created using the UNIX program AWK which looks for specified ASCII representation in a file and outputs changes as specified. Once again, UNIX’s ability to redirect output makes it simple to save changes to a file.

In order to represent the distributed nature of the measurement, a large mesh is necessary. Studies were done to investigate the dependence of simulation results on the mesh size. The limitation on size set by the program is five thousand nodes. The study showed that a fifty by fifty node mesh would be sufficient. The mesh is created so that there are two tenths of a millimeter between each nearest neighbor node, making fifty nodes equal to a centimeter. The three and a half millimeter diameter
Schottky contact is horizontally located in the middle and vertically off center towards the top. The ohmic contact is placed one millimeter below the Schottky contact. Although there are actually two contacts in the measurement system, they both have been lumped together. Also, the ohmic contact position varies from measurement to measurement but this only has a slight effect on the contact resistance value so the exact contact position in the circuit file is not entirely important.

A network representation of the intrinsic element layout of such a mesh is illustrated in Figure 5. Nodes within the area of the Schottky contact are interconnected with the sheet resistance values for the particular etch depth being simulated. Other nodes have the unetched sheet resistance connecting them. The unit area capacitance is placed between the nodes within the Schottky contact and the voltage supply. A fixed capacitance is added to the unit area capacitance and a leakage resistance is added between the supply and the nodes within the Schottky contact. The leakage resistance, additional capacitance, and ohmic contact resistance values are obtained from the data of the ECV measurement, contactless sheet resistance, and contact formation measurements.

4.3 Extraction Routine

Sections 4.1 and 4.2 describe the steps necessary for the simulation of an ECV measurement. In order to extract parameters, comparisons need to be made between the simulation and the measured results. From this comparison and a knowledge of the effects of different parameters on the measured values, the parameters can be updated and the simulation run again. In this manner the parameters are iteratively
arrived at. Figure 6 is a flowchart of the extraction routine.

To extract the desired parameters, an initial value for them must be determined. This will be described in Section 4.3.1. The parasitic element values must then be determined which is described in Section 4.3.2. Finally, the simulation is run and rerun until the logic of the parameter extraction has been fulfilled. Description of the logic sequence is in Section 4.3.3.

4.3.1 Initial value determination

All of the material parameters are set to the target values supplied with the sample except for those to be extracted. Active planar doping level is a prime example of a parameter to extract. The target value is quite possibly the correct amount of silicon atoms present, but it is not the net amount of free charge supplied by the dopants, which is the electrically important quantity.

In order to determine an initial value, simulation studies of the dependence of the some salient feature of the small signal capacitance and conductance on the parameter are carried out. An example of such a feature is the etch depth difference between the decrease in capacitance at the n+ cap Schottky layer junction and the capacitance peak due to the channel electrons. The overall functional dependence is linearized over the range of possible values for ease of calculation and then the function is inverted so that the parameter is the dependent variable (e.g. the fore mentioned etch depth difference as a function of planar doping level is investigated, linearized, and then inverted so that we have doping density as a function of etch depth difference). Using the measured results as the independent value then gives an estimate of the
parameter. In developing the function for this estimate, the small signal feature used should be independent of the parasitic elements.

4.3.2 Parasitic element extraction

The additional capacitance, leakage resistance for the cap, and the contact resistance must be obtained from the capacitance and conductance data measured for the cap. A unique solution is impossible, but with the added information of the sheet resistance, measured by QED using a contactless eddy current system, along with the contact to contact resistances measured by the ECV profiler during ohmic formation, the contact resistance can be independently determined. Knowing the diameter of a front contact, \( a \), and the distance between the two front contacts, \( D \), the relationship between the capacitance and this geometry, illustrated in Figure 7, can be determined [7]:

\[
C = \frac{\pi \epsilon}{\cosh^{-1}\left(\frac{D}{2a}\right)}
\]

The resistance can then be obtained through the basic relationship:

\[
R = \frac{\rho D}{C}
\]

Taking the resistivity, \( \rho \), to be the product of the sheet resistance and the centroid of conductivity, estimating the alloying to penetrate to the centroid of conductivity, and assuming the contact resistance for each contact is the same, the lumped contact resistance of the two contacts is determined to be:

\[
R_c = \frac{1}{4} \left( R_{\text{meas}} - \frac{R_{\text{c}}}{\pi} \cosh^{-1}\left(\frac{D}{2a}\right) \right)
\]
where $R_{\text{meas}}$ is the resistance measured during contact formation and $R_{\text{f}}$ is the sheet resistance.

With the contact resistance approximated, a simulation of the ECV measurement is run for the case of zero etch. A UNIX script is used to iteratively update the leakage resistance and additional capacitance until the resulting simulated small signal conductance and capacitance are equal to the measured values within some tolerance. Updated parasitic element values are determined from the linearization of studies done on the effect of variations of the elements on the final results and are calculated using a C program.

After the script has determined the parasitic elements for zero etch, it is used three more times to determine the parasitics at different etch depths. Since the electron concentration level decreases significantly after etching through the cap layer, it is expected that the leakage resistance should increase. The three etch depths chosen are therefore past the cap layer. The additional capacitance is attributed to the measurement system and therefore shouldn’t change as the material is etched through.

Once the six new values have been determined and there is not much variation between them, an average value is calculated. The average capacitance is then compared to that obtained from the zero etch simulation. If the values are fairly close, to within a 0.01 uF/cm², the parasitic elements have all been determined. However, if the capacitances are not close, the contact resistance is modified and the whole parasitic extraction is run again until the capacitances are in agreement.
4.3.3 Extraction logic

With the initial parameter values for the material structure and parasitics determined, extraction can begin. The one dimensional and two dimensional simulations are carried out. Alignment of the simulated to the measured data is the next operation to be performed since the measured cap thickness is not the grown cap thickness. Before starting an ECV profile, some deposition of electrolyte or erosion of semiconductor ions occurs due to the measurement of the diode IV and CV characteristics. The best feature to align to is the drop in small signal capacitance and conductance that occurs as the etch profile passes from the cap into the Schottky layer.

Two C programs have been written to calculate the best shift of the simulated profile edge to the measured edge and adjust the profile. The first program calculates the error between the two profiles around the capacitance drop off, using triangulation to determine the best shift value. This value is then passed to the second program which linearly interpolates between simulated points to update the simulated ECV data.

Error between the simulated and measured data is then quantified. The value of the weighting factor for each etch depth in the error calculation depends on the parameter being extracted and is determined through simulation studies or physical understanding. For instance, to extract the thicknesses and doping levels of two uniformly doped epilayers it would be best to use the etch depth necessary reach the epilayer junctions and the capacitance levels of the epilayers as indicators. Therefore
more weight should be given to the inflection points in the capacitance for the thicknesses and the mid regions of the epilayers should be weighted more heavily for the doping levels. A Poisson equation solver could be used to determine the dependence of the capacitance profile on the doping levels and layer thicknesses, the results of which would be used in the update procedure. Another valid approach in this case would be to use the depletion approximation to revise the doping levels and thicknesses. A C program checks whether the error values are within tolerance or has reached a minimum and accordingly the extraction is either completed or the error value is used to update the parameter and the extraction continued.
Chapter 5
Results and Discussion of Planar Doping Level Extraction

The low noise PHEMT structure described in Section 3.3 was measured using the Polaron Profiler with the program modifications discussed in Section 3.1. The results of this measurement are discussed in Section 5.1. Extraction of the planar doping level was carried out, and the results are addressed in Section 5.2. Section 5.3 contains a discussion of the results.

5.1 Measurement Results

The measurement of structure 1683c.03 resulted in typical PHEMT measured doping profile and small signal characteristic curves (see Figure 8 for the doping profile and Figure 9 for the small signal characteristics). An average contact to contact resistance of 350 $\Omega$ was obtained. The necessary measurement and etch biases of -0.3 V and 0 V respectively were determined from the IV and CV characteristics. A lamp intensity of 64 percent of full was used in order to etch at a suitable rate with 50 Å intervals between measurements.

The capacitance curve shows a relatively large constant value as the cap layer is profiled through, as is to be expected due to the constant doping level. The capacitance tails off as the depletion edge passes from the n$^+$ cap layer into the n GaAs layer. Using the doping level for the n layer, 5.0x10$^{17}$ cm$^{-3}$, a built in potential of 0.7 V, and the depletion approximation we arrive at a depletion width of 450 Å. This means that if no band discontinuity existed between the n GaAs and the n
AIGaAs Schottky layers, the depletion edge would reach into the Schottky layer by the time the entire cap layer was etched away. Due to the band discontinuity between the two layers, there is an accumulation of electrons on the GaAs side of the discontinuity. This discontinuity and accumulation of electrons is the reason for the slight leveling in capacitance after the initial decrease. The depletion edge makes its way through the cap/Schottky interface which causes the capacitance to decrease slightly due to the built in depletion on the Schottky layer side of the interface. The capacitance then increases due to the charge donated by the planar doping layer. This charge resides mainly in the channel, but there is also some in the Schottky layer. Finally the capacitance drops off to zero as the channel is completely pinched off.

The conductance profile is very similar to the capacitance profile in over-all shape except the drop off in conductance from the cap value is accentuated. The eventual increase in the conductance is somewhat unsettling. Conductances are typically a function of total charge, so as the material is profiled through one would expect the curve to be monotonically decreasing. The form of the profile is due to the way in which the information is represented. The measurement system reports a capacitance and a conductance that are based on a parallel RC equivalent circuit, but a better representation of the system is a series equivalent circuit.

5.2 Extraction Results

The extraction of the planar doping level of structure 1683c.03 was carried out in the manner outlined in Section 4.3. A contact resistance of 55 Ω was calculated. The parasitic extraction resulted in an added capacitance of 0.3 μF/cm² and leakage
resistances of 1000 and 4300 MΩ/cm² for the cap and deeper etches respectively.

The etch depth difference between the roll off of the cap capacitance and the roll off of the channel capacitance was chosen for the simulation study done on the planar doping level. The study showed the relationship between the simulated measurement and the doping level to be highly sublinear. The initial level was calculated to be 7.5x10¹¹ cm⁻² using the linearization.

A triangulation routine was used for the extraction. It adjusts the doping level according to the total error between the measured and simulated current amplitudes and makes judgements based on the present and minimum error values. Initially the doping level is set to increase by 1.0x10¹² cm⁻² intervals and the minimum error was set to an unattainably high value. In this scheme the new error is compared to the minimum error value obtained so far. If the new error is larger than the minimum error, then the increment value is halved and the sign of the interval is changed. If it is smaller than the minimum value, the present doping level is set as the best value and the parameter is increased or decreased according to the sign of the increment. Once the increment value becomes less than 1.25x10¹¹ cm⁻², the extraction is determined to be complete. The final result reached with such a technique is a planar doping level of 1.5x10¹² cm⁻². The simulated and measured capacitances are displayed in Figure 10 while the conductances are displayed in Figure 11.

5.3 Discussion

The results of the extraction routine show the active planar doping level to be almost one third of the target value. This difference is attributed to self compensation
of silicon. This electrically important value has not been determined through any other technique. SIMS only reports the total number of atoms present. Spreading resistance and Hall measurements can effectively determine the amount of charge in the channel, but are incapable of measuring the charge donated by the planar doping layer to the Schottky layer due to the extremely low mobility of AlGaAs. Conventional CV and ECV techniques are able to describe amounts of charge in the various layers of the structure, but this cannot be correlated with the planar doping level without an extraction routine.

The results of room temperature Hall measurements were available from QED, and the measured channel electron concentration is reportedly $1.7 \times 10^{12} \text{ cm}^{-2}$. Integration of the simulated channel electron concentration using the extracted planar doping level also resulted in a value of $1.7 \times 10^{12} \text{ cm}^{-2}$. The Hall measurement therefore verifies the results of the planar doping level extraction.

The importance of the amount of charge donated to the Schottky layer can be illuminated through further discussion of ECV and other simulations. Based on the simulations run for the initial parameter determination, shown in Figures 12 and 13, one sees a large difference between the results of a 5.0, 2.5, and $1.0 \times 10^{12} \text{ cm}^{-2}$ doped samples. In comparing the high and low doping cases, we see that much more of the material must be etched through before the channel is contacted in the highly doped case. However, once contacted, the charge is swept out much more quickly. The reason for this difference is the screening of the charge in the channel by the additional charge placed in the Schottky layer. If the sole effect of larger planar
doping level activation was additional charge in the channel, the channels should be contacted at roughly the same etch depths.

Simulations of the gate recess etch process in which the ungated source-drain current is monitored as a function of etch depth show a strong dependence on the planar doping level and explain the discrepancies between materials described in [8] (see Figure 14). As expected, the larger the planar doping level, the higher the initial current level. This increase in current is due to the additional charge donated to channel by the planar doping level. In the gate recess process, etching is typically continued until the channel is just beginning to be pinched off, which is the final roll off of the current. From the simulations we see that too high of a planar doping level will give an abrupt decrease in channel current and therefore make the process difficult to control. This is an undesirable quality which is caused by the charge donated to the Schottky layer by the planar doping layer.

Simulations of the transconductance of a device constructed from this structure also show a strong dependence on planar doping level (see Figure 15). The larger the level, the larger the transconductance peak and smaller the transconductance width. The decrease in the width of the transconductance with planar doping level is once again due to the additional charge donated to the Schottky layer. The increase in the peak transconductance is mainly due to charge added to the channel.
Chapter 6

Conclusions

A technique for the extraction of PHEMT structure parameters has been developed. The extraction iteratively simulates ECV data and compares it to measured results, updating the simulation until it converges to a final structure. The extraction of the active planar doping level of PHEMT structure 1683c.03 was used as a test vehicle, and verification of the extracted result was obtained through a comparison between Hall and simulated channel charges. By virtue of the reverse engineering scheme used, the extraction is able to resolve details that measurements are not capable of determining.
Chapter 7

Future Work

Having extracted the planar doping level of a low noise PHEMT structure, it is natural to extend the range of studies to power PHEMT’s, which have two planar doping levels, bulk doped PHEMT’s, which have no planar doping levels, and MESFET’s. Also the extraction of other parameters such as actual thicknesses, mole fractions, and mobilities are possibilities depending on the electrical sensitivity of the given structure to the parameters. Additional information may also be obtained for extraction of parameters by simultaneously measuring an ungated FET current along with the small signal Schottky diode capacitance and conductance.

Extractions of parameters of many more structures should be made in order to optimize the update logic in the extraction routine. Also, by developing a C program that solves large matrices, PSPICE could be bypassed which would cut down on calculation time. Finally, in order to obtain more exact results, either a post processing program to solve Schroedinger’s equation over other potential wells should be developed in C, or a program that solves Poisson’s and Schroedinger’s equations over the entire structure should be substituted for POSES.
References


Figure 1. Target parameters and Conduction band diagram of structure 1683c.03.
Figure 2. Electrochemical cell.
Figure 3. Dark and illuminated Schottky diode IV characteristics.
Figure 4. Small signal capacitance and conductance characteristics of a Schottky diode.
Figure 5. Distributed network for two dimensional analysis.
Figure 6. Extraction routine flowchart.
Figure 7. Ohmic contact geometry.
Figure 8. Measured doping concentration profile calculated using the conventional capacitance-voltage analysis.
Figure 9. Measured conductance and capacitance profiles.
Figure 10. Comparison of simulated and measured capacitance profiles.
Figure 11. Comparison of simulated and measured conductance profiles.
Figure 12. Simulated small signal capacitance with planar doping level as a parameter.
Figure 13. Simulated small signal conductance with planar doping level as a parameter.
Figure 14. Simulated saturation current measurement during gate recess etch process with planar doping level as a parameter.
Figure 15. Simulated PHEMT transconductance with planar doping as a parameter."
Vita

Robert E. Leoni III was born in DeLand, Florida on February 3, 1970. He obtained Bachelor of Science degrees in both Electrical Engineering and Engineering Physics from Lehigh University by January 1993. Before starting his current graduate studies at Lehigh University, he worked for Dr. Y. Kim in the Lehigh University Physics Department as a research assistant. Since the fall of 1993 he has worked in the area of microwave device material characterization at the Compound Semi-conductor Technology Laboratory. For a ten week period in the summer of 1994 he worked at the Aerospace Corporation in El Segundo, California as an associate member of technical staff.

Publications


Presentations


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