Data quantizer integrated circuit for fiber-optic data link applications

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DATA QUANTIZER INTEGRATED CIRCUIT FOR FIBER-OPTIC DATA LINK APPLICATIONS

by

Edward Eugene Campbell

A Thesis
Presented to the Graduate Committee
of Lehigh University
in Candidacy for the Degree of
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in
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December 5, 1991
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Most importantly, I dedicate this thesis to my newlywed wife Lori for her love, patience, and sacrifice during this period.

I also dedicate this thesis to my mother Marilyn K. Baker. For with her love, support, and encouragement, my many years of academic pursuits became possible.
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ABSTRACT

The design of a modular data quantizer circuit for fiber-optic data link receiver applications is described. The circuit converts small analog pulses from a preamp to digital ECL output levels.

The circuit provides 60dB of gain at a -3dB bandwidth of 160MHz, through wide-band linear differential amplifier stages. This gives the circuit an input sensitivity of 1.8mV, for good overall receiver sensitivity. It has a wide dynamic input range of 58dB. This will accommodate a variety of optical network configurations, where the input power to the receiver varies, depending on how close it is to the transmitted optical signal.

Low input offsets of <1mV are achieved through a transconductance amplifier configured in a DC feedback loop. This provides auto-zero cancellation of input offsets. Additional features include AC or DC coupling, an output disable circuit which latches the data outputs in the absence of an input signal. This eliminates output "chatter". Also, a link monitor flag circuit gives an indication of the presence of an input signal.

The circuit is fabricated in AT&T's Microwave Complementary Bipolar Integrated Circuit (CBIC-U) technology, and operates from a single 5V power supply. Bit error rate, sensitivity, and eye diagram measurements have shown satisfactory performance at data bit rates of up to 600Mb/s.
CHAPTER 1

INTRODUCTION

1.1 Historical Review & Optical Receiver Application

Fiber optics is becoming the technology of choice for telecommunication systems. Advances in lightwave components and implementation of new standards, such as Fiber Distributed Data Interface (FDDI) and Synchronous Optical Network (SONET), are having a substantial effect on short and long-haul networks. Traditional copper-based systems face inherent bandwidth limitations and EMI/RFI problems. These systems also have a definite weight and size disadvantage in the cables. Optical fibers need only a fraction of the space that copper-coax cables require.

Due to the tremendous bandwidths offered by optical fiber communication systems, the optoelectronic devices and electronic circuits that supply and receive data are becoming the focus of attention for higher bandwidths and improved noise sensitivity. The electronic and optoelectronic interfaces are what limit the system data bit rates. A basic optical fiber communication system is composed of a transmitter, optical fiber, and the receiver.

The system bandwidth is primarily determined by the receiver. Dynamic range and sensitivity are other parameters associated with the receiver. Four principal functions of the optical receiver are [1]:

2
Photodetection - conversion of an optical signal into an electrical signal containing the information being communicated, which can be extracted.

Amplification - increasing the amplitude of the electrical signal from the photodetector to the levels necessary for effective utilization of the signal.

Filtering - limiting the bandwidth of the receiver to what is required for the signal spectrum and designing the frequency response $H(j\omega)$ of the receiver in order to optimize its performance.

Signal Processing - processing the amplified and filtered signal to provide the proper output signal characteristics or interface needed by the user.

Therefore, an optical receiver contains a photodetector, which will convert a normally weak optical signal into a correspondingly weak electrical signal, and subsequent amplification and signal processing stages that produce an electrical signal of sufficient power and impedance level to convey the transmitted information to the system user.

A receiver photodetector is actually composed of a photodiode, either a PiN diode or an avalanche photodiode (APD), and the first electronic circuit stage, known as the preamp. Since the output of the photodiode with applied light is a current, a transimpedance amplifier is predominantly used as the preamp, giving a small voltage signal output. A very basic block diagram of an optical receiver is shown in Figure 1.1 The voltage from the preamp is coupled into the decision circuit. AC or DC coupling can be used, depending on the application. The photodiode and preamplifier are commonly referred to as the receiver "front end," and the decision circuit and subsequent stages are referred to as the "back end." The design of the preamplifier is usually such that noise produced in subsequent circuit stages has a negligible effect on the overall receiver signal-to-noise ratio (S/N).
Sensitivity is usually defined as the minimum received signal power, such that the output signal has a bit error rate (BER) of $< 10^9$ for intensity modulated optical signals, otherwise known as ON/OFF keying (OOK) [2]. This is similar to pulse code modulation (PCM) of analog signals. It is usually expressed in dBm and is a negative number, meaning that the sensitivity is less than 1mW. The noise produced in the receiver will tend to mask small signals, thereby increasing the minimum input power required. Improved sensitivity is equivalent to a lower minimum signal power needed for the BER requirements.

The total noise is dominated by thermal noise, and is therefore directly proportional to the bandwidth of the preamp. This would suggest that bandwidth should be kept to a minimum for better S/N ratio. However, smaller bandwidths will result in slower rise times and spreading of the pulse shape to the point where the successive pulses start to overlap. Now the receiver may not be able to
distinguish between them, and binary 1/0 decision errors will result. This interference between adjacent pulses is known as intersymbol interference (ISI), and is inversely proportional to bandwidth. Optimum preamp bandwidth design is a trade-off between ISI and S/N or sensitivity [3]. Improvements in sensitivity for an optical fiber system are obtainable through the use of an APD, with carrier multiplication. This would be used instead of a PiN diode in the photodetector part of the receiver. Other improvements will be obtained ultimately with the development of coherent optical communication techniques, which is similar to superheterodyne detection in radio communications. However, these improvements also have increased cost associated with them.

Although the receiver sensitivity is primarily determined by the photodetector/preamp stage, the data decision point occurs in the comparator or decision circuit stage. The decision circuit usually will have its threshold level set so that there is an equal probability of error for HI and LO logic level decisions in the output signal. Amplification and filtering stages are also present in this section of the receiver.

Because noise is a random variable, an exact value of the noise at a specific time cannot be determined. When the noise is combined with the signal, the range of values of signal plus noise which represents a binary 1 will overlap the range for just the noise alone, which represents a binary 0. Because of this, decision errors cannot be reduced to zero.

Optical data link (ODL) transmitters and receivers are designed to be low-cost communication systems for shorter distances (~2Km). These low-cost receivers often use asynchronous detection without built-in clock recovery or retiming circuits. Clock recovery is more critical to longer distance regenerative systems such as undersea fibers. Here, the clock recovery circuit retimes the logic
transitions of the outputs to remove phase noise or jitter which occurs over the longer distances due to factors such as dispersion due to the optical fiber, pulse width distortion, and timing jitter. Without retiming of the data, the jitter problems would be additive at each regeneration of the signal. For the ODL receiver, the decision circuit outputs are used directly as the data outputs. Historical advances in ODLs have seen bit rates increase from 50Mb/s to greater than 200Mb/s, as well as data links designed to meet FDDI and SONET standards.

Monolithic integration is essential for these optical receivers to achieve small, highly reliable circuits with low power dissipation and improved speed [4]. The decision circuits in the ODLs utilize wide-band differential amplifiers. Higher bit rate receivers, on the order of a few gigabit/s, tend to use digital D flip-flop circuits [5]. Most decision circuit or comparator outputs are ECL or TTL compatible. Usually, comparators with ECL outputs have faster response time than those with TTL outputs [6].

1.2 Scope of Thesis

This Thesis presents a modular approach to the back end decision circuit or data quantizer circuit, implemented in a separate integrated circuit (IC) chip. This allows flexibility in matching different front end circuits to the back end circuit. Also, separate front end and back end ICs have improved stability implications due to a reduction in parasitic feedback paths. Figure 1.2 shows the partitioning between the front and back end circuits in the ODL receiver. The data quantizer section contains the decision circuit, along with the data link status monitor circuits. The link status monitor basically is a wide-band full-wave rectifier circuit with ECL outputs. It gives an indication of the presence of an optical signal, as opposed to monitoring if the receiver performance is meeting a BER requirement, which
usually is $< 1$ error per $10^9$ data bits. The circuit directly interfaces with the clock recovery circuit, as indicated in Figure 1.2.

The output from the preamplifier is coupled into the decision circuit, which basically is comprised of cascaded stages of wide-band linear amplifiers. These provide up to 60dB of gain, amplifying the front end signal to the level needed for the ECL DATA outputs. The logic level voltage swing of these outputs is $\sim 800\text{mV}_{\text{P-P}}$. The circuit input accepts a wide dynamic range of signal strengths ($>55\text{dB}$). This is needed for the typically large range of output voltage from the preamp which can be as small as $2\text{mV}_{\text{P-P}}$, and $>1.2\text{V}_{\text{P-P}}$. 

Figure 1.2: Modularity concept in receiver partitioning
A transconductance amplifier is available for configuring in a feedback loop. Used with an external bypass capacitor, the circuit provides DC feedback for auto-zero input offset cancellation.

Other existing decision circuits, such as those by Micro Linear and Signetics, are limited to 100 Mbaud data rates. The data quantizer, of this thesis, is designed to operate at higher data rates. The circuit has been characterized at 600 Mbaud with satisfactory performance. The circuit was implemented as a redesign of an existing one chip receiver IC comprised of both front end and back end circuits. The components from the front end circuits were utilized to add some of the above mentioned features to the existing decision circuit, as well as making it a more modular design.

This work will concentrate on the frequency response of the data path, along with a complete design analysis of the sub-circuits in the feedback loop. Both open and closed loop frequency response of the circuit will be evaluated. Because of the modularity concept of the circuit, different input configurations can be compared, such as DC coupling of the preamp and decision circuits versus AC coupling. Circuit simulations will be presented for comparison to theoretical results. Packaged IC models have been characterized to access the design performance.
CHAPTER 2

DESIGN CRITERIA & THEORY

2.1 Block-Level Design

2.1.1 Data Quantizer Circuit Topology

Regardless of the actual circuits used as a solution in making up the optical receiver, there are primary functions that the circuits must perform. As previously mentioned, these are amplification and signal processing of the photodetector signal. This circuit uses wide-band linear differential amplifiers to perform asynchronous detection of the signal. That is, the circuit performs a conversion of the variable amplitude, analog preamp signal to a digital logic level swing. This is illustrated in Figure 2.1. The use of complementary signals offers good rejection to common mode noise.

The design of the data channel represents an optimization of bandwidth, propagation delay, and power dissipation parameters [7]. Specifically, this becomes the question; for a given overall voltage gain, what is the number of gain stages and what is the gain of each stage to be used for optimization of the parameters. It is well known that the overall bandwidth of the system will decrease exponentially as the number of gain stages increases
linearly. Usually, circuits reported in the literature for speed optimization do not include power dissipation constraints. However, for realistic circuits this is an important parameter. The following analysis provides a derivation of the number of gain stages to be used for optimization of the design parameters [8].

Referring to Figure 2.1, it is assumed that the amplifier chain consists of n identical, non-interacting stages. This means that the input impedance is infinite and the output impedance is = 0. This approximation is reasonable for this level of analysis. The desired dynamic range of input signal is such that only the last or output stage operates in the non-linear range, with the previous amplifiers being linear. This provides a minimum of propagation delay with fast rise and fall times of the output signal from the overdriven stage. The total system gain $A_v$ is equal to the product of the individual stage gains. The individual stage gain $A_x$ is found by

$$A_v = A_1 * A_2 * \ldots * A_n \Rightarrow A_x = A_v^{1/n}$$

(2.1)
Each individual gain can be expressed as a product of a transconductance $GM_x$ that is proportional to the amplifier supply current $i_x$ and a resistance $R_x$ as shown below

$$A_x = GM_x R_x = \frac{i_x}{V_k} R_x$$  \hspace{1cm} (2.2)

The proportionality constant is $1/V_k$. To a first order, the frequency response of each individual amplifier can be assumed to be determined by a single dominant pole or time constant $t_x$ which is equal to the resistance $R_x$ and a lumped capacitance $C_x$ as shown below

$$t_x = R_x C_x$$  \hspace{1cm} (2.3)

Equations (2.2) and (2.3) can now be combined to give the time constant of the amplifier in terms of its gain as follows

$$t_x = \frac{A_x}{GM_x} C_x = t_o A_x = t_o A V^{1/n}$$  \hspace{1cm} (2.4)

where,

$$t_o = \frac{1}{GM_x} C_x = \frac{V_k}{I_x} C_x$$  \hspace{1cm} (2.5)

The total supply current $I_{cc}$ for $n$ stages can be approximated by

$$I_{cc} = n i_x \Rightarrow i_x = \frac{I_{cc}}{n}$$  \hspace{1cm} (2.6)

and equations (2.5) and (2.6) can be combined to give

$$t_o = n \frac{V_k}{I_{cc}} C_x = n t_o$$  \hspace{1cm} (2.7)
where,

\[ t_o' = \frac{v_k}{I_{CC} C_x} \]  \hspace{1cm} (2.8)

Intuitively, the total system propagation delay \( t_t \) through \( n \) stages, is equal to the sum of the individual time constants as shown below

\[ t_t = nt_x \]  \hspace{1cm} (2.9)

This is a good approximation for a large number of stages; however, there is some error for \(<5\) stages. Although, for insight into the design optimization, equation (2.9) is accurate enough without making the math unnecessarily tedious. Now, an expression for the total system propagation delay as a function of \( n \)-number of stages can be obtained by a combination of equations (2.4), (2.7), and (2.9)

\[ t_t = n A_v^{1/n} t_o = n^2 A_v^{1/n} t_o' \]  \hspace{1cm} (2.10)

Equation (2.10) is shown plotted in Figure 2.2 as propagation delay, normalized to a particular value of \( t_o' \), versus the number of gain stages \( n \) for different values of gain. It can be seen that the propagation delay decreases to a minimum value, then increases for either a smaller or larger number of gain stages.

The relative minimum for propagation delay can be found by differentiating (2.10) with respect to \( n \), this gives

\[ \frac{dt}{dn} = t_o' \left( 2n A_v^{1/n} - \frac{n^2 A_v^{1/n} \ln(A_v)}{n^2} \right) \]  \hspace{1cm} \rightarrow

\[ \frac{dn}{dn} = t_o' A_v^{1/n} (2n - \ln(A_v)) \]  \hspace{1cm} (2.11)

setting the derivative equal to 0 and solving for \( n \) results in,

\[ n_{opt} = \frac{\ln(A_v)}{2} \]  \hspace{1cm} (2.12)
Now, with an expression for the optimum number of stages, the optimum gain of each stage for minimum propagation delay can be found. From (2.1) and (2.12),

\[
A_{x(\text{opt.})} = A_v^{1/n_{\text{opt.}}} = A_v^{2/\ln(A_v)} \quad => \\
\ln(A_{x(\text{opt.})}) = \frac{2\ln(A_v)}{\ln(A_v)} = 2 \quad => \\
A_{x(\text{opt.})} = e^2 = 7.389
\]  

(2.13)

Therefore, the optimum gain for each stage is a fixed value, and the optimum number of gain stages for minimum propagation delay can be found from (2.12) as shown in Figure 2.2.
2.1.2 Open Loop Gain

To amplify small signals from the preamp, that are on the order of 1mV \( p-p \) to the 800mV ECL output swing, a total gain of \( \sim 60\text{dB} \) is needed. For minimum propagation delay, equation (2.12) can be used to give the optimum number of individual gain stages. This results in \( n_{\text{opt.}} = 3.45 \) stages. Obviously, the number of stages used must be a whole number. Referring to the curve in Figure 2.2, going to a smaller than optimum number of stages results in a sharp increase in the propagation delay. Going to a larger than optimum number of stages gives a more gradual increase in the propagation delay. Therefore, this circuit basically uses 4 gain stages, each with \( A_x \approx 15\text{dB} \).

2.1.3 Input Sensitivity

If the effects of noise could be neglected, then the input sensitivity or minimum detectable signal would be determined by the total gain of the amplifier stages. Characterization of an available front end preamplifier circuit showed the typical RMS noise voltage \( \sigma = 0.9\text{mV} \). A range for \( \sigma \) of between 0.8mV and 1.5mV was predicted by ADVICE computer simulations [9]. Even if the back end circuit could detect signals smaller than about 1mV, they would be swamped by the front end noise, resulting in a poor signal-to-noise ratio. Experience with the original receiver IC shows the input referred noise for the decision circuit to be \( <60\mu\text{V} \) RMS. Clearly, the signal-to-noise ratio is determined by the front end noise. Low noise characteristics requires that devices with poor noise characteristics, such as zener diodes, active loads, and large value resistors, must not be used in the signal path [10].
2.1.4 Wide Dynamic Range

The strength of the optical signal delivered to the receiver depends on the attenuation that occurs in the optical fiber. The amount of attenuation is directly related to the length of fiber between the transmitter and receiver. The dynamic range of the fiber optic system will primarily be determined by the receiver front end as long as the decision circuit can accept an input range that is greater than the complete range of output voltage from the preamp. To satisfy these conditions, it is desirable the input dynamic range be \( > 55 \text{dB} \). This is a range from \( 2 \text{mV}_{p-p} \) to larger than \( 1.2 \text{V}_{p-p} \).

For small input signals, the decision circuit must provide full amplification for the required output logic levels. The linear amplifier stages operate as comparators in an open loop configuration. As mentioned, the back end dynamic range should be greater than the output from the front end. Therefore, the input to the decision circuit must be able to handle voltages greater than the output logic level swing. No automatic gain control (AGC) is used in this circuit, so the linear amplifiers must act as limiting stages also. This is an inherent feature with the differential amplifiers used.

Referring back to Figure 2.1, it was assumed that the amplifier stages were identical and non-interacting. It has been shown that the minimum over-all rise time for a given gain is achieved through using all gain stages that are similar [8]. It is usually desired that the output stage have fast rise and fall times for conversion to a digital signal. Therefore, the input to the last stage is overdriven to square the output signal. This will however, also increase the propagation delay of the signal.
2.1.5 Bandwidth Requirements

The cascaded chain of linear amplifiers making up the decision circuit act as a series of single pole low-pass filters to the data signal. The bandwidth of the receiver will affect the shape of the PCM pulse. The PCM pulses usually are used in a non-return-to-zero (NRZ) data bit format. The amount of distortion of the pulse depends on how the bandwidth compares to the frequency spectrum of the PCM pulse. However, it usually is not necessary that the exact shape of the transmitted pulse be preserved. The distortion of the pulse shape is important only to the extent that it affects the ability of the receiver to make binary decisions on the data [1].

The correlation of receiver bandwidth to the data bit rate and the effect on the PCM pulse shape will be investigated. The bandwidth requirements for the back end decision circuit relative to the overall receiver bandwidth will also be presented.

The spectrum for a rectangular PCM pulse of duration T is obtained by taking the Fourier transform of the time domain response. This is shown in Figure 2.3. The spectrum extends to infinity, but it can be approximated by a bandwidth that goes to the first zero of the spectrum. This would suggest that a bandwidth of \( \frac{2}{T} \) Hertz would be needed.

\[
X(f) = VT \frac{\sin \pi f T}{\pi f T} \tag{2.14}
\]

For the NRZ data bit format, the data bit rate \( R \) can be related to the pulse width by

\[
R = \frac{1}{T} \quad \text{(bits/sec.)} \tag{2.15}
\]
By simply looking at the spectrum of the PCM pulse, the conclusion might be made that the bandwidth needed would be twice the bit rate. However, the actual effect of a low-pass filter on the pulse must be investigated.

The Fourier transform pair for an ideal low-pass filter is given in the following equations

\[
F(j\omega) = \begin{cases} 
1, & |\omega| < \omega_0 \\
0, & |\omega| > \omega_0 
\end{cases} 
\]  

(2.16)

\[
f(t) = \frac{\sin\omega_0 t}{\pi t} 
\]  

(2.17)

The output pulse shape is given by the convolution of the rectangular PCM pulse and the time domain response of the filter. This is shown in Figure 2.4 for several bandwidths.
When the filter bandwidth is greater than the bit rate, the flat top of the pulse starts to appear and the duration of the pulse decreases to the original pulse width $T$. When the bandwidth is less than $0.5R$, the pulse height does not reach its full amplitude. Smaller bandwidths result in slower rise times and spreading of the pulse width occurs. The original flat top of the pulse is not necessary for recovering the information conveyed in the data bit. However, as the pulse duration increases the successive pulses in the data stream begin to overlap. When this becomes significant, the interference between adjacent pulses, known as intersymbol interference (ISI), will result in the receiver making errors in the binary decision.

The effects of ISI can best be understood by examination of the "eye diagram" in Figure 2.5. It is formed by the superposition of pseudo-random sequences of PCM pulses. The decision points are made at the center of the eye opening. For a good system, the decision threshold or intersection of the rising and
falling edges of the signal should be at the 50% points of the signal transition from the binary 0 to a 1. The eye diagram in Figure 2.5 is for a filter with a bandwidth equal to half the bit rate of the signal. All of the pulse shapes in Figure 2.4 can be seen in the diagram, depending on the successive number of 1's in the pseudo-random sequence of bits. The larger the eye opening, the more reliable will be the binary decision. Although the original pulse shape is significantly degraded

![Eye diagram with BW = 0.5R](image)

**Figure 2.5:** Eye diagram with BW = 0.5R

for a bandwidth = 0.5R, the eye diagram is adequate for a reliable system. A smaller bandwidth for the same bit rate, or a faster bit rate for the same bandwidth would cause the eye opening to close, resulting in less reliable decisions. Noise in the system can also cause the same effect. Experience with practical receivers, where noise effects cannot be neglected, has shown the optimum bandwidth to be equal to 0.65R [3]. Therefore, the minimum bandwidth for bit rate R is given by

\[ BW = 0.5R \text{ (Hz)} \]  

(2.18)

For example, a signal bit rate of \( R = 300\text{Mb/s} \) would require a minimum receiver bandwidth \( BW = 150\text{MHz} \).
The decision circuit bandwidth requirements can be established by looking at the transfer function for the front end and back end circuits. For simplicity, both sections of the receiver are represented by single dominant pole amplifier stages. The break frequency or pole of the front end is $\omega_1$, and the back end is $\omega_2$. Then the transfer function is given by

$$H(j\omega) = \frac{H_0}{\left[1 + j\frac{\omega}{\omega_1}\right]\left[1 + j\frac{\omega}{\omega_2}\right]}$$ \hspace{1cm} (2.19)$$

The magnitude of the function is given by

$$|H| = \frac{H_0}{\sqrt{\left[1 + \frac{\omega}{\omega_1}\right]^2\left[1 + \frac{\omega}{\omega_2}\right]^2}}$$ \hspace{1cm} (2.20)$$

The bandwidth is defined by the frequency at which the magnitude curve is 3dB down from the DC or low frequency value. This is when

$$|H| = \frac{H_0}{\sqrt{2}}$$ \hspace{1cm} (2.21)$$

Combination of (2.20) and (2.21) results in an expression that relates the overall system bandwidth $\omega$ to the individual stage poles

$$\left[1 + \left(\frac{\omega}{\omega_1}\right)^2\right]\left[1 + \left(\frac{\omega}{\omega_2}\right)^2\right] = 2 \quad \Rightarrow$$

$$\frac{1}{\omega^2} = \left[\frac{1}{(\omega_1)^2} + \frac{1}{(\omega_2)^2} + \frac{\omega^2}{(\omega_1)^2(\omega_2)^2}\right]$$ \hspace{1cm} (2.22)$$
If \( \omega_2 > \sqrt{2} \omega_1 \), then the last term in (2.22) will be small compared to the other terms and can be neglected. This gives a more usable formula for the overall bandwidth as

\[
\frac{1}{\omega} = \sqrt{\frac{1}{(\omega_1)^2} + \frac{1}{(\omega_2)^2}}
\]

(2.23)

Also for this condition, \( \frac{\omega_1}{\sqrt{2}} < \omega < \omega_1 \), which means that the overall bandwidth will not be less than \( \frac{\omega_1}{\sqrt{2}} \). Therefore, the receiver bandwidth \( BW \) is primarily determined by the front end. As the back end bandwidth \( \omega_2 \) is increased further, the bandwidth \( \omega \) approaches the exact value of \( \omega_1 \). This suggests a back end bandwidth criteria of

\[
\omega_2 > 2\omega = 2BW
\]

(2.24)

when combined with (2.18) gives

\[
\omega_2 > 2(0.5R) \quad => \quad \omega_2 > R \quad (\text{Hz})
\]

(2.25)

The bandwidth criteria in (2.25) represents a very conservative design approach. For a given data bit rate \( R \), \( \omega_2 \) can be smaller. The penalty is a slower rise time for the output signal; however, this usually is acceptable as long BER requirements are met. Also, a smaller bandwidth effectively slows down the back end such that the power consumption decreases during the switching intervals.
2.2 Circuit Features & Data Sheet

Now that the design criteria for the decision circuit has been established, the features of the actual data quantizer circuit will be presented. Some of the information is actually from simulation and measurement results for the circuit. It is briefly presented here with the specifications in order to highlight the circuit features and to have that information together in one section.

The decision circuit is shown in more detail in Figure 2.6. The output from the preamplifier is coupled into 4 cascaded stages of wide-band linear amplifiers, providing 60dB of gain at a -3dB bandwidth of 160MHz. The circuit will operate at much higher bit rates than what the bandwidth would indicate, with good results. The penalties are slower rise times of the output signal and an increase in the input sensitivity level. The data outputs of the output driver stage are F100K ECL-compatible. This is a standard topology for the output stage which is a basic ECL switch (differential amplifier) driving low output-impedance emitter follower buffers [11]. The specified output logic levels for this ECL logic family are shown in Table 2.1.

The circuit input has a wide dynamic range of 58dB. The range is from the input sensitivity of 1.8mV\textsubscript{p-p}, up to the saturation level of the decision amplifier which is 1.5V\textsubscript{p-p}. 
Figure 2.6: Block diagram of data quantizer circuit
The circuit offers differential 750Ω input resistances which can be tied to a reference voltage. External resistors can also be added to increase the value of input resistance. Either the internal reference voltage ~3 Vbe, or an external voltage source can be interfaced to the resistors through the voltage buffer circuit. This provides a low impedance node to reduce common mode signal at the amplifier input. Either AC or DC coupling can be used to feed the preamplifier signal into the circuit.

An output disable circuit is included to latch the DATA outputs in the absence of input signal. This eliminates output "chatter" caused by noise at the circuit input. The circuit is activated by applying an ECL LO logic level at the disable circuit input. This results in latched condition with DATA=LO and DATA-Bar=HI. The input signal could be a control signal from a microprocessor. The disable circuit input is internally tied HI to allow normal circuit operation while leaving this input float. Another useful application is to prevent incorrect data from being passed by the system if the incoming signal falls below the power level set by the link monitor circuit. This is accomplished by feeding the FLAG output signal into the disable circuit input.

Input offset is very small (<1mV) with auto-zero cancellation. This is achieved by using the integrated transconductance amplifier in a DC feedback loop.

---

**TABLE 2.1: F100K ECL-compatible logic levels**

<table>
<thead>
<tr>
<th>Logic Level</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>High (VOH)</td>
<td>-1025</td>
<td>-952</td>
<td>-880</td>
<td>mV</td>
</tr>
<tr>
<td>Low (VOL)</td>
<td>-1810</td>
<td>-1715</td>
<td>-1620</td>
<td>mV</td>
</tr>
<tr>
<td>Voh - Vol</td>
<td>595</td>
<td>763</td>
<td>930</td>
<td>mV</td>
</tr>
</tbody>
</table>
The signal is tapped from midway through the cascaded amplifier chain, then low pass filtered and fed back to the amplifier input in a negative feedback configuration. The feedback loop is also used to provide the voltage reference for the DC coupled configuration.

The circuit operates from a single 5V power supply. A standard -5.2V can be used for ECL application, or +5V can be used for "raised" ECL logic levels. This would be similar to a TTL application, but with ECL logic level swings.

Independent power supply pins are provided for the data channel circuits and the link status monitor circuit. This reduces parasitic coupling between the data signal and the link status output. There is also a separate pin for the data output stage power supply $V_{ccA}$. This supply is only for the output emitter follower buffers so that changes in load currents during switching will cause no change in the data channel supply $V_{cc}$. This would be occur because of the small but finite inductance of the $V_{ccA}$ bond wire and package lead. All of the supply pins are then tied to the common $V_{cc}$ supply outside the package.

For comparison, existing decision circuits by Micro-Linear and Signetics, are compared to the data quantizer (ODL-DQ) as shown in Table 2.2. Most of the data is for typical operating conditions of $V_{cc} = +5V$ and $T_{amb} = 25^\circ C$. A direct comparison of the input referred noise (EN) values is not valid. This is because the noise is integrated over the bandwidth, and the circuits have different values of bandwidth.
TABLE 2.2: Comparative data sheet of decision circuit specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Signetics</th>
<th>ODL-DQ</th>
<th>u-Linear</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>DC Specifications</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Icc</td>
<td>Vcc Supply Current</td>
<td>42</td>
<td>75</td>
<td>65</td>
<td>mA</td>
</tr>
<tr>
<td>VIN</td>
<td>Input Sensitivity</td>
<td>2.0</td>
<td>1.8</td>
<td>2.0</td>
<td>mVp-p</td>
</tr>
<tr>
<td>VIN</td>
<td>Max Input Signal</td>
<td>1.6</td>
<td>1.5</td>
<td>1.4</td>
<td>Vp-p</td>
</tr>
<tr>
<td>VOS</td>
<td>Input V-Offset (No Auto-Zero)</td>
<td>-</td>
<td>1</td>
<td>3</td>
<td>mV</td>
</tr>
<tr>
<td>AC</td>
<td>AC Specifications</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Small Signal Bandwidth</td>
<td>75</td>
<td>160</td>
<td>65</td>
<td>MHz</td>
</tr>
<tr>
<td>EN</td>
<td>Input Referred Noise (max)</td>
<td>-</td>
<td>60</td>
<td>25</td>
<td>uV (max)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(typ)</td>
</tr>
<tr>
<td>tPD</td>
<td>ECL Output Propagation Delay</td>
<td>-</td>
<td>12</td>
<td>10</td>
<td>nS</td>
</tr>
</tbody>
</table>
2.3 DC Feedback

The design criteria and features of the decision circuit have been explored in detail. Specific criteria for operating the circuit with the DC feedback loop for input offset cancellation must be evaluated. Depending on the application, Vos may or may not be a problem. In many audio applications the stages are all capacitively coupled, thereby blocking DC voltages. For wide dynamic range applications, such as the decision circuit, Vos becomes a concern since useful signal levels are comparable in magnitude to the offset voltage. During an absence of input signal, the data outputs will "chatter" due to input noise, but the DC level of the outputs should be balanced. For large input offset, the outputs can be latched to the full ECL logic level swing. In this case the outputs will exhibit severe pulse width distortion for small input signals.

A block diagram demonstrating the negative feedback loop is shown in Figure 2.7. The first 2 gain stages in the data channel form the error amplifier, $a$, which has about 30dB of gain and a frequency response of 2 dominant poles in the hundreds of MHz range. The feedback amplifier $f$ is represented by the transconductance amplifier driving a load resistance $RL$:

$$ f = GM(RL) \quad (2.26) $$

A single dominant pole is set by capacitor CP for the frequency response of $f$.  

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Negative feedback is indicated since the error signal $v_e$ is equal to the difference of the input signal $v_i$ and the feedback signal $v_f$:

$$v_e = v_i - v_f$$  \hspace{1cm} (2.27)

The output of the transconductance amplifier is a current, but since it is driving a load resistance, the feedback amplifier overall acts as a voltage amplifier, representing *series-shunt* feedback [12]. The closed loop gain for the system $A$ is given by the following

$$A = \frac{a}{1 + af}$$ \hspace{1cm} (2.28)

where, the loop gain $T$ is equal to the product of the error and feedback amplifiers:

$$T = af$$ \hspace{1cm} (2.29)
The conditions for stability come from the Nyquist criterion which states that the magnitude of the loop gain should be less than unity at the frequency where the phase shift around the loop equals -180°:

\[ |T(j\omega)| < 1 \quad \text{where, ph} \ T(j\omega) = -180° \tag{2.30} \]

Typically, negative feedback is used to stabilize closed loop gain over a desired frequency range. The gain is usually > unity. For VOS cancellation, a closed loop gain of < unity (0dB) is desired, only at DC or very low frequency. The desired gain vs frequency curve is shown in Figure 2.8.

![DC feedback frequency response curve](image)

Figure 2.8: DC feedback frequency response curve

Evaluation of (2.28) shows that in order for \( |A(j\omega)| \) to be < 1, \( f \) must be > 1 so that the loop gain \( T \) is > a. With the dominant pole in the feedback path, the magnitude of the feedback will decrease to zero as frequency increases. The system is then back to the open loop gain of the wideband amplifiers. Ideally, there would
be a zero in the closed loop transfer function at DC or \( \omega = 0 \), since the magnitude of the gain must reach the open loop value over the desired frequency band of the signal. However, this would require a capacitance value \( C_P = \infty \).

The closed loop transfer function is derived by substituting the open loop functions \( a(s) \) and \( f(s) \) into equation (2.28). This will give more insight into how the DC feedback cancels the DC offset, and yet allows the data signal to be amplified by the full open loop gain of the data channel. The error amplifier, \( a \), has 2 high frequency dominant poles, so the transfer function is given by

\[
a(s) = \frac{a_0}{\left(1 + \frac{s}{P_2}\right) \left(1 + \frac{s}{P_3}\right)}
\]  

(2.31)

The dominant pole of the feedback amplifier \( f \) is determined by the filter capacitor \( C_P \), giving the transfer function as

\[
f(s) = \frac{f_0}{\left(1 + \frac{s}{P_0}\right)}
\]  

(2.32)

For good signal transfer, the feedback must go to zero over the signal frequency range; therefore, \( P_0 < < P_2, P_3 \). Since the feedback will only be active at low frequencies, \( P_2 \) and \( P_3 \) can be neglected for the closed loop response. The derivation of \( A(s) \) is as follows

\[
A(s) = \frac{V_O}{V_i} = \frac{a_0}{1 + a_0 f(s)} = \frac{a_0}{1 + a_0 \left[ f \left( \frac{s}{P_0} \right) \right]} = \frac{a_0}{1 + a_0 \left[ f \left( \frac{s}{P_0} \right) \right]}
\]
As the frequency dependent terms of the equation are separated from the DC gains, 2 changes become evident. First, the dominant pole $P_0$ in the open loop response becomes a zero $Z_0$ in the closed loop response. Also, another pole $P_1$ is created and is higher in frequency than $P_0$ by a factor of $T_0$ the loop gain:

$$P_1 = P_0(1 + a_0 f) = P_0(1 + T_0)$$ (2.33b)

Finally, the transfer function is given by

$$A(s) = \frac{a_0 \left( 1 + \frac{s}{P_0} \right)}{(1 + a_0 f) \left( 1 + \frac{s}{P_0(1 + a_0 f)} \right)} = \frac{a_0 \left( 1 + \frac{s}{P_0} \right)}{1 + \frac{a_0 f}{P_0}} \frac{1 + \frac{s}{P_0}}{1 + \frac{s}{P_1}}$$

(2.33a)

It is desirable to decrease the closed loop gain $A(s)$ by making $f > 1$. However, as seen in (2.33b), as $f$ gets larger so does pole $P_1$. $P_1$ is the corner frequency where the gain curve, after rising at $+20$dB/dec. because of the zero $Z_0$, levels out at the open loop gain $a_0$. $P_1$ must be kept low enough so that it does not extend into the frequency range of the signal.
CHAPTER 3

SUB-CIRCUIT DESIGN

3.1 Introduction

The transistor level circuit design is now presented. The sub-circuits implement the design criteria obtained from the fiber optic system requirements, as discussed in Chapter 2.

The design analysis will concentrate on the circuits in the data signal path of the decision circuit and the DC feedback loop. The data channel is comprised of 4 linear differential amplifier stages. The first 2 stages are included in the feedback loop. The voltage gain and frequency response of these circuits are investigated. The frequency response includes calculation of dominant poles and bandwidth. This is important for the stability analysis that was presented in Chapter 2.

The transconductance (GM) amplifier provides the feedback path for input offset cancellation. The circuit functionality is presented along with calculation of the gain, which is of importance in determining the feedback factor $f_o$. The frequency response is also investigated, although it will be set by an external dominant pole capacitance for offset cancellation.

The output drive stage not only drives the load, but is compatible with digital 100K ECL logic. This stage provides voltage gain and temperature stabilization of the output logic levels.
The high frequency analysis uses the hybrid-$
$ model for the bipolar transistor. This model is very useful to a first order for manual calculations. However, there are some limitations that become significant at higher frequencies. The basic model ignores lateral current flow in the transistor base, along with the excess phase shifts that are due to the distributed nature of the actual transistor parameters. This causes the model to be inaccurate at frequencies approaching $f_T$ of the transistors. Usually, the model is simplified further by the Miller-effect approximation, which assumes that the load is purely resistive with negligible capacitive loading at the output. These inaccuracies are most critical in predicting the response of feedback circuits, and a more sophisticated model should be used [10].

However, the feedback loop used in this circuit operates only at DC and low frequencies. Therefore the hybrid-$
$ model is used for insight into the manual calculations.

3.2 Linear Wide-Band Amplifiers

The input stage, along with the voltage reference circuit and input termination resistors, provide the interface with the signal from the preamp. The input sensitivity of the decision circuit is determined by this stage. This is because errors, such as $V_{os}$, induced from the first stage will be multiplied by the total circuit gain, resulting in large errors at the output. Errors induced by the subsequent stages are not as important, since they are only multiplied by smaller gains.

The second and third stages provide additional amplification of the signal. The circuits are similar, with only a difference in setting the DC bias. The input and second stages utilize a bandgap reference which generates the bias currents. The
third stage has its bias controlled by the output disable circuit. In the disable mode, the circuit simply turns off the bias to the third stage, and also forces the inputs to the output driver circuit such that the outputs are in the ECL logic LO state.

Thus, the gain of the first 2 stages is stabilized over temperature, the third stage will vary slightly. However, this is acceptable since over most of the input signal dynamic range, the third stage will be in the nonlinear region of operation. The output driver, on the other hand, has a bandgap reference control of the DC bias to assist in stabilization of the output logic levels.

3.2.1 Input Stage

The input stage or decision amplifier (DECAMP) uses a basic emitter-coupled pair differential amplifier topology

![Emitter-coupled pair with emitter follower inputs](image)

Figure 3.1: Emitter-coupled pair with emitter follower inputs
with emitter follower input buffers, as seen in Figure 3.1. The emitter-coupled pair is useful for the input stage because of its low offset voltage and high frequency response. Cascades of these stages can be directly coupled without interstage capacitors. The emitter follower buffers are used to obtain high input impedance and low input currents.

The effect of the emitter follower buffers on the amplifier transfer function can be neglected for frequencies of operation that are \(< 10\%\) of \(f_T\). The voltage gain is \( \approx 1 \) as long as the product of the transconductance and emitter resistor is much greater than unity:

\[
A_{\text{EF}} \approx 1 \quad \text{for} \quad gm_1 RE >> 1 \tag{3.1}
\]

where,

- \( A_{\text{EF}} \Rightarrow \) voltage gain of emitter follower buffer
- \( gm_1 \Rightarrow \) transconductance of transistor Q1
- \( RE \Rightarrow \) emitter resistor

The high frequency gain is controlled by a pole and a zero in the transfer function. Typically, the zero is slightly higher in frequency than the pole, but both are near the \(f_T\) of the emitter follower transistor [12].

The transfer function for the emitter-coupled pair is obtained by using the small-signal equivalent of the differential-mode half circuit as seen in Figure 3.2a&b. The equivalent circuit in Figure 3.2b is simplified further by using the Miller-effect approximation for the collector-base junction capacitance \(C_{u3}\). This capacitance is replaced by a capacitor in parallel with \(C_{r3}\) and another in parallel with \(C_{c3}\), giving equivalent capacitances of
\[ CT = C_{r3} + (1 + g_{m3} R_L) C_{u3} \]  \hspace{1cm} (3.2)

and,

\[ CL = C_{ca3} + C_{u3} \]  \hspace{1cm} (3.3)

Also,

\[ C_T = C_{je} + g_{mTF} \]  \hspace{1cm} (3.4)

Figure 3.2: (a) Differential-mode half circuit for emitter-coupled pair
(b) Small-signal equivalent circuit

where,

- \( C_{r3} \) => base-emitter junction and diffusion capacitance
- \( g_{m3} \) => transconductance of transistor Q3
- \( R_L \) => differential amplifier load resistance
- \( C_{u3} \) => collector-base junction capacitance
- \( C_{ca3} \) => collector-substrate capacitance
- \( C_{je} \) => base-emitter junction capacitance
- \( t_F \) => forward base transit time

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Parasitic wiring capacitances from the IC layout can be lumped into $C_L$, the total collector capacitance. Circuit analysis of Figure 3.2b gives the transfer function $a(s) = \frac{V_o}{V_i}$. The DC gain $a_0$ is given by

$$a_0 = -g_{m3}RL \left( \frac{r_{x3}}{(R_S + r_{b3} + r_{x3})} \right) \quad (3.5)$$

and the transfer function is given by

$$a(s) = \frac{a_0}{(1 + sR_L C_L) \left( 1 + sC_T \frac{(R_S + r_{b3})r_{x3}}{(R_S + r_{b3} + r_{x3})} \right)}$$

$$a(s) = \frac{a_0}{\left( 1 + \frac{s}{P_L} \right) \left( 1 + \frac{s}{P_2} \right)} \quad (3.6)$$

where,

- $r_{x3} \quad \Rightarrow \quad$ small-signal input resistance $= \frac{\beta_o}{g_m}$
- $R_S \quad \Rightarrow \quad$ source resistance (equal to the output resistance $R_O$ of the emitter follower buffer)
- $r_{b3} \quad \Rightarrow \quad$ base spreading resistance

The negative sign in (3.5) indicates that the amplifier is inverting. Equation (3.6) shows 2 poles as

$$P_L = \frac{-1}{(2\pi R_L C_L)} \quad (3.7a)$$

$$P_2 = -\left( \frac{(R_S + r_{b3} + r_{x3})}{(R_S + r_{b3})r_{x3}} \right) \left( \frac{1}{2\pi C_T} \right) \quad (3.7b)$$

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Most of the terms used in (3.2) through (3.6) are obtained from the processing parameters. However the transconductance $g_m$ depends on the design value for the transistor DC collector current according to

$$g_m = \frac{I_{c3}}{V_T}$$

(3.8)

where $V_T$ is the thermal voltage constant = 25.8mV at room temperature. It has been shown that the derivation of optimum transistor biasing for minimum propagation delay in the basic emitter-coupled pair results in a value of $I_{c,\text{opt}} = 1.1\text{mA}$ [8]. Using this and (3.5), the proper load resistance $R_L$ is found, such that the amplifier gain $A_o = 15\text{dB}$. The real frequency value of the poles are found by substitution of $s = j\omega$ into (3.6) and using the PSPICE models to obtain the following small-signal parameters used in (3.7)

$r_{b3} = 55\Omega$ \hspace{1cm} $C_{je3} = 405\text{fF}$ \hspace{1cm} $C_{u3} = 107\text{fF}$

$C_{cs3} = 195\text{fF}$ \hspace{1cm} $\beta_3 = 28.7\text{ps}$

with the values of the poles as

$\text{P}_2 = -931\text{ MHz}$ \hspace{1cm} and, $\text{PL} = -3.5\text{ GHz}$

$\text{P}_2$ is seen to be the dominant pole and approximately sets the -3dB bandwidth of the amplifier. A more representative schematic is shown in Figure 3.3. Transistors Q5 and Q6 are used to shift down the maximum voltage on the collectors of Q3 or Q4 at the stage output. This is so that the input of the subsequent stage is not saturated. Transistors Q7 and Q8 make up the tail current source and are biased by a bandgap reference.
Figure 3.3: Wide-band differential amplifier stage
3.2.2 VOS Calculation

The overall input offset of an amplifier is actually composed of an input offset voltage $V_{os}$ and an input offset current $I_{os}$. These represent the effect of all the component mismatches within the amplifier, referred back to the input. In the emitter-coupled pair, the offset is due to mismatches in transistor base width and doping level, collector doping level, effective emitter area, and in collector load resistors. In more general terms, $I_{os}$ is primarily due to differences in input currents because of mismatches in transistor $\beta$. Also, $V_{os}$ is primarily due to mismatches in transistor $V_{be}$ [13].

Since voltage sources are used at the inputs of the first stage, the input base currents see the same thevenin impedance, and $V_{os}$ is more of a concern than $I_{os}$. $V_{os}$ is then the differential input voltage which must be applied to the amplifier to drive the output to zero. Providing this cancellation voltage is the purpose of the feedback loop. The voltage is developed at the input through the current output of the transconductance amplifier driving the input resistance. The maximum $V_{os}$ is calculated here, to determine the current drive requirements of the transconductance amplifier.

The following calculation of $V_{os}$ assumes that the transistors are of uniform base, $r_b = 0$, and that the component mismatches are statistically independent. The analytical procedure involved is then less tedious. Through variational analysis, the input offset is

$$V_{os} = V_T \sqrt{\left( \frac{\Delta R_E}{R_E} \right)^2 + \left( \frac{\Delta I S_{1,2}}{I S_{1,2}} \right)^2 + \left( \frac{\Delta R L}{R L} \right)^2 + \left( \frac{\Delta I S_{3,4}}{I S_{3,4}} \right)^2} \quad (3.9)$$
The first 2 terms are due to emitter resistor mismatches and transistor saturation current density mismatches in the emitter follower buffers. The third and fourth terms are due to load resistor mismatches and saturation current mismatches in the emitter-coupled pair.

The numerical value for the offset is obtained from a worst-case saturation current density mismatch of ±8%, and a resistor mismatch of ±1%. This gives

\[
V_{OS,\text{max}} = V_T \sqrt{0.0001 + 0.0064 + 0.0001 + 0.0064} \quad (\text{mV})
\]

\[
V_{OS,\text{max}} = 2.96\text{mV} \quad (3.10)
\]

The sensitivity of input offset to temperature is not zero. Therefore, even if input offset is trimmed to be as low as possible or cancelled out, as the temperature changes, the offset will increase. Besides temperature, supply voltage changes and aging of the device will also increase the offset. The best solution is auto-zero of the offset. This correction is independent of temperature, age, and power supply.

3.2.3 Second Stage

The equations presented in Section 3.2.1 for development of the amplifier transfer function are also used with the second stage. The circuit is the same as that in Figure 3.3, only with different emitter resistors in the emitter follower buffers. The outputs from the first stage are directly coupled into the second stage and so on to the third and output stages. Following the same derivation, the poles are found to be

\[ P_3 = -758 \text{ MHz} \quad \text{and,} \quad P_L = -3.3 \text{ GHz} \]
$P_3$ is seen to be the dominant pole and approximately sets the -3dB bandwidth of the amplifier.

### 3.3 Transconductance Amplifier

The primary application of the DC feedback loop is as was shown in Figure 2.6. The output of the feedback amplifier must drive the low input impedance of the termination resistors at the input stage. Therefore, a voltage input to current output circuit is used. The current driving the input resistors, gives an overall voltage gain for the amplifier. Since high output resistance is needed for the feedback amplifier, a cascode configuration is chosen. The cascode amplifier has benefits of large voltage gain in a single stage with an active PNP load, high output impedance, and a reduction in the high frequency feedback that occurs from the output to the input through $C_u$ as occurs in the common-emitter stage used in the basic differential amplifier [14]. A basic cascode differential amplifier will first be presented. Then, the advantages of the folded cascode amplifier will be investigated. The small-signal gain will be determined through analysis of the small-signal equivalent circuit.

#### 3.3.1 Folded Cascode

The cascade configuration is a common-emitter stage driving a common-base stage. It has a higher degree of isolation between its input and output than does the common-emitter stage. This is because the reverse transmission through the compound device stage is reduced by the impedance mismatches between the transistors. The cascode amplifier can be configured as a differential amplifier as shown in Figure 3.4. This configuration eliminates common-mode DC output voltage sensitivity to device mismatches and component variations. Now the common-emitter collector output sees the input to the common-base stage as the
load instead of \( R_C \). This reduces the Miller effect on Q1, thereby reducing the feedback through \( C \).

![Cascode Differential Amplifier Diagram](image)

Figure 3.4: Basic cascode differential amplifier

It is important that the source resistances are matched. This minimizes any DC offsets in this amplifier due to the input base currents. Also, noticeable are the emitter degeneration resistors \( R_E \). These provide local series feedback in the stage, to stabilize the gain. Other benefits are an increase in input impedance and an increase in the linear input range for the differential pair. This increases the range of offset that the feedback amplifier can cancel. Although the amplifier shown here has a voltage output, these principals and benefits will be applied to the actual feedback amplifier.
A substantial disadvantage of this configuration is the decrease in input dynamic range from the basic emitter-coupled pair. The common-base transistors Q3 and Q4, in Figure 3.4, need adequate collector-emitter bias voltage. This directly subtracts from the available input dynamic range.

The folded cascode amplifier maintains the larger input dynamic range of the basic emitter-coupled pair as well as the benefits of the cascode configuration. The folded cascode transconductance amplifier is shown in Figure 3.5. Here the common-base transistors are "folded over" and feed into a current mirror. Because of the change of direction in the current flow, these transistors are now PNPs. The bias voltage for the common-base transistors is provided by the $V_{be}$ multiplier formed by Q8 and R1 and R2. The voltage supplied to the bases of the PNPs (referenced to $V_{cc}$) is given by

$$V_{bias} = V_{be} \left( 1 + \frac{R2}{R1} \right)$$  \hspace{1cm} (3.11)

The single-ended output allows the circuit to source and sink current that is proportional to the differential input voltage. Here, the load current into the reference leg of the current mirror is controlled by the collector current of Q1 through the folded cascode transistor Q3. Similarly, the current through cascode transistor Q4 is controlled by the collector current of Q2. And, the current into the mirror transistor Q6 is also controlled by $I_{c1}$. The output current $I_o$ is equal to the difference of $I_{c4}$ and $I_{c6}$, which are both respectively controlled by $I_{c2}$ and $I_{c1}$. Therefore, the currents are related by

$$I_o = I_{c1} - I_{c2}$$  \hspace{1cm} (3.12)
The circuit still has emitter degeneration, which as a voltage to current amplifier, helps to stabilize the overall transconductance $GM$ even against variations in the tail current. Also, the output resistance $R_O$ increases.
Figure 3.5: Folded cascode transconductance amplifier
3.3.2 Small-Signal Gain

The small-signal equivalent circuit for the basic cascode amplifier in Figure 3.4 can be used to derive the overall GM for the folded cascode circuit. To determine the -3dB bandwidth, the device parasitics of the current mirror must also be included since a portion of the output signal from the feedback amplifier goes through it. However, the frequency response of the feedback amplifier will be dominated by the external capacitor $C_P$ and the termination resistor at the input stage.

The low frequency equivalent circuit for the differential-mode half circuit is shown in Figure 3.6. However, the placement of $R_C$ is the same as in the folded cascode circuit. The $r_b$ of Q3 is neglected; this is reasonable except at very high frequencies. The circuit is further simplified by treatment of the emitter degeneration resistor $R_E$, as shown in Figure 3.6. It is replaced by the new simple common-emitter stage with the following parameters:

\[
R_{1}' = r_x (1 + g_m R_E) \\
R_{O_1} = r_{01} (1 + g_m R_E) \\
G_M = \frac{g_m}{(1 + g_m R_E)}
\]  

(3.13)  
(3.14)  
(3.15)

also for the common-base stage of Q3,

\[
R_{O_3} = B_0 R_{03} \\
r_{e3} = \frac{\alpha_{03}}{g_m} \approx \frac{1}{g_m} \\
\alpha_{03} = \frac{I_c}{I_e}
\]  

(3.16)  
(3.17)  
(3.18)
Figure 3.6: Cascode small-signal equivalent circuit
where,

\[ r_{v1} \Rightarrow \text{small-signal input resistance} = \frac{\beta_o}{g_m} \]
\[ r_o \Rightarrow \text{incremental output resistance} \]
\[ r_{e3} \Rightarrow \text{effective emitter resistance} \]
\[ \alpha_{o3} \Rightarrow \text{product of emitter injection efficiency and base transport factor (-1)} \]

The benefits due to emitter degeneration are evident from (3.13) through (3.15). It is evident that the Miller effect is reduced since the collector of Q1 sees the parallel combination of \( R_C \) and \( r_{e3} \). The common-base stage has a current gain from emitter to collector of Q3 of \( \alpha_{o3} \), which says

\[ i_{c3} = \alpha_{o3} (i_{c1}) = i_{c1} \] \hspace{1cm} (3.19)

Therefore, the overall transconductance of the circuit \( GM \) is approximately equal to the transconductance of the common-emitter stage \( GM_1 \).

A few correction factors will give better accuracy. These are due to the voltage divider between \( R_S + r_{b1} \) and \( R_i' \) at the circuit input, the actual current gain of the Q3 stage \( \alpha_{o3} \), and the current divider between \( R_C \) and the input resistance of the Q3 stage \( r_{e3} \), which is

\[ K = \frac{R_C}{(R_C + r_{e3})} \] \hspace{1cm} (3.20)

Finally, the overall \( GM \) of the circuit is given by

\[ GM = \frac{i_o}{v_s} = \left[ \frac{R_i'}{(R_i' + R_S + r_{b1})} \right] \left( \alpha_{o3} K \ GM_1 \right) \] \hspace{1cm} (3.21)
It should be noted that $Rs$ in (3.21) is output resistance of the emitter follower buffer in the third amplifier stage. The input signal to the feedback amplifier and the link status monitor flag circuit is actually tapped off the data channel after the input buffer of the third stage, not directly at the output of the second stage.

The equivalent voltage gain for the circuit can be derived by adding the load that the GM amplifier will drive. This is shown in Figure 3.7. Here, $RO$ is the output resistance of the circuit and is the parallel combination of $RO_3$ and the output resistance $RO_{cs}$ of the current mirror of transistors Q5 and Q6 from Figure 3.5. $RO$ will typically be in the MΩ range. $RO_{cs}$ is found by

$$RO_{cs} = r_{o6} \left[ 1 + \frac{I_{o6}R_3}{VT} \right]$$

(3.22)

$$r_o = \frac{VA}{I_c}$$

(3.23)

where,

$$VA \rightarrow \text{Transistor Early voltage}$$

![Figure 3.7: Two-port small-signal equivalent of GM amplifier](image)
$R_L$, shown in Figure 3.7, represents the termination resistor at the input stage, and $C_P$ is the dominant pole capacitance used in the feedback loop. Since typically the condition will exist where $R_L < < R_O$, the output voltage $v_o$ will be the product of the output current and $R_L$. The low frequency gain $f_o$ is then derived as follows

$$v_o = i_o R_L \quad \text{and, } i_o = G_M v_B \Rightarrow$$

$$f_o = \frac{v_o}{v_B} = G_M (R_L)$$

(3.24)

which is the same as equation (2.26). This gives the pole $P_0$ from (2.32) as

$$P_0 = \frac{1}{(2\pi R_L C_P)}$$

(3.25)

Plugging in the appropriate parameters from the PSPICE models for the transistors, the value for $G_M$ is found to be

$$G_M = 1.146 \quad (\text{mA/V})$$

(3.26)

When this and $R_L = 75\Omega$ is used in (3.24), $f_o = .086$ is the result. This is far less than the desired gain of the feedback amplifier of $f_o > 1$. As mentioned earlier, external input resistors can be used to increase the input resistance in the data quantizer circuit. A value of 5K$\Omega$ increases the gain to $f_o = 5.7$ or 15.1dB. Now the feedback gain is the same as one of the individual gain stages in the data channel.

3.4 Data Output Driver Stage

The output stage, shown in Figure 3.8, is a standard topology for an F100K ECL-compatible output buffer. Basically, it is a linear differential amplifier stage similar to the first three. The differences are that the outputs of the emitter-coupled pair drive large emitter follower transistors Q7 and Q8, and the cross-connected
The diode and resistor combination of Q5 and Q6 and R5 and R6. The output drive transistors are large enough to drive the external 50Ω loads to a $V_{cc} - 2V$ supply.

The diode and resistor combination provides temperature compensation of the ECL output logic levels by controlling the output voltage level over the required temperature range. During the switching intervals, both diodes turn off, so that the gain does not decrease. A separate power supply pin $V_{ccA}$ provides power to the emitter-coupled stage and the large output driver transistors.

Figure 3.8: F100K ECL output drive stage
CHAPTER 4

FABRICATION

4.1 High-Frequency Technology

The ability for an integrated circuit (IC) to perform well at high frequencies is strongly dependent on the frequency response characteristics of the active devices used. Often circuit techniques can be used to optimize performance, but this is no substitute for having devices with good high-frequency characteristics. Special considerations must go into the structure of such devices.

Typically, the NPN bipolar transistor has the best high-frequency characteristics, and is used in the signal path of most circuits. Therefore, building blocks such as active loads usually are not used in wide-band amplifiers. IC Processes that do have PNPs, are often lateral or substrate devices with poor characteristics, and so they are confined to biasing applications.

The Complementary Bipolar Integrated Circuit (CBIC) technology features vertical NPN and PNP transistors with comparable gain and frequency characteristics. The advantage here is that circuit designs can have high output load drive capability, large input and output voltage swings, reduced power consumption, and still operate at high-frequencies. However, these advantages require higher wafer fabrication costs due to additional masks and diffusion steps.
4.1.1 Device Requirements

For an amplifier to operate up to a particular -3dB bandwidth, the desirable ft of the transistors needs to be 5-10 times higher in frequency [10]. To increase ft, emitter-base and collector-base junction areas must be minimized to reduce parasitic capacitance. Also, the transistor base width must be kept to a minimum to reduce the transit time tf. The transistors must be biased at high emitter currents, where ft is maximum.

Because of base current crowding, the base-emitter transistor action tends to occur along the emitter periphery instead of underneath the emitter. Therefore, to minimize the parasitic series base spreading resistance rb, a multiple base and emitter narrow stripe geometry is used. The reduction in rb is also good for noise considerations. The parasitic series collector resistance is reduced by use of a low-resistance buried layer under the collector.

4.1.2 AT&T CBIC-U Process

The CBIC-U process offers complimentary transistors that are true vertical devices. The 12V NPN has a typical ft = 4 GHz with β0 = 125. The 11V PNP has a typical ft = 2.7 GHz with β0 = 35 [15]. Cross-sections of the transistors are shown in Figure 4.1. The transistors are junction isolated. After the buried layers for the transistor collectors are implanted into the p-type substrate, an n-type epitaxial (n-epi) layer is grown on top. This layer forms the collector region of the NPN, surrounded by a p-type diffusion isolation ring. The PNP collector is formed by a deep p-type implantation in the epi layer. The transistor collector regions wrap around the base regions which are implanted. The n-epi serves as the substrate for the PNP transistor and should be tied to the most positive potential in the circuit to
Figure 4.1: CBIC-U transistor structure
maintain device isolation. Similarly, the p-substrate should be tied to the most negative potential.

4.2 IC Layout

The data quantizer circuit is processed in AT&T's Microwave CBIC-U technology. The circuit is a re-metallization of an existing base chip which is a 1-chip receiver IC design. This is different than a linear array design, in that transistor, resistor and capacitor size and location is optimized for a preamp circuit and decision circuit on one chip, and not a generic tile layout of certain components as in an array. The components from the preamp circuit were utilized in adding the new features, such as output disable circuit, the voltage buffer circuit, and the DC feedback circuit. Also, the original circuit was designed when the technology was in its early stages. At that time it was felt that a mostly NPN design was a lower risk. Therefore, the entire data channel circuits use NPNs exclusively. The DC feedback amplifier, which is a new design, uses PNPs.

The photomicrograph of the IC is shown in Figure 4.2. The right one-third of the IC contains the cascaded linear amplifiers with the bandgap references. The signal inputs are at the bottom of the IC and the data outputs are at the right, top corner. This separation reduces parasitic feedback from output to input. The link status monitor flag circuit is in the remaining upper, left side of the chip. The flag outputs come out to the left side of the IC, away from the signal path. This reduces parasitic coupling to the data signal. The new circuits are in the remaining lower, left side of the chip.
Figure 4.2: Chip photomicrograph of data quantizer IC
CHAPTER 5

EXPERIMENTAL RESULTS & ANALYSIS

5.1 Circuit Simulation

The design was verified through the use of ADVICE, the AT&T proprietary IC circuit simulator. After functionality of the circuit was established, the frequency response of the data channel was simulated to help predict the maximum bit rate. Then, the use of the feedback loop for input offset cancellation was investigated. The simulation results presented here are from the nominal device models at room temperature for comparison to calculated values. The various input configurations for the circuit are shown in Figure 5.1. The supply voltage is +5V. The data outputs are terminated by 50Ω to [V_{cc} - 2V]. Worst-case simulations performed during the circuit design phase are not included.

5.1.1 Open-Loop Response

The gain vs. frequency curves for the linear amplifiers in the signal path were found through AC analysis of the circuit, using the configuration in Figure 5.1a. A gain of 15dB and a -3dB bandwidth of 950 MHz for the input stage is shown in Figure 5.2. A gain of 15dB and BW = 814 MHz for the second stage is shown in Figure 5.3. The gain for all 4 cascaded stages and the phase of the output signal is shown in Figure 5.4. The input signal is 1mV_p-p or -60dB. The overall gain is slightly larger than 60dB, with the extra gain in the output stage. It is the output stage that drastically limits the decision circuit’s -3dB bandwidth to 160 MHz.
Figure 5.1: Various input configurations
This primarily is due to the parasitic capacitance associated with the large output emitter follower transistors. It is possible to drive the output stage at a higher current and improve the frequency response. However, power consumption also increases.

The differential output voltage of each stage vs. time was found through transient analysis of the circuit, using the same configuration. Figure 5.5 shows the outputs for a 10mV<sub>p-p</sub>, 400Mb/s, 1010 input signal pattern. It can be seen that the third gain stage (ECLAMP2) is operating in the non-linear range. The output rise and fall times are beginning to appear slow compared to the other signals. Figure 5.6 shows the outputs for a 50mV<sub>p-p</sub>, 600Mb/s, 1010 input signal pattern. It can be seen that both the second (ECLAMP) and third stages are operating in the non-linear, signal limiting region. The output rise and fall times now exceed the pulse width and the signal amplitude is degrading. This does not mean that the circuit is not useful at this bit rate, as long as BER requirements are still met.
Figure 5.2: Input stage AC frequency response

Figure 5.3: Second stage AC frequency response
Figure 5.4: Data channel AC frequency response
Figure 5.5: Gain stage output signals at 400Mb/s

Figure 5.6: Gain stage output signals at 600Mb/s
5.1.2 Closed-Loop Feedback & VOS Cancellation

The GM transfer curve measures output current vs. input voltage for the feedback amplifier. The linear range of the output current extends ±200μA, as shown in Figure 5.7. This is more than sufficient for input offset cancellation.

The -3dB bandwidth of the folded cascode transconductance amplifier is given for 2 different values of $R_L$ as shown in Figure 5.8. For $R_L = 75Ω$, $BW = 181MHz$; and for $R_L = 5KΩ$, $BW = 24.7MHz$. This agrees with calculated values obtained by zero-value time constant analysis [12]. For $R_L = 75Ω$, the voltage gain is < unity, and the circuit shows -21dB attenuation, while the input is -20dB. For small values of $R_L$, the bandwidth changes very little, with the device parasitics determining the value. As $R_L$ increases, the parasitics of the output devices become dominant in setting the bandwidth. For $R_L = 5KΩ$, the circuit shows 15dB of gain, which will give a more desirable closed-loop frequency response.

The frequency response of the decision circuit with DC feedback is shown in Figure 5.9 for $R_L = 75Ω$. For these simulations, the input configuration of Figure 5.1b was used, with the data outputs terminated the same as in Figure 5.1a. Although the feedback does decrease the low-frequency gain, any input offset still gets amplified instead of attenuated, this is undesirable. The value of $C_P$ is .03μF, and the gain curve does agree with the calculations in section 2.3 for the closed-loop pole and zero. The closed-loop frequency response with $R_L = 5KΩ$ is shown in Figure 5.10. Here, the stronger feedback decreases the low-frequency gain below unity, and input offset gets attenuated. A smaller value of $C_P = 1000pF$ can be used.

The effects of the DC feedback are seen in Figure 5.11. Here, the Data and Data-Bar outputs are shown for a 10mV $V_{PP}$ input signal to the input stage with $V_{OS} = +3mV$. The pulse width distortion is very evident with the 0's much longer than
the 1's for the Data output. Then the output signals are again shown for the same conditions, but using the feedback loop. Here, the offset is cancelled such that the output signal matches that of the circuit with no offset.
Figure 5.7: Large-signal transfer characteristics of GM amplifier

Figure 5.8: Feedback amplifier AC frequency response
Figure 5.9: Closed-loop AC frequency response with $RL = 75\Omega$
Figure 5.10: Closed-loop AC frequency response with $R_L = 5\,\Omega$
Figure 5.11: Input offset cancellation with DC feedback
5.2 Experimental Results

The metal mask generation and wafer fabrication were done by AT&T Microelectronics at Reading, Pennsylvania, using the CBIC-U IC process. Since automated testing has not yet been developed, visually good chips were selected from the wafer after sawing. These were packaged in 32-pin ceramic chip carrier packages to accommodate the inputs and outputs as well as the multiple power supply pads which are then tied together on the printed-circuit test board. This package was chosen for minimization of package lead inductance.

The devices were then hand tested for functionality, using the same test configurations as for the simulations. Those that passed these tests were then also dynamically tested for sensitivity and BER measurements.

5.2.1 DC Functionality

Many of the characterization results were presented in Table 2.2 for comparison to other similar circuits. Typical values for $V_{OS}$ were from .5 to .9mV.

Other characterization included the loop transconductance of the feedback loop. This is a measure of

$$a_{\text{GM}} = \frac{i_o}{v_1}$$

(5.1)

It is similar to the transfer curve in Figure 5.7 for the feedback amplifier, but gives the GM amplifier output current vs. the input signal to the input stage. This is shown in Figure 5.12. The current scale is similar, but the voltage input is much smaller because of the gain of the first 2 linear amplifier stages.

5.2.2 High-Frequency Dynamic Performance

The test configuration of Figure 5.1a was used with a device with low $V_{OS} < .4mV$ to evaluate how the open-loop bandwidth effects the eye diagram. This is
shown in Figures 5.13, 5.14, and 5.15 for 200Mb/s, 400Mb/s, and 600Mb/s pseudo-random word patterns respectively. The eye-openings are good for 200 and 400Mb/s operation, but the eye starts to close at 600Mb/s. However, this may still be acceptable, as long as the BER requirements are met. Actually, it is felt that estimation of maximum bit rate from single pulse trains or small-signal bandwidths are not sufficiently reliable methods. More informative for the particular application is the eye pattern of the output voltage [5].

The test configuration of Figure 5.1b was used to evaluate the effects of input offset on the eye diagram, and the ability of the feedback loop to cancel it. A +3mV offset was added to the circuit by externally feeding current into the 5KΩ input resistor at D1. The input signal amplitude was only 5mV_{pp}, and at a bit rate of 300Mb/s. The resulting eye diagram with no offset cancellation is shown in Figure 5.16a. It can be seen that the decision threshold has been shifted in a positive direction. There is also severe phase jitter in the output signal. The eye diagram with the DC feedback loop is shown in Figure 5.16b. It has good eye opening and is the same as the device with low Vos used in the open-loop configuration.

The sensitivity and bit error rate measurements were performed on the low Vos device using the configuration in Figure 5.1a. The test set-up is shown in Figure 5.17. The tau-tron Bit Error Rate transmitter model STX-1101 is driven by a Wavetek signal generator. The DATA output of the tau-tron, which is a 2^{11}-1 pseudo-random word bit pattern, drives the D1 input of the data quantizer circuit through a -26dB attenuator which gives better resolution of the input signal at low levels for the sensitivity measurements. The input signal amplitude is measured with a high impedance FET input probe to a Tektronix model 11801 digital sampling oscilloscope. The scope triggers off the SYNC Pattern output for
measuring the input pulses. The SYNC Clock output is used to trigger the scope for looking at eye diagrams. The circuit Data output goes into the tau-tron Bit Error Rate receiver model SRX-1101.

The input signal sensitivity of the decision circuit vs. the bit rate is shown in Figure 5.18. The input sensitivity is defined as the signal amplitude needed to maintain a 10-9 BER. The sensitivity performance is good even at 600Mb/s. Next, keeping a constant bit rate of 600Mb/s, the BER is measured as the input signal amplitude varies. The resulting graph of BER vs. input signal strength is shown in Figure 5.19. These results show that operation of the decision circuit at 600Mb/s is possible, but has penalties of slow rise and fall times of the output signal and a degradation in the input sensitivity which decreases the input dynamic range.

5.2.3 DC Coupled Application

The circuit can be used for DC coupled applications with the input configuration of Figure 5.1c. However, the use is limited to applications where there are frequent transitions in the data signal, such as is typical of telecommunication applications. Also, the data cannot be of a duty cycle much different than 50%. For this circuit, the decision reference voltage is derived from the DC average value of the data signal over a much longer time constant than the pulse width. This is because of the low-frequency limitation of the feedback loop.

The characteristics of Inter and Intra-office computer communications are typically those of short bursts of digital data followed by dead spaces, where no data is transmitted. Although these data bursts often have a "preamble" of sacrificial data transition bits for the receiver to establish a reference voltage for the decision threshold, it must be set fast enough or errors will be made in the binary logic decisions for the first true data bits. This application is known as Burst Mode.
Establishing the decision threshold requires more sophistication than sensing the average value of the data signal over a period of time for this application [16].

The circuit configuration of Figure 5.1c was used with a $2^7-1$ pseudorandom word bit pattern. The functionality of the configuration was verified, and sensitivity results similar to the AC coupled configuration were measured. Typically, AC coupling should have superior sensitivity over DC coupling because of the band limiting provided by the coupling capacitor. This limits the noise into the decision circuit.
Figure 5.12: Large-signal transfer characteristics of feedback loop
Figure 5.13: Eye diagram of Data output @ 200Mb/s
Figure 5.14: Eye diagram of Data output @ 400Mb/s
Figure 5.15: Eye diagram of Data output @ 600Mb/s
Figure 5.16a: Effect of +3mV offset @ 300Mb/s

Figure 5.16b: Good eye diagram with DC feedback
Figure 5.17: Test set-up for sensitivity and BER measurements
Figure 5.18: Input sensitivity vs. bit rate
Figure 5.19: BER vs. input signal strength @ 600Mb/s
CHAPTER 6

CONCLUSION

The design and operation of a data quantizer circuit for fiber-optic data-link applications has been verified. The circuit implements the design criteria for the decision circuit in an optical receiver, but with superior performance compared to other available decision circuits.

There was good agreement between the design calculations and the simulated results. The circuit operation was as predicted by the design using parameters obtained from the PSPICE simulation models of the CBIC-U transistors. The new circuits were implemented with available components on the existing base chip that had formed a preamplifier circuit. This made the design similar to that of using an array layout. Excellent results were obtained.

A correlation of bandwidth to the bit rate was investigated. Although the bandwidth helps determine the maximum bit rate, it does not necessarily limit it. Other factors such as the BER requirements strongly determine the maximum bit rate. Optical communication standards such as SONET place specifications on the shape of the opening of the eye diagram as a factor in determining bit rates.

Through the use of feedback, input offset cancellation is achieved with no degradation to the data signal. This can replace trimming of the input offset, which requires an additional testing step for every IC to be manufactured. It also enables
the use of DC coupling, for some limited applications, in a decision circuit that primarily was limited to AC coupling only.

The test configuration of Figure 5.1b, using the DC feedback loop, initially had problems with noise on the connection to the external capacitor CP. The feedback loop was working, but with 10 to 15 mV measured on the external wire, the input signal strength had to be much larger. Most of the external circuit wiring used striplines on the pc-board; unfortunately, the feedback loop had to be externally wired. Shielding the wire improved the performance only slightly. Putting a 1KΩ external resistor in series with the loop as close as possible to the D2 input formed a voltage drop which significantly decreased the noise input to D2, but allowed the same feedback current to pass. This allowed the same input sensitivity as in the open-loop case.

Also, for a good comparison of AC to DC coupling to be made, a lower noise set-up would be needed, such as mounting on a HIC instead of a pc-board, with miniature external components. In this set-up, additional components should not need to be added to decrease noise effects.

Overall, the circuit is useful for many optical data link applications, with good input sensitivity and wide dynamic range. This performance extends up to bit rates of 600Mbaud.
REFERENCES


Edward Eugene Campbell was born on July 31, 1962 to Howard R. and Marilyn K. Campbell in Harrisburg, Pennsylvania. He graduated 4TH in his class on June of 1980 from Newport High School, Newport, PA. Afterwards, he attended Harrisburg Area Community College while working part time as a mechanic and gas station attendant. Ed earned the degree of Associate in Arts for Electrical Engineering with high honors in May of 1982. He then transferred to the Pennsylvania State University - Harrisburg Campus. Here he was a student member of the IEEE and received the degree of Bachelor of Science in Electrical Engineering Technology with honors in May of 1984.

After graduation, Ed began to work for AT&T Bell Laboratories in Reading, PA in June 1984 as a Senior Technical Associate. His initial assignments involved reliability, production testing, and design of Bipolar-CMOS-DMOS (BCDMOS) High-voltage ICs.

He began work on the degree of Master of Science in Electrical Engineering at Lehigh University, Bethlehem, PA, and later transferred into the Analog ICs for Lightwave Design Department doing Failure Mode Analysis on Optical Data Link ICs. He was promoted to Member of Technical Staff-1 in November of 1990. In October of 1991, Ed was married to the former Lori J. Enck, the daughter of Robert and Jan Enck. Ed is scheduled to receive his MSEE degree in January of 1992.