An accelerated test method for electromigration in integrated circuits

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AN ACCELERATED TEST METHOD FOR ELECTROMIGRATION IN INTEGRATED CIRCUITS

by

Paul Andrew Uliana

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ABSTRACT

As integrated circuit geometries continue to shrink, current densities in metal interconnects are increasing. Because of this, electromigration is an issue that is becoming a great concern in the industry. In previous years this problem was known about but was often ignored because it did not pose a threat to circuit quality. Engineers are now discovering that this is a reliability problem that demands serious attention.

This work examines this issue and recent work relating to it. Investigating the literature reveals that there is much disagreement on electromigration theory and testing methodologies and that very few standards are now accepted. Building on research of previous works the author has developed a new test method. The author then uses this method to develop a computer controlled test system that can test the quality of aluminum interconnects based on the theory of metal migration. Experiments show that the test system is accurate and fast as well as easy to use. It is demonstrated that electromigration testing which commonly takes several weeks is now accelerated to the fastest possible limit of tens of seconds. Because of its accuracy and speed, it has the potential to be used as a continuous process line monitoring tool capable of finding inferior metal thus helping to insure high reliability circuits.
1. INTRODUCTION

As a current flows through a metal conductor an interesting phenomena may occur whereby atoms of the conductor are physically moved by the momentum of the charge carriers. This process is referred to as electromigration and the study of it has been progressing for a long time. As early as the 1860's electromigration has been noticed in liquid alloys. Some early studies documented the movement of markings on gold wires subject to a current stress. In the late 1950's and early 1960's many of the mathematical formulas used to describe electromigration began evolving. During the 1960's the use of thin film conductors in integrated circuits became widespread. At this time electromigration induced failures began to appear on electronic devices.

An occurrence of an electromigration event can result in two basic types of failure modes in integrated circuits. The first is the development of voids which leads to opens. As the void begins to form the local conductor width decreases. This results in the local current density increasing which further accelerates the metal migration until catastrophe. The second failure mode results from the formation of hillocks. These hillocks extrude from the sides of the conductor and have the potential to cause shorts to nearby metal lines. Other failure modes such as diffusion of Si in Al causing high resistance contacts have also been identified. The observance of these failures threatened to limit the success of the entire electronics industry. Because of this, there began an increased interest in the topic in order to better understand what was going on.

In integrated circuits, one of the consequences of shrinking linesizes and increasing circuit densities is that interconnects are required to carry higher current densities. The average
lifetime of a metal line has been shown to have approximately an inverse square relationship on current density - as the current density doubles the lifetime reduces by about a factor of four. In many cases, metal lines are no longer predicted to have lifetimes in the hundreds of years but now these lifetimes are approaching unacceptable sub-twenty year values. Semiconductor manufacturers now have an increased interest in electromigration because their success depends on their commitment to supplying devices that are reliable. Some applications such as military electronics, satellites, avionics, medical electronics, etc. must demand high reliability from their suppliers.

In the early days of integrated circuits, it was generally believed that designing conductors wide enough to assure that current densities would not exceed the latest "rule of thumb" limit was a straightforward task. As the technology advanced, the industry realized the problems with this thinking.

1. Simulating circuits to determine what maximum current densities are present in a conductor at any time of operation was hard to do. As simulation tools became more sophisticated and quicker, circuits were also becoming more densely populated with components. More components meant the number of conductor paths and the number of possible states of the circuit increased by orders of magnitude.

2. "Rule of thumb" guidelines for current densities (commonly $1-2 \times 10^5$ A/cm$^2$ for aluminum films and $5 \times 10^5$ A/cm$^2$ for aluminum alloys) were not well understood. Several guidelines became more refined to include metal of varying linewidths, pulsing currents and other effects. As a result of many reliability studies, engineers were beginning to question the validity of these limits. Some results were suggesting that smaller allowable current densities must be used. These suggestions do not please designers who are pushing for maximum component densities on minimum silicon real estate.
Historically, integrated circuit densities have doubled every 18 months. Because of extensive geometry scaling, the issue of electromigration is beginning to get much more serious attention. To understand why, one should look at what is happening to conductor currents. As the thickness and widths are scaled by $\lambda$, the cross sections are thus scaled by $\lambda^2$. But what is happening to $I = C \frac{dV}{dt}$? Capacitance ($= \frac{WLC}{t_{ox}}$) would appear to reduce by $1/\lambda$ but in reality designers are packing chips with more devices and thus conductors now have much higher fanouts forcing capacitances back up. Because circuit complexities are increasing, line length does not scale by $\lambda$ since in reality longer lines will be needed to connect between several devices.

Voltage change ($dV$) remains constant because of limitations imposed by systems (5 Volts). In addition, system designers are forever greedy for the highest speeds possible ($dt$ small). With all these factors taken into consideration one can see that current densities are becoming much greater due to scaling. Moreover, chip power is increasing (especially dynamic power in VLSI CMOS) resulting in higher device operating temperatures. Electromigration is believed to have an exponential dependence on the inverse of temperature. Because of this and the inverse square dependence of current density, the above comments lead to the conclusion that electromigration should now be a very important issue and one that will become more of a problem in the future.

To guaranty high reliability, manufacturers must now monitor metal quality continuously. To do this an effective testing method is needed which will be accurate and economically feasible. It should be able to determine process variations that will effect metal lifetimes so that the processing can be tightly regulated and enhanced.

This paper will examine what we understand about electromigration today and what measures have been taken to prevent it. The effectiveness of these measures will be investigated. In order to study this long term reliability problem it is important to be able to test for it. One of the largest obstacles in research has been how to effectively test for resistance to
electromigration. Because of this, the different testing methods currently used will be presented and discussed. In response to the need for a better testing technique, the author developed a type of test that is fast and effective. The system needed to implement the test has also been built and proven along with associated software control.
2. ELECTROMIGRATION IN ALUMINUM INTERCONNECTS OF INTEGRATED CIRCUITS

2.1 Theory

The process of electromigration refers to material transport as a result of the interaction between charge carriers flowing through a conductor and the atoms of the conductor. As conducting electrons (or holes) travel through a metal they exchange momentum with atoms of that conductor. If the current density is great enough and the physical properties of the metal allow it, this momentum transfer will result in the creation of vacancies and/or build up of metal atoms. These build ups are sometimes referred to as "hillocks." The force which causes this material transport, namely the interaction between the ions and flowing electrons, is usually referred to as the "electron wind." The electrostatic interaction between the ions of the metal and the electric field is also a force resulting in material transport but the electron wind is the prevailing cause of movement in materials that are highly conductive.

The phenomena of electromigration can be described as a lattice diffusion process in bulk material. The net atomic flux \( J_A \), due to electromigration can be expressed as

\[
J_A = N \frac{D}{kT} Z^* qE = N \frac{D}{kT} Z^* q \rho j
\]

where \( N \) is atomic density of ions, \( D \) is diffusion coefficient \((=D_0 e^{-Q/kT})\), \( Z^* q \) is the effective charge on diffusing ions, \( k \) is Boltzmann's constant, \( T \) is temperature, \( \rho \) is the resistivity, \( j \) is the current density through the conductor and \( E \) is the electric field \((=\rho j)\).
In the case where the conductor is a thin film, the occurrence of lattice diffusion is negligibly small compared to grain boundary diffusion. In integrated circuits, metalization is deposited as thin films with relatively small grain sizes making grain boundary diffusion the dominant process. For this reason, experiments on thin film conductors generally use relatively high current densities and low temperatures which minimize the probability of lattice diffusion. The expression for atomic flux of metal ions can be modified for electromigration due to grain boundary diffusion using the subscript $b$

$$J_b = N_b \frac{\delta D_b}{d} Z^* q \rho j$$  \hspace{1cm} (2)$$

where $N_b$ is now the local density of ions in the grain boundary, $\delta$ is the effective width of the boundary, $d$ is the average grain size, $D_b$ is the grain boundary diffusion coefficient.\(^1\)

Electromigration in thin film conductors cannot occur unless there exists a source of flux divergence of ions. Two major causes are recognized as the source of flux divergences: temperature gradients and structural irregularities in the film. An expression for divergence of flux, $\nabla \cdot J_b$, can be written to take into account temperature gradients $\nabla \cdot T/T$, and structural irregularities. Three structural irregularities are identified as sources of flux divergences in grain boundary diffusion.

The first of these irregularities is grain boundary mobility where a change in ion mobility between grain boundaries causes a divergence in the flux of vacancies. Metal deposited as a thin film will assume a crystallographic orientation of grains, that is, the grains that make up the film will tend to have a dominant orientation. The direction of this orientation can be changed by using different methods of metal application. Grain boundary mobility is related to the crystallographic orientation of the metal deposition.\(^2\) Thus, altering the orientation will
lead to changes in the probability of grain boundary mobility. For example, metal deposited in the <111> orientation has been shown to be more resistant than other orientations to migration of atoms. The second source of inhomogeneities are triple point divergences. Triple points are regions where three grain boundaries with different transport properties meet. The relative contribution of this effect is related to the angles that grain boundaries have with the electric field. For this reason, changing the crystallographic orientation of grains in the film will also have an effect on flux of vacancies arising from triple points. Another source of irregularities is a change in grain size. Flux divergences will be created at boundaries where grain size changes from large to small and charge carriers will transport ions from this small grain area and create voids. This effect can be minimized by using films with known orientation rather than a random one.

Figure 1. Two types of structural irregularities that are sources of flux divergences: a) triple points and b) change in grain size.
Temperature gradients, unrelated to the physical structure of the film, are also a factor that generates atomic flux divergences. Depending on the direction of current flow, temperature gradients will promote mass transport. Where the electron flow is in the direction of increasing temperature, vacancies in the metal can occur. Conversely, accumulations can be seen where temperature decreases in the electron flow direction.

\[ T_2 > T_1 \]

**Figure 2. Void and hillock creation caused by temperature gradients.**

In thin films, the effect of thermal gradients is usually not as important, due to the temperature stabilizing effect of the substrate (usually Si having a high thermal conductivity) which is generally in good thermal contact with the metal. Also, aluminum itself is a good thermal conductor. It has generally been found that electromigration tests on thin films result in failures that are randomly distributed across the length of the conductor thus confirming that temperature gradients are rarely causes of failure.\(^6\)\(^7\) Many studies on electromigration in thin films used as conductors in electronic devices have ignored the effects of temperature gradients in order to simplify the formulas. However, many authors warn that for long test structures the temperature gradients should not be ignored when developing electromigration tests.\(^8\) Buehler's
use of a thermal coupling matrix technique determined that over long structures, carrying
current densities in the range of \(2-3\) MA/cm\(^2\), the change in temperature can be as much as
20\(^\circ\)C.\(^9\) Figure 3 is an typical example of this temperature profile.

![Temperature profile graph](image)

**Figure 3.** Temperature profile of a long segment under current stress.

Under normal use, metal lines would not experience this degree of temperature
variations. Therefore, it is important to maintain a constant temperature across a conductor
during accelerated electromigration testing to insure valid results. Some studies have attempted
to correct this by constantly monitoring the line temperature and varying the wafer temperature
to compensate but this is difficult and can take much time.

One way to avoid these gradients is to break up the long test structure and insert wide
pieces of metal in between each segment to act as heat sinks. This approach has been taken in
designing the structures of this study. LaCombe and Parks have shown statistically and
experimentally that testing a segment of length \(L\) is the same as testing \(n\) segments each of
length \(L/n\).\(^{10}\)
2.2 Equations

Along with describing the process and some of the causes of electromigration, researchers have been looking for accurate models which could be used to predict failures. One of the most widely used equations is an empirically derived Arrhenius type formula sometimes referred to as Black’s equation.\(^{11}\)

\[
MTF = A J^{-n} e^{E_a/kT} \quad (3)
\]

where MTF is the median time to fail and the other parameters will be described below. Venables and Lye\(^{12}\) have derived a statistical model beginning with the velocity of atomic migration from Huntington and Grone:\(^{13}\)

\[
v = j\rho Z^* q \frac{D_o}{kT} e^{-E_a/kT} \quad (4)
\]

where parameters are similar to equation (2). The term \(j\rho Z^* q\) can be described as the driving force of the electron wind and the rest of the expression accounts for the temperature dependent mobility of atoms. Using the understanding that electromigration voiding occurs as a result of structural irregularities as described above, these authors derived an expression for this increase in voids over time

\[
\frac{\partial p}{\partial t} = Cn \rho o \left\{1 + \alpha (T-T_o)\right\} \frac{j o}{1-\rho} \frac{D_o}{kT} e^{-E_a/kT} \quad (5)
\]

Here \(p\) is used to mean porosity or voiding. The temperature is also a function of the current density (which is a function of \(1-\rho\), the cross section of the remaining material) and the
Substituting this expression for $T$ into (5) and using the definition $x = 1 - \frac{T}{T_0}$ results in a differential equation that can be solved to give an expression for the time to failure

$$T_F = \frac{1}{2Cn} \left\{ \frac{\tau_o kT_o}{j_o \rho_o D_o e^{E_a/kT}} \right\} \int_{x_o}^{x_1} \frac{e^{-E_a/kT}}{x^2(1-x+x\alpha T_0)} \, dx \quad (8)$$

The complexity of this equation has hindered its widespread use in subsequent research. In application, the Black equation has proved to be a very accurate model for many studies.

Although experiments have shown that equation (3) is an effective model, there is not common agreement over the parameters used. Some comments about each of these parameters will help explain how to apply the model.

1. MTF - mean time to fail.

This is also referred to as MTTF, $T_{FE}$ or $T_{50}$. MTF refers to the time at which 50% of product will fail. In order to prove models, experiments often stress a sample of $N$ devices at a constant current and temperature to determine the $T_{50}$ for that sample as in Figure 4.
Figure 4. Experimentally determining $T_{50}$.

The straight line in figure 4 indicates a lognormal failure rate. This rate has a standard deviation, $\sigma$. Knowing $T_{50}$ and $\sigma$, the probability density function, $f(t)$, can be used to determine the probability that a device will fail during a small time $dt$ at $t$, given by

$$f(t) = \frac{1}{\sigma t \sqrt{2\pi}} \exp \left\{ \frac{(\ln t - \ln T_{50})^2}{2\sigma^2} \right\}$$ (9)

Reliability engineers find it more useful to express failure rates in terms of FITs where 1 FIT = $10^{-9}$ failures per device hour. This instantaneous failure rate in FITs is then

$$\text{Failure Rate} = \frac{10^9 f(t)}{1 - \int_0^t f(\tau) d\tau}$$

When $t \ll T_{50}$, then the integral is small and the instantaneous failure rate is $f(t) \cdot 10^{-9}$. 

13

Because many effects are generally lumped into this one constant, it must be empirically determined. It will take into account geometry; physical characteristics of the film, passivation and substrate; resistivity; electron free path; average electron velocity; effective ionic scattering cross section; statistical distribution of inhomogeneities which cause flux divergences; etc. Some authors have further quantified it by using it as a function of activation energy\(^{14}\)

\[ A = A_0 e^{-bE_a} \]  

(10)

3. J - Current density

\[ J = \frac{I}{wt} \]  

where \(w\) and \(t\) are width and thickness of conductor and \(I\) is the current.

4. n - Current density factor

When equation (3) was introduced, \(n\) was found to be equal 2. Since then many studies have found this value to be typical while other authors have reported values of \(n\) in the range of \(1 - 5^{15,16}\). The reason that numerous studies have been conducted to determine \(n\) is its exponential effect on MTF— the difference between \(n = 1.75\) and \(n = 2\) can be a 20 times difference in MTF. It has been found that for flux divergences caused by structural inhomogeneities a value of \(n\) closer to 1 should be used and if the cause is mainly due to temperature gradients then \(n\) closer to 3 is more accurate. This follows the observation that by using substrates or passivation with lower thermal conduction capabilities the heat will not be dissipated as quickly, temperature gradients will be more important and the value of \(n\) increases.\(^{17}\) A model incorporating both effects agrees with experimental results of \(n = 2\) or slightly less than 2.\(^{18}\) Studies have also indicated that \(n\) will be different depending on the type
of failure mode that is generated. Because the current density has a complex dependency on many factors, it has been advised not to rely on a single power, $n$, for experiments using different current densities, geometries, and film materials. For example, some workers have investigated the relation between the magnitude of current density used and the value of $n$ observed. In the range of $J = 1 - 2 \times 10^6 \text{ A/cm}^2$ almost all papers report $n$ close to 2. For smaller $J$ the value of $n$ decreases to 1. When values of $J$ greater than $2 \times 10^6 \text{ A/cm}^2$ were used $n$ has been reported as high as 4 - 5. Further, $n$ increases very quickly for current densities above $2 \times 10^6 \text{ A/cm}^2$ and slowly for $J$ below $5 \times 10^5 \text{ A/cm}^2$. Figure 5 is a graph representing this trend. Data for this figure is the average value of $n$ as taken from many sources.

Figure 5. An estimated trend of $n$ vs. $J$ as derived from data in the literature.
This curve fits a relation of

\[ n = e^{aJ+b} \]  \hspace{1cm} (11)

where \( a = 24 \), \( b = 0.37 \) and \( J \) is in \( \times 10^6 \text{A/cm}^2 \). This relationship applies for values of \( J \) in the range of \( 5 \times 10^5 \text{A/cm}^2 \) to \( 4 \times 10^6 \text{A/cm}^2 \) which is the typical range for electromigration testing. Below this range \( n \) should approach a limit of 1 (mean time to fail has a linear dependence on \( J \) for small \( J \)) and this is not predicted by this model. The procedure used to find \( n \) from experimental data is to measure the time to fail on a lot of \( N \) devices stressed to current density \( J \). Then find the time when 50\% of \( N \) fail and call it \( T_{50} \). Repeat for similar lots over a small range of different current densities and extrapolate a graph similar to Figure 4. The slope gives \( n \).

![Graph showing the current density dependence of time to fail](image)

**Figure 6.** Experimentally determining the current density dependence, \( n \).
5. **Ea - Activation energy.**

Activation energy is related to the energy of diffusion of atoms. The effect of temperature on the reaction rate in chemical or diffusion processes is often found to exhibit the Arrhenius relation:

\[ \text{Rate} = A e^{-Ea/kT} \]

(12)

This relation has been used to describe the temperature dependence on the rate of the electromigration process in equation (3). In electromigration studies on Al films the activation energies range from 0.45eV to about 1.4eV. The value of Ea for bulk Al (not thin films) is approximately 1.4eV. This can be measured by recording the amount of mass transport per time at several temperatures. Various studies have measured this mass transport with TEM or SEM observations, electron microprobe analysis, or changes in resistance. Another technique used to measure Ea is to measure the change in rate of resistance increase due to a rapid change in temperature at a constant current.\(^{21}\) The reasoning here is that a change in resistance is caused by accumulation of a temperature activated defect that has an activation energy for diffusion, Ea. Then, if the temperature changes from \(T_1\) to \(T_2\), the slope of the resistance curve will change according to

\[ \frac{\dot{R}_{T_1}}{\dot{R}_{T_2}} = \exp \left( \frac{-Ea}{k} \left( \frac{1}{T_1} - \frac{1}{T_2} \right) \right) \]

(13)

In electromigration studies, a common way to measure Ea is to stress a sample of N devices at temperature T and current density J to find \(T_{50}\) for this sample. This is repeated with similar samples at the same J and with different T's. A graph like figure 7 is drawn and the value of Ea is represented as the slope.
Data fitting a straight line verifies the Arrhenius relation. A change in the slope of this curve can be seen if data is taken for temperatures greater than about 350°C. At these temperatures, lattice diffusion begins to become important and $E_a$ approaches that of bulk Al. Further experiments revealed that $E_a$ is not only a function of metal structure but also of current density. That is, the slope of figure 7 becomes smaller for larger current densities.

Partridge and Littlefield\textsuperscript{22} have suggested using $E_a$ as a function of $J$

\[
E_a = E_{am} - \beta J \tag{14}
\]

where $E_{am} = E_a$ for bulk Al, and $\beta = \text{a coefficient in } \frac{eV \cdot \text{cm}^2}{A}$ was found to be $3.6 \times 10^{-7}\text{eV/J}$.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure7.png}
\caption{Experimental data to determine activation energy, $E_a$.}
\end{figure}
6. \( T = \) Temperature of the conductor. (K)

Stressing a metal line with a high direct current density (>5 \( \times \) \( 10^8 \) A/cm\(^2\)) will result in Joule heating of the line. This means that the temperature used in equation (3) is no longer the ambient temperature. Calculating the conductor temperature becomes one of the major problems in electromigration testing. Due to the exponential it is important to very accurately calculate \( T \). For example, an error of only 5°C in a temperature reading of 270°C can produce a 30% error in MTF. The amount of the conductor's change in temperature at a current density \( J \) depends on the thermal conductivities of the insulators surrounding it. Let \( \kappa_{i\text{-thermal}} \) (\( \text{watts/cm\cdot°C} \)) be the thermal conductivity of the SiO\(_2\) of thickness \( t_i \) under the conductor of sheet resistance \( \rho_s \), width \( w_c \), and length \( l_c \) (SiO\(_2\) is about 100 times worse as a thermal conductor compared to silicon). The change in temperature is then

\[
\Delta T = \frac{\text{Power}}{\text{conductor area} \cdot \kappa_{i\text{-thermal}}} \quad (15)
\]

\[
\text{Power} = \rho_s J^2 w_c l_c \quad (16)
\]

\[
\Delta T = \frac{\rho_s J^2 t_i}{\kappa_{i\text{-thermal}}} \quad (17)
\]

The most commonly used method to measure change in metal line temperature is by measuring the change in resistance. Resistivity of a metal is mostly caused by collisions of the conductor electrons with phonons. At increased temperature the number of phonons increases thus causing the resistivity to increase. A simple experiment can find the thermal coefficient of resistance, \( \beta \), to fit the expression

\[
\Delta T = \frac{R - R_o}{\beta R_o} \quad (18)
\]

relating the measured change in resistance to a calculated change in conductor line temperature.

7. \( k \) - Boltzmann's constant = \( 8.62 \times 10^{-5} \) eV/K (or \( 1.38 \times 10^{-23} \) Joule/K)
2.3 Current Research and Methods used to Alleviate Electromigration

Through the years of research on electromigration in integrated circuits, many new methods have been developed to combat this threatening phenomena. Some studies explain successful technology changes that greatly increase lifetimes of metal lines. Other experienced people are not quite so optimistic and state that new breakthroughs are needed and the problem will continue to require increased research efforts. Some of the more significant findings will be summarized below.

It should be noted that software engineers have also begun to attack these problems. Circuit designers are realizing that modifying conductor widths based on calculations using number of devices, average current per device and rule of thumb current densities is not enough to assure customers the highest reliability. Very recently several new software tools have emerged that claim to be able to accurately simulate worse case current densities in critical paths or power buses at any time of circuit operation. The thrust here is to provide SPICE-like current waveforms on entire CMOS VLSI circuits under any input vector stimuli. Clever algorithms are needed to do this with reasonable processor time. No doubt more of these simulations will be developed in the upcoming years.

Alloying

One of the most commonly used ways to combat electromigration is the addition of another element to aluminum. A myriad of papers document the results of alloying with different concentrations of Si, Cu, Ni, Cr, Mg, Ag and Au. Combinations of these have also been tried. Great increases in MTF have been seen with each of these excluding Ag and Au which showed nominal success. The combination of Al-Cu-Si is currently used extensively in
different recipes throughout the industry because of its relatively low cost and very high increase in MTF.

Cu atoms, being heavier than Al, are not as easily moved under the force of an electron wind. It has been shown that copper doping increases MTF about 50-70 times but does not change intrinsic properties of the aluminum line such as activation energy.\textsuperscript{26,27} Likewise, the current density and temperature dependence on MTF appears to remain the same after copper doping.

One of the reasons Al is doped with Si is the fact that Si dissolves in Al. When a contact between Al and Si is heated above about 250°C the Si quickly dissolves into the Al through a diffusion process until the solution reaches a saturated state. Diffusion of Si is about 50 times greater in thin film Al than in bulk Al. The solvus curve of the Al-Si phase diagram (Figure 8) defines this maximum solubility versus temperature.

When the dissolved Si cools, it precipitates leaving a conductive Al-Si crystal mixture. Dissolved Si at Al-Si contacts leaves behind pits in the Si at the negative contact. The Al is then able to spike through these voids and permit leakage to the substrate. Alternately, an increase in resistance can be found at the positive terminal due to build up of higher resistance silicon. Predissolving Si in Al will help control this problem. An alternative solution involves the use of a barrier metal such as tungsten or platinum between the Al and Si.\textsuperscript{28}
Figure 8. Al-Si phase diagram

Figure 9. $T_{50}$ results for Al vs. Al 4% Cu with $T = 175°C$, $J = 4 \times 10^6$. From reference 27.
Some fabrication processes introduce alloying by means of a sandwich process. For instance, copper doping can be achieved by depositing a layer of Al then a layer of Cu followed by a third layer of Al and then annealing the sandwich. Other processes laminate another metal of lower conductivity in between two Al based metals. When the inter-Al layer is one that is more resistant to migration (Ti for example) then this laminated structure can help prevent failures due to opens. This structure does not prevent the formation of extrusions which can become shorts.

Method of Metal Application

The method of applying the metal has also been shown to effect the resistivity to electromigration. Applying metal using an e-beam evaporator (e-gun) has about a 10 times greater MTF than using sputter gun deposition.

Figure 10. Distribution of electromigration failures for e-gun vs. sputtered Al.

From reference 31.
The main reason for this is that sputtered films have relatively random grain orientation and sizes — things which lead to more locations of flux divergences. The metal lines deposited by e-beam have a more uniform grain size with larger grains and a dominant orientation (usually \(<111>\)).

**Effect of Grain Size**

Larger grain sizes mean fewer grain boundaries which can initiate metal migration. Increasing grain size has been shown to linearly increase MTF. With larger grain sizes, the probability of lattice diffusion becomes non-negligible as compared to grain boundary diffusion. Thus, there is an apparent increase in activation energy associated with larger grains. Using the annealed sandwich structure explained above results in very large grain sizes.

**Line Width**

Many studies have investigated the effect of varying the interconnect line width on electromigration resistivity. The results of all these studies indicate that as stripe width increases then the MTF also increases in a somewhat linear fashion. Simply put, there must be a greater amount of metal moved before a void can create an open across a wider metal line. However, as the stripe width is decreased to less than a few times the average grain size then MTF begins increasing. The minimum MTF occurs at a width of about 3-5 times the grain size as shown in figure 11.
Figure 11. $T_{50}$ varies linearly with line width until the width approaches the median grain size.

When the line width is less than the average grain size then there is a "bamboo" type structure.\textsuperscript{31} The bamboo structure is very resistant to metal migration since the number of triple points and other structural inhomogeneities becomes very small. This is one characteristic of VLSI devices that is more promising in terms of electromigration. In VLSI the bamboo line is often achieved by e-beam evaporation giving narrow metal lines of very large grains having a preferred orientation.

There has also been a study demonstrating that the MTF has a much less pronounced dependence on line width when a pulsed dc current is used with a small duty cycle as compared to a constant current.\textsuperscript{32}
Pulsed dc Current

All of the experiments on electromigration in aluminum mentioned up to now have involved stresses from continuous dc currents. In real integrated circuit applications currents through conductors are often pulsing at various frequencies. In order to relate the experimental results to real circuits, the assumption is usually made that only the on time will be included in the MTF. That is, the lifetime increases linearly with the reciprocal of the duty cycle. This assumption has been the topic of closer scrutiny by many people who have found that it is not strictly correct. As expected, the lifetime does improve as duty cycle decreases but the amount of increase in lifetime has been shown to be greater than the ratio of on time would predict. The explanation of this is that during the off time there is some recovery from damage that takes place. A time constant, \( \tau \), has been associated with this void concentration, \( n(t) \). This is believed to be due to other early stages of metal migration happening a short distance away which tend to feed (relax) these voids. When the pulsing frequency is smaller than \( 1/\tau \) then the assumption of total on time to determine the lifetime is valid. When the frequency is greater than \( 1/\tau \) (and this may be in the kHz range) then the concentration of voids that feed the relaxing vacancy over time is found to be inversely proportional to the square of the duty cycle. This relation is explained by the reasoning that for pulses shorter than \( \tau \), \( n(t) \) is approximated by a triangular waveform and \( \int n(t) dt \) is proportional to the square of the on time.\(^{33}\) Figure 12 displays some experimental results showing this effect.
Passivation

The use of an overglass protection layer will increase the MTF of an integrated circuit. This effect has been studied by many authors but there still is not a very good understanding. It is generally agreed the mechanical force that the rigid passivation layer exerts on the metal conductor acts to inhibit hillock and void formation. The compressive stresses of the overglass retard the migration of metal. There have been a few experiments that contradict this theory but the following results tend to support it.

1. When passivation thickness is increased, thereby increasing the force that this layer exerts on the conductor, the MTF was found to increase.\textsuperscript{34}

2. With a constant overglass thickness a hydrostatic pressure analogy suggests that reducing the thickness of the conductor will effectively cause a greater pressure from the glass on the metal. This should retard migration. Indeed, experiments have shown that MTF does increase if this procedure is followed.
3. Introducing a defect (pinhole, crack) in the passivation above the metal line will relieve some of the stress in the line local to this defect. This should give rise to a greater probability of electromigration failure at this location. In experiments, intentionally induced defects have shown this increase in electromigration failures.35

4. Varying the type of passivation used from less rigid to more rigid does increase the MTF as predicted.36
These stresses induced by the passivation oppose the movement of metal. In addition, metal that has been moved will disturb the stress distribution equilibrium such that the overglass will, to some degree, tend to redistribute metal towards its original location thus relaxing the void or hillock formations. This effect might show large improvements in MTF under pulsed dc conditions where the conductor is able to relax between each cycle. To the author's knowledge, this theory has neither been suggested nor researched to date.

While the factors described above all have some effect on electromigration lifetimes, it is important to understand the relative contribution of each one. Before changing a process to enhance electromigration resistivity, something must be known about how much improvement will be gained by the change. This is especially true if there are trade offs associated with the change (increased metal resistance, increased processing costs, etc.). Burkett and Miller\textsuperscript{37} have investigated the relative contributions of several parameters on electromigration. After analyzing the results of several experiments they proposed empirically derived modifications to equation (3) that include many variables. Si-Al lines, for example, were found to obey the following relation.

\[
MTF = 4.47 \times 10^{12} \cdot \exp\left\{6.19(TP) - 2.41(\ln(J)) + .69(GN) - .39(t) - .21(w) - .19(GLASS)\right\} \quad (19)
\]

Where: \( TP = 1000/\text{Temp(K)} \)  \( t = \text{metal thickness (kÅ)} \)
\( J = \text{Current Density (A/cm²)} \)  \( W = \text{line width (µm)} \)
\( GN = \text{Grain Size (µm)} \)  \( GLASS = \text{Glass thickness (kÅ)} \)

One result of their efforts was that out of all parameters, grain size seemed to have the most impact on MTF.
3. TESTING FOR ELECTROMIGRATION

There is a type of disease now becoming very common in the semiconductor industry. Its name is electromigrationphobia. Victims are often heard asking the same question: “How reliable is our metal?” Physicists have struggled with this question and have come up with many theories and equations but these theories are not enough to cure the problem. Because of the many parameters involved in electromigration, the only way we have to really answer this question is by statistical analysis of actual test results. The real engineering problem then is developing accurate and efficient test methods. In the past there have been many different types of tests used. Some of the more popular ones will now be explained along with comments on advantages and disadvantages of each.

3.1 Constant Current Test

The most frequently used test to determine electromigration lifetime in thin films is the constant current test. The basic strategy is to stress test features on a group of devices using a constant current and measure the time when 50% of them fail. Current densities used are usually in the range of $2 \times 10^5$ A/cm$^2$ to $2 \times 10^6$ A/cm$^2$. This is currently the standard test method used in almost all types of experiments. Some of the major drawbacks associated with it are:

1. A constant current causes joule heating of the metal line and changes in line temperature can exponentially change the metal lifetime.

2. If the current is kept low enough to avoid joule heating then a great amount of patience is needed because the measured time to fail will be very long.

3. In order to get good correlation, a large number of devices must be tested.
Although automated test systems can easily be set up to perform the test, this increases the test cost and the waiting time is still painful. To make matters worse, if a sample of N devices is tested it is not good practice to stop after 50% of them fail for electromigration and call this $T_{50}$ because this can produce error. It is important to finish testing until greater than 90% fail and apply linear regression analysis to the log normal data.

In a constant current test there are also other ways to measure electromigration besides measuring $T_{50}$. $T_{50}$ is the time when 50% fail due to electromigration that is so severe that it has caused opens (or shorts). It is also possible to measure the amount of mass transport directly. This means measuring the volume of mass that has moved under the influence of a constant current. This can be done by observation with transmission electron microscopy (TEM), scanning electron microscopy (SEM) or using electron microprobe analysis. This has the advantage that you don't have to wait until failure but measurements are visual and, therefore, prone to error.

Another method that can be used to measure the migration of metal is measurements of conductor resistance over time. This change in resistance is believed to be mainly due to the mass accumulation and depletion across the stripe. Assuming this is true, the fractional change in resistance over time can be related to the ion migration in a conductor of length $l$ by the relation:

$$\frac{\Delta R}{R_0} = C \frac{v_s l}{l}$$  \hspace{1cm} (20)

where $v_s$ is the ion velocity and $C$ is a constant found to be typically close to 1 for thin films. With automated test equipment, $\frac{\Delta R}{R_0}$ is easy to measure accurately. The calculated value of $v_s$
averaged over the length then gives a measurement of metal migration. A problem with this technique is that a change in resistance can also be due to other changes in metal structure besides migration.

Although the change in resistance method has been a very common procedure, evidence has proven that it is not a very reliable indicator. If one were to plot the change in resistance from the beginning of current stressing until the point of aluminum line failure due to open circuit one would not find a continuously increasing curve. During this time several random large increases in resistance may be found followed by random decreases of comparable magnitude. It is believed that during these periods of decreasing resistance the metal line is healing from either temperature expansion closing voids or other atom migration upstream feeding the voids. Experiments indicate that the line can locally open and heal several times before complete failure.

3.2 Constant Temperature Test

Temperature control is one of the most challenging obstacles in achieving an accurate constant current test. Under the influence of the same current density, two identical interconnect lines on different devices may exhibit different increases in temperature due to joule heating. This variation comes from small differences in geometries, composition or other properties. This limits the ability to obtain accurate results from constant current electromigration experiments on a sample of devices. In order to account for this problem it is important to either somehow maintain constant temperature from device to device or to measure the resulting temperature and normalize all results to one temperature.

One way to stress each device to a constant temperature is to somehow measure or calculate the metal line temperature and then adjust the external device temperature so that the
joule-induced rise in temperature plus the device temperature always equals the target line temperature. The conductor temperature can be measured having knowledge of the resistance versus temperature curve. Another method which has been tried with minimal success was placing diode type temperature sensors near the line under stress.\(^{39}\) One problem of this test is the difficulty in accurately measuring line temperature. Another drawback is that extra hardware is needed to accurately and automatically control the temperature of the device under test. If this hardware is available it is then still very difficult to precisely know the effect of the external temperature on the line under stress. This is limited to one’s knowledge of the thermal resistance characteristics of the line to substrate to package (or wafer chuck) network.

In an effort to reduce the test time, another type of isothermal electromigration test has been proposed. It has been named the wafer-level isothermal joule-heated electromigration test or WIJET.\(^{40}\) In thin film studies it is important to observe migration effects due to grain boundary diffusion rather than lattice diffusion. To do this the test must not exceed a maximum metal line temperature, \(T_m\), found to be around 320 - 350°C (recall figure 7). The idea of WIJET is to find the stress current needed to achieve \(T_m\) and apply this current as quickly as possible. To determine this, a constant is needed relating change in temperature to change in resistance. This constant, \(\beta\), is then assumed to remain the same from wafer to wafer. Then the power into a line given by

\[
Q_{in} = I^2R = I^2(\beta T + R_o)
\]

(21)

is equated to the power dissipated by the line

\[
Q_{out} = C(T - T_1)
\]

(22)
using the thermal conductance C where \( T_1 \) is the ambient temperature. At \( T = T_m \) then \( I = I_{\text{max}} \) resulting in

\[
I_{\text{max}} = [C(T_{\text{max}} - T_1)/(\beta T + R_o)]^{0.5} \tag{23}
\]

Theoretically, stressing a line at \( I_{\text{max}} \) will give the maximum acceleration possible while staying under the temperature limit between lattice and grain boundary diffusion regimes.

### 3.3 Temperature or Current Ramp Tests

Another type of test uses a temperature ramp to derive information that can be used to predict electromigration resistivity. This test contends that change in resistance gives an indication of electromigration damage according to the relation

\[
\frac{1}{R_o} \frac{dR_{EM}}{dt} = A^T e^{-E_a/kT} \tag{24}
\]

where \( A^T \) is a pre-exponential factor and \( R_{EM} \) is the electromigration component of resistance. The resistance is known to be a function of both time and temperature and the electromigration component of resistance can be separated from the temperature component (the so called "Matthiessin’s rule") by the relation:

\[
R_{EM} = R - R_o (1 + \alpha \beta t) \tag{25}
\]

with \( \alpha \) being the temperature coefficient of resistivity and \( \beta \) being the rise in temperature with time.

The procedure for this test involves the use of a constant current source and a controlled ambient temperature that increases linearly with time. Data on the change in resistance with time and temperature is then collected automatically. The test is thus called the Temperature-
ramp Resistance Analysis to Characterize Electromigration or TRACE test. The data recorded is then manipulated to derive the kinetic electromigration parameters $A^T$ and $E_a$ during a test that only takes a few hours. $A^T$ is broken down into two components, $A$ and $C_1$, where $C_1 = j^2$ and $A$ is a corrected pre-exponential factor. Unlike conventional electromigration testing, TRACE does not give direct information on metal time to failure but the parameters can be used in the equation

$$MTF = C_2 \frac{\Delta R}{R_0} A j^{-2} e^{E_a/kT}$$

(26)

where $C_2$ is an empirical constant analogous to $A$ in equation (3) as described earlier. A value of $\frac{\Delta R}{R_0} = 10\%$ is assumed to correspond to conductor failure. By applying TRACE parameters to equation (24), different test structures can be compared with respect to their relative resistance to electromigration. This may be useful in determining the effects of using process or material variations on integrated circuits. One drawback of this technique is that the correlation between TRACE results and conventional MTF type test results is not well understood. Also, the analysis is not straightforward and the apparatus can be somewhat expensive. It has, however, been demonstrated as a very effective method for quickly and accurately measuring activation energies of individual metal lines.

A current-ramping test has also been implemented which is called the Breakdown Energy of Metallization (BEM) technique. It has been developed in response to the need for a very fast (~1 minute) wafer level test that does not require external heating. It results in a value of Median Energy to Failure (MEF) which gives information on electromigration resistivity. The energy idea is introduced in order to factor out unmeasurable process variables from the widely used MTF equation. MEF is energy per unit length which is MTF normalized to current and temperature. The BEM test involves integrating energy under a ramped current...
stress by using the equation

\[
\text{MEF} = \int_{t_0}^{t_f} \frac{I^2 R e^{-EA/kT}}{L} \, dt
\]

(27)

where \( t_0 \) is starting time, \( t_f \) is time of failure, \( R \) is the temperature dependent resistance and \( L \) is the metal length. During the ramp, a very high current density is reached. Under the influence of this great amount of joule heating it is important that the line temperature remains under the 350°C limit for grain boundary diffusion. This is done by measuring metal resistance to determine line temperature. The test has been shown to provide quick process monitoring information through a wafer level test.
4. THE STANDARD WAFER-LEVEL ELECTROMIGRATION ACCELERATED TEST

4.1 Introduction to SWEAT

It has been established that because geometries are shrinking, electromigration is becoming a more serious problem. Many manufacturers are realizing that expected metal lifetimes are approaching unacceptable limits imposed by reliability specifications. Because of this it is now more important to constantly monitor metal quality. Various electromigration tests mentioned above have the ability of monitoring some or all of the following:

1. Expected metal lifetimes
2. Poor step coverage
3. Effects of different metal compositions
4. Poor line width or thickness
5. Effects of grain size, passivation, method of application, current pulsing, etc.
6. Maximum allowable current density

Even though it is becoming increasingly more important to monitor each of the above items, the widespread application of these electromigration tests has been limited because they do not have the following desirable characteristics:

1. The test should be fast. Ideally it should be fast enough so that it can be used as a continuous process monitor.

2. The test should be easy. It should be easy to operate the equipment (automated so that an engineer isn’t required to run the test), easy to gather data (let the computer do everything) and easy to interpret the results (is the metal good or bad?).

3. The test should be at one temperature - preferably room temperature.
4. It would be best to test wafers rather than packages. It is cheaper to throw away bad wafers than bad packages and results can more quickly be fed back to the production line.

The SWEAT test (Standard Wafer-level Electromigration Acceleration Test) which was first introduced in 1985 by Root and Turner\textsuperscript{45} has the potential to satisfy all the criteria listed above. The author has taken the basic idea presented in the Root and Turner paper and developed new methodologies and theories that will make the test feasible and accurate. To prove this methodology, the author develops a SWEAT test system and the software needed to enable optimum operation under computer control. This paper will discuss this variation of the SWEAT test including details on how it was implemented and the results.

In conventional testing, the time to failure is measured for a line under the influence of a current stress. The SWEAT test differs because it sets the time to fail instead of the current and temperature. This is achieved by giving each line under test an \textit{equivalent stress factor} (ESF). The ESF is set at a level such that the average or baseline test structure will fail in \( t \) seconds under this stress. By doing this every test structure line is stressed equally. Structures that last greater than \( t \) seconds will be expected to have longer lifetimes than the baseline metal and those that fail in less than \( t \) seconds are inferior. Thus, the SWEAT test is really a comparison test. With the SWEAT system developed here the baseline metal is fully characterized to get information about its lifetime. Then, SWEAT is used to compare metal lines from other devices or other wafers to this baseline metal. If done carefully the test can be used to extract actual expected lifetimes of metal but the real advantage of using the test is as a line monitor to screen inferior product, not to determine a value for expected metal lifetimes.
Root and Turner point out that one problem with the constant current test is that lines which are more resistive appear to fail sooner because the temperature is much higher due to joule heating. In reality, some lines that are more resistive actually have longer lifetimes as in copper doped aluminum for example. The SWEAT test overcomes this problem by giving each line an equivalent stress. A similar problem with the constant current test is that lines with larger cross sections will be stressed with a lower current density and temperature. Again, the SWEAT test equally stresses lines even when the cross sections are different. These are a few of the fundamental problems with constant current test that are overcome by using SWEAT.

The basic idea of SWEAT is to control the joule-heated line temperature by adjusting the power density. To do this a power pulse is applied to the line and the resulting increase in line temperature is determined by measuring increase in resistance. Then, knowing the line temperature and power density, the stress factor is calculated. The power pulse is then adjusted until the target ESF is reached. This exact stress is then maintained through the entire test. The ESF is based on the familiar electromigration equation

\[ \text{MTF} = A \cdot J^{-n} \cdot e^{Ea/kT} \]  

(28)

During the test, I is measured and J is calculated as I/wt where w and t are the previously known width and thickness. If structures are tested which have w and t different than the predicted value then the MTF will be changed accordingly. Thus, the test results will give information about inferior line width and thickness (also related to step coverage).

The line temperature will be measured during the test and it will consist of the ambient, \( T_o \), plus the increase due to joule heating, \( \Delta T \). The resulting equation which will be used in SWEAT becomes
\[ \text{ESF} = S \cdot A \left( \frac{1}{w_l} \right)^n e^{E_a/kT} \]  

where \( S \) is an empirically determined constant used to relate the accelerated SWEAT results to time to fail data and \( T \) is the line temperature.

4.2 Test Structures

A series of test structures have been designed and manufactured to optimize the SWEAT results. The higher the probability that a structure will fail, the shorter the SWEAT test time will be. To increase the chances that a migration event will occur the line should be made very long. As mentioned previously, a long narrow test line is subject to large temperature gradients across the line (figure 3). In order to minimize these effects, several large heat sinks are periodically placed in the test line as shown in figure 14. Each of the structures used here has a total of 20 narrow lines separated by wide sections. The optimum width of the wide sections is still under investigation.

\begin{figure}
\centering
\includegraphics[width=0.5\textwidth]{sweat_structure.png}
\caption{Basic SWEAT structure.}
\end{figure}
At the ends of the structures bond pads are attached in order to allow probing. Because there is a finite voltage drop from the test structure to these bond pads, additional pads (Kelvin pads) are placed very close to the ends of the structure (see figure 15) to achieve the most accurate voltage measurements.

These structures were fabricated on both the first and second levels of metal interconnect in a two level metal 1.25um CMOS process. Minimum dimensions were used for the narrow portion of the test lines. Metal 1 and metal 2 thickness and minimum width are different and the SWEAT software does account for this.

All structures were also designed with extrusion detectors. This consists of running a metal line along both sides of the SWEAT feature at a minimum spacing. These lines are then connected to a bond pad. When hillocks form on the sides of the SWEAT conductor line they may reach the nearby extrusion detector. This will result in a short between the SWEAT structure and the extrusion detector. These can be seen in figure 15.

Another structure called a control structure was designed to help in characterizing the test. This is the same as figure 13 with all the narrow portions removed. Its use will be described later.

To examine the effect of metal step coverage on electromigration resistance, structures were developed that contained perpendicular poly or metal lines on levels under the narrow line of the SWEAT structure as shown in figure 16.
Figure 15. Layout of metal-2 SWEAT structures. On the left is the standard SWEAT structure and on the right is the structure with topography under the narrow lines. Extrusion detectors are also shown on both.
At the ends of the structures bond pads are attached in order to allow probing. Because there is a finite voltage drop from the test structure to these bond pads, additional pads (Kelvin pads) are placed very close to the ends of the structure (see figure 15) to achieve the most accurate voltage measurements.

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Figure 16. SWEAT structures with topography: a) top view, b) cross section.

The photolithography process is stepper based so it is not feasible to place individual test chips on various locations of every production wafer. However, these structures are compact enough to be placed in the saw apart region of every die and for every device manufactured. This allows the SWEAT test to be used as a process monitor for all devices manufactured. It also allows great flexibility for a SWEAT sampling plan since all wafers would have the SWEAT structures.
4.3 Test Parameters

The first step of the SWEAT procedure involves accurately determining the parameters of equation (29). After these are derived then the test setup and procedure will be explained.

During the SWEAT test it will be important to accurately determine the line temperature at all times. In order to do this, the relationship between resistance and temperature must be understood. Prior to implementing the SWEAT test, the metal test structure must be characterized in the following manner. A heated wafer chuck with an accurate temperature controller is used to set the wafer at different temperatures. After the wafer reaches temperature equilibrium, a small current (no joule heating) is forced through a test structure and the resulting voltage across it is measured. An HP4145 semiconductor parametric analyzer was used to measure line resistance as the wafer was heated to various temperatures (see figure 17). A thermocouple was pressed directly on top of the wafer to more accurately record the temperature. The maximum temperature used was 300°C to avoid metal annealing.

Analyzing the measured resistances yields a temperature versus resistance graph as shown in figure 18. This figure provides an average across several baseline structures. The temperature versus resistance curve must be determined for each different structure. Included in this graph are results for the metal 2 SWEAT structure, the same structure with topography, the control structure and a National Bureau of Standards electromigration test structure. In each case the lines were linear with a correlation coefficient of greater than 0.99. By measuring wafers from several lots, it has been found that the slope of this curve remains almost constant for a given process but small (10 %) variations in actual line resistance are not uncommon. Because the change in slope from lot to lot is small, it is proposed that this parameter need not
be measured often and therefore can be considered as constant for the SWEAT test. Since the line resistance will be measured for every structure tested, variations in line resistance will be accounted for using the SWEAT method developed here.

The slope of this temperature versus resistance line is $\beta R_o$, where $\beta$ is the thermal coefficient of resistance. During the test the temperature of the line can then be calculated by measuring the resistance change and using the equation

$$\Delta T = T_o + \frac{\Delta R}{\beta R_o} \quad (30)$$

Figure 17. Resistance measurements using the HP4145.
For the SWEAT test, the important measurement is the narrow portion of the test line. Under a current stress this portion can rise to a higher temperature than the adjacent heat sinks. The change in resistance has contributions from both the narrow portion and the heat sinks. The control features can be used to express this relationship as

\[ \Delta R = \beta R_{\text{control}} \Delta T_{\text{control}} + \beta R_{\text{narrow}} \Delta T_{\text{narrow}} = \beta R_0 \Delta T \] (31)

Here \( \Delta T_{\text{control}} \) is the average temperature of the heat sink. In reality there is a temperature gradient in the region where the heat sink tapers to meet the narrow strip but for simplicity, we do not lose much accuracy when we say that there are two constant temperatures, \( T_{\text{control}} \) and \( T_{\text{narrow}} \). During a current stress, the difference in these two temperatures will be proportional to the power density through each section. This is then proportional to the line resistance \( \left( \frac{I^2}{R} \right) \).
which is proportional to the number of squares as follows

\[
\Delta T_{\text{narrow}} = \frac{N_{\text{narrow}}}{N_{\text{control}}} \Delta T_{\text{control}} = \frac{R_{\text{narrow}}}{R_{\text{control}}} \Delta T_{\text{control}}
\]

(32)

where \(N_{\text{narrow}}\) is the number of squares in the narrow line, \(R_{\text{narrow}}\) is the resistance of the narrow line, etc. Substituting \(N\) for narrow and \(C\) for control, equation 30 can then be rewritten for the narrow line as

\[
\Delta T_N = \frac{\Delta R}{N_C/N_N + \beta R_o}\n\]

(33)

giving

\[
T_N = T_o + \frac{R - R_o}{N_C/N_N + \beta R_o - \beta R_o C} = \frac{\Delta R}{\beta R_o}\n\]

(34)

The number of squares ratio has been calculated in Appendix 1 as \(N_C/N_N = 0.55\). By actual measurements the ratio of resistances was found to be 0.52. The latter will be used in the software.

The current density factor, \(n\), is most effectively determined using a series of constant current tests on several samples of devices as explained previously. For the same metal composition and method of application, the variation in \(n\) from lot to lot will be small. This means that the value of \(n\) for a process need not be determined often. To determine \(n\) for the metal test structures used in this experiment several samples with a size of eighty devices were stressed at a constant current until failure. Each group of eighty was stressed at different current densities so that a plot similar to figure 6 could be drawn to determine \(n\). All tests were
For the SWEAT test, the important measurement is the narrow portion of the test line. Under a current stress this portion can rise to a higher temperature than the adjacent heat sinks. The change in resistance has contributions from both the narrow portion and the heat sinks. The control features can be used to express this relationship as

\[ \Delta R = \beta R_{\text{control}} \Delta T_{\text{control}} + \beta R_{\text{narrow}} \Delta T_{\text{narrow}} = \beta R_{\text{n}} \Delta T \]  

(31)

Here \( \Delta T_{\text{control}} \) is the average temperature of the heat sink. In reality there is a temperature gradient in the region where the heat sink tapers to meet the narrow strip but for simplicity, we do not lose much accuracy when we say that there are two constant temperatures, \( T_{\text{control}} \) and \( T_{\text{narrow}} \). During a current stress, the difference in these two temperatures will be proportional to the power density through each section. This is then proportional to the line resistance \( \left( \frac{I^2}{R} \right) \)
which is proportional to the number of squares as follows

\[
\Delta T_{\text{narrow}} = \frac{N_{\text{narrow}}}{N_{\text{control}}} \Delta T_{\text{control}} = \frac{R_{\text{narrow}}}{R_{\text{control}}} \Delta T_{\text{control}} \quad (32)
\]

where \(N_{\text{narrow}}\) is the number of squares in the narrow line, \(R_{\text{narrow}}\) is the resistance of the narrow line, etc. Substituting \(N\) for narrow and \(C\) for control, equation 30 can then be rewritten for the narrow line as

\[
\Delta T_N = \frac{\Delta R}{\left( \beta R_C N_C + \beta R_N \right)} \quad (33)
\]

giving

\[
T_N = T_0 + \frac{R - R_0}{\left( \beta R_C N_C + \beta R_N - \beta R_C \right)} = T_0 + \frac{\Delta R}{\beta R_0} \quad (34)
\]

The number of squares ratio has been calculated in Appendix 1 as \(\frac{N_C}{N_N} = 0.55\). By actual measurements the ratio of resistances was found to be 0.52. The latter will be used in the software.

The current density factor, \(n\), is most effectively determined using a series of constant current tests on several samples of devices as explained previously. For the same metal composition and method of application, the variation in \(n\) from lot to lot will be small. This means that the value of \(n\) for a process need not be determined often. To determine \(n\) for the metal test structures used in this experiment several samples with a size of eighty devices were stressed at a constant current until failure. Each group of eighty was stressed at different current densities so that a plot similar to figure 6 could be drawn to determine \(n\). All tests were
conducted at the same ambient temperature of 260°C. For higher current densities, the effect of joule heating on the MTF should be accounted for. This is done by determining the amount of temperature rise for the line at each current density (using resistance thermography) and normalizing all results to one temperature and activation energy. For example, if \( T = 533K \) but it is determined that at one current density, \( J \), there is additional metal line heating of \( \Delta T = 15K \) then the measured mean time to fail would be for a line temperature of \( T + \Delta T \). The measured mean time to fail, \( MTF_m \), must then be normalized to \( T \).

\[
MTF = MTF_m \exp \left( \frac{E_a \Delta T}{kT(1+\Delta T)} \right)
\]  

These experiments revealed that using \( n=2 \) will be accurate over a large range of current densities.

The activation energy can be found using a series of constant current tests at various temperatures. Again, several samples with a size of 80 devices was stressed at a constant current. Each sample was done at a different temperature and the time to fail was recorded. The mean time to fail was then plotted versus temperature as shown in figure 7. From these results it was determined that using an activation energy of 0.7 will be accurate over the typical SWEAT test temperatures.

The SWEAT software thus uses \( n=2 \) and \( E_a=0.7 \) but these values can be updated as needed by the user. All other parameters needed for the SWEAT test are found automatically by the program. If \( n \) and \( E_a \) are assumed as above then only one other parameter, \( \beta R_o \), is needed to perform the SWEAT test on any structure. For the test developed in this paper, the ESF and the SWEAT constant will be determined by the test system.
4.4 Test Setup

The entire test setup is controlled by an HP9836 microcomputer. An automatic probe station and a programmable power supply and current meter are controlled with this computer. An additional AT&T PC6300 is attached to the bus so that various PC software packages can be used to analyze output data. The system block diagram is presented in figure 19.

Figure 19. SWEAT test system block diagram.
4.5 Test Procedure

When the program is run, the initial screen presents several options which are selected by using the softkeys. If running the test for the first time, the structure must be characterized by selecting the “CHARACTERIZE” softkey. It is important that this is done using a wafer (or wafers) that you believe to be baseline or typical of your process. Characterizing this wafer will result in parameters needed for SWEAT testing of subsequent wafers.

The first phase of characterizing is determining the relationship of power versus metal line temperature. In order to maintain a constant ESF during SWEAT, the line temperature must be known at all times. This is done by applying a voltage pulse, measuring the resulting current, and calculating the power, $IV$. The temperature is then found from the power vs. temperature curve. The slope of this curve is $Q$, the power coefficient of temperature. The user will be prompted to enter $\beta R_0$ for the device. If it is unknown, then the default will be the value used by the last user. In the default case the program will ask which structure is being tested so the correct value is used. The value for $\beta R_0$ will then be computed using equation (34). To find $Q$ first the resistance of the line with no joule heating, $R_0$, is found. Knowing $R_0$ the program will effectively shift the line of figure 18 to correspond to the structure under test. Then the voltage across the line is increased in small increments and the line temperature is calculated using equation (30). Using $\beta R_0$ and equation (34), $Q$ for the narrow line is determined. Figure 20 is a graph of these lines.

The program then uses a least mean squares fit to calculate the slope. If the correlation coefficient is much less than 1 then the line resulting from the data is not very straight. In this case the program will automatically alert the user, disregard that test, and move to another site. The test will be repeated at various sites across the wafer and a summary similar to figure 21 will be generated.
Figure 20. Power vs. temperature curves.

************** WAFER SUMMARY for Q **************

<table>
<thead>
<tr>
<th>SITE#</th>
<th>Q (K/Watt)</th>
<th>CORRELATION COEFFICIENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>455.08</td>
<td>0.99995</td>
</tr>
<tr>
<td>2</td>
<td>432.84</td>
<td>0.99985</td>
</tr>
<tr>
<td>3</td>
<td>448.31</td>
<td>0.99991</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>451.08</td>
<td>0.99995</td>
</tr>
</tbody>
</table>

Average Q for this wafer is 442.426446629

****************************

Figure 21. Example wafer summary for Q.
The next action is determining the target time to fail. In practice the SWEAT test can be characterized to run as fast as you like - even into the seconds range. If you characterized your baseline devices to have a mean time to fail of say five seconds then, using the same parameters, any chips failing before this target time are inferior and those surviving longer are more robust. This high test speed is one of the most appealing aspects of this system, especially since traditional electromigration tests typically can take weeks to complete.

There is, however, one problem with running the test at blazing speeds of a few seconds. When you heat the metal line to temperatures higher than about 350°C lattice diffusion becomes a very significant factor of metal migration. Metal ion movement is no longer in a regime governed mainly by grain boundary diffusion. With lattice diffusion the activation energy is much higher (over 1.2eV). More importantly, the SWEAT test is used to accelerate migration that will be seen in normal use of the circuit and lattice diffusion would not apply during normal use. It is therefore, important that the SWEAT test not exceed about 350°C.

The system will determine the maximum possible SWEAT test speed (the minimum ESF). This is done by first finding $R_o$ and $Q$, then setting the temperature of the narrow line equal to $T_{Nmax}$ of 350°C in the equation

$$\left(T_{Nmax} - T_o\right)\beta R_o' + R_o = \frac{V}{I}$$  \hspace{1cm} (36)$$

The test will stress the line to this temperature and the line temperature will be constantly monitored using the equation

$$\frac{(T_{Nmax} - T_o)}{Q} = VI$$  \hspace{1cm} (37)$$
Combining equations 36 and 37 the voltage needed to achieve this maximum line temperature can be calculated as

\[ V = \left\{ \frac{(T_{N_{max}} - T_o)}{Q} \left( (T_{N_{max}} - T_o) \beta R_o' + R_o \right) \right\}^{1/2} \quad (38) \]

This equation is used to establish the starting voltage for the test. While the structure is being stressed, changes can occur in its resistance. Because of this it is important to recalculate the narrow metal line temperature as the resistance changes and adjust the stress voltage so that the temperature remains constant through the entire test. Under software control the system will fine adjust the stress voltage at least every 50ms. After stressing for some period of time at this maximum line temperature, the line will open due to electromigration. The test is then stopped and the time is recorded. Several sites across the wafer will then be tested in the same way and the average time will be calculated. At each site the average current and voltage is also recorded and printed. For accuracy voltage and current readings during the last few moments of the test are pruned from this average because at this time the line is undergoing migration which can lead to large variations in resistance. With knowledge of this average current, the SWEAT constant, \( S \cdot A \), is then determined at each site by solving the equation

\[ T_{fail} = S \cdot A \left( \frac{I_{av}}{w_i} \right)^{-2} \exp \left\{ \frac{E_a}{k T_{N_{max}}} \right\} \quad (39) \]

A wafer summary similar to figure 22 is produced. From this summary the SWEAT constant and the target time to failure is extracted. This target time to failure will be the maximum speed that the SWEAT test can be run for that structure. Using this maximum speed, SWEAT can be used to compare metal from one device to the baseline material. Running the test any faster will result in inaccurate results because bulk diffusion will dominate. In order to extrapolate actual metal lifetimes using the SWEAT test it should be run at a much slower
speed. This will reduce effects of temperature gradients and current density dependence variations. To characterize the structure to run at a slower speed one would lower the value of $T_{N_{max}}$ (less than 350°C) while running the program. The system would then calculate a longer ESF and a new A·S constant.

<table>
<thead>
<tr>
<th>Site #</th>
<th>Resistance Ohm</th>
<th>Time to fail (s)</th>
<th>Avg current (mA)</th>
<th>Avg voltage (V)</th>
<th>SWEAT constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5.08 Ohm</td>
<td>20.370</td>
<td>251.30E+00 mA</td>
<td>2.675 V</td>
<td>9.373E+17</td>
</tr>
<tr>
<td>2</td>
<td>4.93 Ohm</td>
<td>28.330</td>
<td>267.23E+00 mA</td>
<td>2.812 V</td>
<td>1.439E+18</td>
</tr>
<tr>
<td>3</td>
<td>4.93 Ohm</td>
<td>25.890</td>
<td>267.60E+00 mA</td>
<td>2.741 V</td>
<td>1.319E+18</td>
</tr>
<tr>
<td>15</td>
<td>4.81 Ohm</td>
<td>18.480</td>
<td>273.23E+00 mA</td>
<td>2.795 V</td>
<td>9.816E+17</td>
</tr>
</tbody>
</table>

*************** WAFTER SUMMARY ***************
The average Q is 458.192614961
Avg Voltage= 2.801
Avg current=270.45E+00 mA
Average $T_{fail}$= 23.012 s
With a standard deviation of 4.46 s
New SWEAT constant is 1.198E+18
Use this $T_{fail}$ and SA for future SWEAT Testing of this structure

Figure 22. Example output of wafer characterization.

After characterizing the baseline wafer the SWEAT test can then be used to monitor all other wafers having the same structure and using the same technology. Figure 23 is a flow chart that summarizes the SWEAT test. After the wafer is set up on the prober, the entire test is performed under software control according to this flow chart. Important steps of this flow chart will now be described in more detail.
To increase the accuracy of the test it is very important to achieve the following three goals:

1. The target ESF must be reached as quickly as possible.

2. During the initial ramp-up of the power pulse and throughout the test, it is important not to exceed the target ESF by applying a power pulse that produces a stress that will make the line fail earlier than the target time.

3. Because the properties of the line may change during the time that the line is stressed, it is crucial to constantly update the ESF by changing the power pulse accordingly.
Point #1 has been successfully achieved by choosing a starting voltage that initially stresses the line to very near the target ESF. This is done by using equation 38 as used in the wafer characterization section. To assure that the stress does not exceed the target stress during this initial ramp-up (point #2), $T_{N_{\text{max}}}$ is set at about $25^\circ \text{C}$ below the $T_{N_{\text{max}}}$ used in characterization ($325^\circ \text{C}$ rather than $350^\circ \text{C}$).

Before calculating the starting voltage the value of $Q$ and $R_0$ must be found for the structure. The original procedure for SWEAT was to find an average value of $Q$ and $R_0$ for a process and use these values for testing all wafers. The author proposes that because resistances and the power versus temperature relationships differ from structure to structure it is important to find a new value for $Q$ and $R_0$ for each structure tested. The system will automatically find these values at the beginning of each test at an expense of about one second of test time.

After calculating the starting voltage it is then applied across the structure. The resulting current and actual voltage is measured and the magnitude of the power pulse is calculated. From this the narrow line temperature is found using

$$T_N = PQ + T_0$$  \hspace{1cm} (40)

Using the ESF equation

$$\text{ESF} = S \cdot A \left( \frac{1}{wt} \right)^{-2} \exp \left\{ \frac{Ea}{kT_N} \right\}$$  \hspace{1cm} (41)

the ESF is calculated and compared to the target ESF. If the calculated ESF is greater than the target (i.e. it would take longer to fail at this ESF) then the voltage is increased. To converge to the correct ESF as quickly as possible without exceeding it something must be known about the differential change in calculated time to fail per volt around that line voltage. This is the slope of figure 24 at the measured line voltage. Based on knowledge of this, the program determines how much change in voltage will be needed to converge to the target ESF.
Figure 24 Calculated time to fail versus voltage across structure.

Under the computer control and using the techniques mentioned above, the tester has been shown to converge to the target ESF very rapidly. Further, the voltage is fine adjusted about every 50ms to assure that the stress remains constant through the duration of the test. The rate of this adjustment is limited by the settling time of the power supply used. To demonstrate this, various parameters were plotted versus test time and are presented in figures 25 to 27. Figure 25 is a test that attempts to provide a stress that will make the line fail in 23.01 seconds. Here we see that the target ESF (23.01sec) is reached in less than 100ms and it is constantly maintained to $\pm 0.05$ sec over the entire test time. The graph then shows that the line opens from electromigration in 24.45 seconds (slightly better than the average of 23.01s). Figure 26 shows the line temperature which raises to almost 350°C during the test and falls back to room temperature as the line opens. Figure 27 is the current density which drops to 0 when the line opens.
Figure 25. Calculated time to fail versus the test time.

Figure 26. Temperature of the narrow line versus the test time.
After each voltage adjustment, the test checks for the line being open. If it is open then the fail time is recorded. The test continues until every structure on the wafer is tested after which point a wafer summary is printed, stored on disk and, if requested, sent to the PC for further analysis. The summary will give the average $T_{fail}$ for the wafer, the standard deviation of $T_{fails}$ and the time taken to test the entire wafer. Another output is a wafer map of fail times as shown in figure 28. Engineers may find this map may be useful in determining if metal reliability problems are related to some zone of a wafer such as the outsides or center. This may give a clue as to what are the sources of the metal reliability problems.
For optimum speed in a production environment, SWEAT can be run as a pass/fail test. In this mode the line would be stressed for t seconds where t is the target time to fail. If the line fails before this then the fail time is recorded as usual. If the structure lasts for t seconds then the test would stop and the metal would be assumed to be at least as good as the baseline. Doing this will be the fastest method to test for electromigration in a production environment but much information is lost. For example, the spread of fail times will not be found and if devices are better than the baseline there is no way of knowing how much better.

4.6 Other Software Features

In addition to those already mentioned, the SWEAT software also has many other features. One worth noting is the ability to send data files or test outputs directly to the PC for
analysis. A wafer map such as figure 28 or a list of fail times for a wafer are two examples. One option will send the summary of fail times for as many wafers as requested and merge these into one data file on the PC. Then the data could be analyzed using spreadsheet or statistical analysis programs. From the PC, data can be uploaded to mainframes for further number crunching and mass storage. This would be useful in a production environment where large quantities of data are to be collected.

If it is determined that the variation in time to fail is very tight across a wafer then it would be more efficient to only test every other site or only a sample of sites on the wafer. One option available is to run the test skipping every other site to cut wafer test time in half. This could easily be taken further by modifying a data map in the program which tells the prober which sites to probe.

The software now includes parameters needed to test metal 1 and metal 2 SWEAT structures for the 1.25µm CMOS process. These options are available while setting up the wafer. The test can be used for any technology in the future by inputing the correct width and thickness of the test structure when the program requests it.

Before any test on a chip (including finding Q, finding R_o, finding S·A or doing the SWEAT test), a contact test is performed to determine if the probes are making proper contact. If it fails this contact test then the chip is ignored and the test moves to the next site. This test also determines if the SWEAT structure has already been opened by a previous test. If no tests make contact on the wafer then the user is requested to check the problem and start the wafer from the beginning.
5. RESULTS OF SWEAT TESTING

Through experimentation, this SWEAT test has been shown to be an accurate reliability screen for electromigration. Wafers from several lots have been tested and compared to the baseline. Variations in time to fail within one lot tended to be small because metal composition and thickness were well controlled. This tight distribution of failure times is one indication that the test is well controlled and it is giving equal stresses to each device. From lot to lot differences in average fail time can sometimes be seen.

A notched box-and-whisker plot is one way to effectively present a great amount of information on a large amount of data in one compact chart. Figure 29 shows results of the SWEAT test on several wafers from the same processing lot. The central box covers the middle 50% of data values bounded by the upper and lower quartiles. The whiskers extend beyond the box to cover all other data points. There is a line in the middle of the box that represents the median value. Extreme data points are plotted separately outside the whiskers. The notches correspond to the width of a confidence interval around the median. In this experiment the baseline metal was characterized to determine the SWEAT constant and a target time to fail of 16.3 seconds was used. If a line is drawn at this target time then if the line is below the notches or intersects them there is at least a 95% confidence that the wafer results meet the target time to fail. A box falling entirely below the 16.3 seconds indicates that the wafer may have a metal reliability problem. All wafers in this lot passed the SWEAT test as can be seen.

Several wafers from another lot were tested to the same criteria as figure 29 and the results for this lot are shown in figure 30. In this lot it is shown that all wafers substantially exceeded the target time of 16.3 seconds. It can thus be predicted that the metal reliability for this lot is much better than the baseline. Reasons for this could be thicker metal or more
uniform metal grain structure.

SWEAT Test for lot 20579
Target Time to Fail is 16.3 sec

Figure 29. Metal 2 SWEAT results for several wafers from lot 20579.
SWEAT Test for lot 20592
Target Time to Fail is 16.3 sec

Using the SWEAT structure with topography as shown in figure 16, the effects of step coverage on metal reliability can be studied. To demonstrate this, a group of several wafers were tested. All chip sites had structures with and structures without topography. The structure without topography was characterized to determine the SWEAT constant and a target time to fail of 23.01 seconds. The wafers were tested for both structures using the same parameters and the results are shown in figure 31.
Effects of Topography on SWEAT Test

Target Time to Fail = 23.01 sec

Figure 31. Testing the SWEAT structures with and without metal topography.

The notch on the graph of structures without topography falls on the 23.01 second line indicating that these chips are acceptable. The box of the structures with topography, however, falls slightly below the target time. In theory the mean lifetimes ($T_{50}$'s) of the two structures...
could be extrapolated from the measured values to actual use conditions using the equation

\[ T_{50use} = T_{50meas} \left( \frac{I_{meas}}{I_{use}} \right)^{-n} \exp \left\{ \frac{E_a}{k} \left( \frac{1}{T_{use}} - \frac{1}{T_{meas}} \right) \right\} \] (42)

The temperature of the line during the SWEAT test is calibrated to be very close to 350°C (T\(_{meas}\)=623K) as explained above. The program was modified to find the average stressing current during the test. For the structure without topography this revealed I\(_{meas}\)~270.4mA and for the structure with topography I\(_{meas}\)~258.8mA. If an I\(_{use}\) of 10mA (dc - not pulsed) and a T\(_{use}\) of 343K is assumed then equation 42 predicts an actual use lifetime of 22.3 years for the line without topography and a degradation to 16 years (28% decrease in lifetime) with topography. For I\(_{use}\) of 2mA these numbers become 557 years and 400 years. The accuracy of these extrapolations are effected by current density dependance variations (n>2) at high current densities.

An additional experiment was performed to show how the SWEAT test can uncover metal width problems. One aluminum problem that has been reported by several wafer manufacturers is the so called "rat bites" as illustrated in figure 32. This is an example of phenomena that will go undetected by any functional or parametric test but can present a serious reliability problem after extended system use.

Figure 32. Metal rat bites - bad news for semiconductor manufacturers.
A batch of wafers were processed to intentionally have these rat bites for the purpose of this experiment. They were then SWEAT tested with a target time to fail of 23.01 seconds. The SWEAT ESF equation assumes that all metal widths and thickness (wt) are constant. Therefore, structures that deviate from the expected wt will fail accordingly at SWEAT testing. Figure 33 confirms these expected results.

SWEAT Testing of Wafers with Ratbites
Target Time to Fail=23.01sec

Figure 33. Rat bite problem successfully flagged by the SWEAT test.
This paper has discussed a reliability problem in integrated circuits - electromigration in aluminum interconnects. It was shown that this is a problem that is becoming increasingly more important to the semiconductor industry as geometries are shrinking. A literature search has revealed that although the problem has been studied for a long time there are still many things that are not explained or well understood. What we understand today about this topic as well as the dominantly accepted theories are presented in this paper. There have been many attempts to develop equations and mathematical models for electromigration and the most widely used ones were presented and explained.

A very common equation that predicts lifetime of metal subject to a current stress is an Arrhenius relation often referred to as the Black equation. It is described in detail including how it was derived and how to apply it. Many electromigration experiments have used some form of this equation to explain results and relate them to the real world. It is an empirically derived relationship and some of the parameters are not based on scientific knowledge but on experimental data. These parameters are generally assumed to be constants and factors which may effect them must be ignored to make the model useful. No matter how refined one is in defining the parameters there will always be some amount of uncertainty in using the model to estimate metal lifetimes. Nevertheless, using the Black equation has enabled many researchers to deduct valuable information which has resulted in ways to make integrated circuits more reliable.

Many of the most important research efforts that have been taken to approach this problem are also discussed. Several techniques have been discovered that have been shown to increase resistance to electromigration. Some of these are alloying, method of metal application,
and using different types of passivation. Researchers have also reported on the relationship of electromigration to factors such as changing metal grain size, pulsing currents, and varying interconnect widths. Findings of many of these studies are summarized in this paper.

In order to estimate probable lifetimes of metal or to determine the effect of different processing variations on metal lifetimes, it is important that an accurate testing strategy be used. After examining the literature it was found that there are now several different testing methods used throughout the industry. There seems to be much disagreement as to what is the best way to test for electromigration. This paper has reported on several of the more prominent types of tests along with advantages and disadvantages. There have been several achievements by many authors in developing a better type of test but to date an economical and effective method to test for electromigration resistivity has neither been proven nor universally accepted.

One type of wafer level electromigration test appears to improve upon many of the shortcomings of other methods. It is the SWEAT test (for Standard Wafer-level Electromigration Accelerated Test). By using some of the commonly accepted theories as a foundation, a variation of SWEAT has been developed by the author. Other types of electromigration tests apply the same current to different devices and compare the results. SWEAT accounts for the fact that different devices will react differently to the same current. It does this by giving each device the same stress factor. The theory for developing the stress factor is explained in this work. The stress factor is chosen so that when baseline product is subject to this stress it will fail in a predetermined amount of time. If the device under test survives for this amount of time then it is at least as good as baseline product. Thus, SWEAT is used to compare metal quality from device to device.
To determine if the test is feasible, a computer controlled test system has been built and associated software has been written as reported in this paper. This system is first used to characterize the metal before running the actual SWEAT test. By using a joule-heated constant temperature test, the system automatically finds the correct target stress factor and then calculates some of the parameters needed to run the SWEAT test. When SWEAT was first introduced the procedure was to arbitrarily choose any target time to fail and then find the SWEAT constant by trial and error. This system automatically finds both the fastest time to fail and the constant. The software has been written with several desirable features including the following:

1. The test system developed here has been shown to reach the target stress factor very fast (<100ms) and to maintain this stress very accurately through the duration of the test.

2. By linking the system to a personal computer the possibilities for data analysis become great. Outputs using several different PC software tools are presented in this paper.

3. The system can easily be adapted to test any level of metal in any technology.

4. Printouts from the SWEAT system are easy to interpret.

5. The system has been developed so that it is easy to run - even for non-engineering personnel.

6. Statistical analysis techniques are used to improve the accuracy of the test.

7. Based on theory, the SWEAT test is accelerated to the fastest possible limit that will still give accurate results.
To demonstrate the system, test structures were designed and fabricated using a 1.25µm two level metal CMOS process. Compared to conventional testing techniques which usually take weeks, the test is extremely fast (tens of seconds per structure tested) and effective. Experiments have been performed to demonstrate some of the abilities of the test. One experiment compared metal lines with large steps to planar structures to determine the reduction in expected lifetime with topography. Another test demonstrated that SWEAT can be used to screen for problems with inferior line width.

Using SWEAT in a research environment could enable us to greatly improve our understanding of how various factors and processing changes affect electromigration resistivity. This is because results from experiments will be known much faster than when conventional testing techniques are used.

In a production environment it is very important to continuously monitor metal reliability. Circuit testing techniques used today do not have the ability to do this. By implementing SWEAT as a process line monitor, each wafer lot can be tested and information on metal quality can be determined and quickly fed back to process engineers who can further investigate the sources. Typical manufacturing tests include parametric tests (CV and IV), followed by chip functional testing, and then a retest after burn in or other reliability screens. With this testing scheme in place there is still a potential that devices with long term metal reliability problems will pass everything and get approval to be shipped to the customer. Performing SWEAT at the time of parametric testing will help to find these unreliable devices. The importance of incorporating a test of this type into the manufacturing loop will continue to become more of a necessity as linesizes are reduced and densities are increased.
Although this SWEAT system has demonstrated that it can be very useful, it is still in its early stages of development and there are many opportunities for improvement and refinement. The system as it exists today needs to be adapted if it is to be placed in a production environment. For example, it could be linked to a large computer for mass data storage and automated analysis. One way to improve the test might be to use a current density dependance factor that is a function of the current density itself as explained in this study. The activation energy constant could also be used as a function of current density as some authors suggest. One weakness of the system is that the relationship between actual SWEAT results and the expected metal lifetime is still not well understood. The ideal SWEAT system would stress a line for tens of seconds and then automatically extrapolate the results to expected hours (years) of in use operation. This type of system is feasible but much must still be learned about the nature of electromigration to make such an extrapolation accurate.

Our understanding of electromigration comes primarily from results of experiments that were done to verify new theories and new processes. Using SWEAT in electromigration experiments has the potential to provide testing results in periods of time that are orders of magnitude shorter. Because of this we can expect that new understandings of the electromigration problem can be achieved at a much faster rate.
REFERENCES


40. Jones and Smith, p. 4670.


46. Personal communication with Daniel P. Chesire.
APPENDIX A

Ratio of number of squares in SWEAT structure

\[ N_{\text{1 to 4}} = \frac{4L}{L + 4W_1} = 2.1639 = \text{effective number of squares for parts 1 to 4 combined} \]

\[ N_5 = 1 = \text{number of squares for part 5} \]

\[ N_C = 3.1639 = \text{number of squares for control section} \]

\[ N_N = \frac{10}{1.75} = 5.714 = \text{number of squares for narrow section} \]

\[ \frac{N_C}{N_N} = 0.554 \]
VITA

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