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K-band power amplifier design.

Gerard N. Chappell

K-BAND POWER AMPLIFIER DESIGN

by

Gerard N. Chappell Jr.

A Thesis

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January 31 1983
(date)

Professor in Charge

Chairman of Department

ACKNOWLEDGMENTS

I would like to acknowledge the inspiration and guidance received from Professor Marvin H. White through graduate studies and this thesis. I wish to express my gratitude to Dennis Poulin, Eric Ehlers, and the rest of the Hewlett-Packard Santa Rosa Technology Center Device Applications Group for their interest and technical assistance in completing this thesis.

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ABSTRACT

K-BAND POWER AMPLIFIER DESIGN

By

Gerard N. Chappell Jr., M.S.

Lehigh University, 1983

Professor Marvin H. White, Advisor

The purpose of this thesis is the design of an 18-26.5 GHz power amplifier capable of 8 dB of small-signal gain and a power out of 18 dBm with an input of 13 dBm. The circuit is realized in two stages on a sapphire substrate with coplanar waveguide transmission lines and FET transistors. Load-pull measurements are made on the FET's to determine the optimum load impedance under actual operating conditions. The circuit is then modeled with two small-signal (linear) simulation programs and a large-signal (non-linear) simulation program. The final circuit is realizable and optimized for maximum power out, as well as gain and flatness over the band. A substrate is then designed and realized, and the circuit assembled. The circuit is modified by laser trimming and reassembled to improve its performance. With the iterative design procedure studied in this thesis, a K-band power amplifier can be developed.

1. INTRODUCTION

1.1. Historical Review

During the past one and a half decades, the gallium-arsenide field-effect transistor has developed from the laboratory sample to one of the fastest three terminal devices. The first GaAs Schottky-barrier FET was introduced in 1967 by Hooper and Hower [1]. Higher technology allowed for smaller device fabrication, and in 1969 Drangeid et. al. reported on a 1 micron gate GaAs FET with a maximum oscillation frequency, f_{max}=30 GHz [2]. Baechtold et. al. followed in 1973 with a half-micron gate device with an estimated f_{max} of 80 GHz [3]. Just prior to that, Baechtold introduced the first X-band amplifier with GaAs FET's [4].

The past 10 years have seen many improvements in both FET processing and microwave amplifier design. GaAs FET amplifiers are beginning to replace TWT and Gunn doide amplifiers in the K-band electronic warfare market [5]. Also, demands for GaAs FET amplifiers operating at K-band or higher are increasing for satellite communications systems applications [6]. However, because of the design accuracy needed at such high frequencies, amplifiers are being designed as monolithic circuits, or at single frequencies rather than broadband. This paper presents a broadband, discrete component K-band amplifier design.

1.2. GaAs FET

Gallium-arsenide Schottky-barrier field-effect transistors are dominating silicon bipolar transistors at microwave frequencies due to the higher electron mobility and a higher saturation velocity of gallium arsenide vs. those of silicon. These properties result in better noise properties and a higher maximum oscillating frequency. Two other properties of GaAs FET's are favorable: the transconductance remains almost constant over the usable frequency range; and, the feedback capacitance is more than one order of magnitude smaller than in bipolars. These properties facilitate design of microwave amplifiers. With relatively simple matching networks, large bandwidths can be obtained [7].

The devices used in designing and realizing the K-band amplifier are TC-320's, Hewlett-Packard Tecnology Center inhouse GaAs Scottky-barrier FET's. The specifications of the TC-320, along with models used in the circuit design, are listed in Appendix II.

1.3. Design Procedure

The flowchart of Figure 1-1 details the design procedure used in developing the K-band amplifier. The circuit specifications are given in the thesis proposal (see Appendix I). Load-pull measurements are taken for both the single and paralleled FET's. This, along with the given substrate thickness and dielectric constant, makes up the design data. Several synthesis methods are used. A small-signal (linear) simulation program, OPNODE, is used

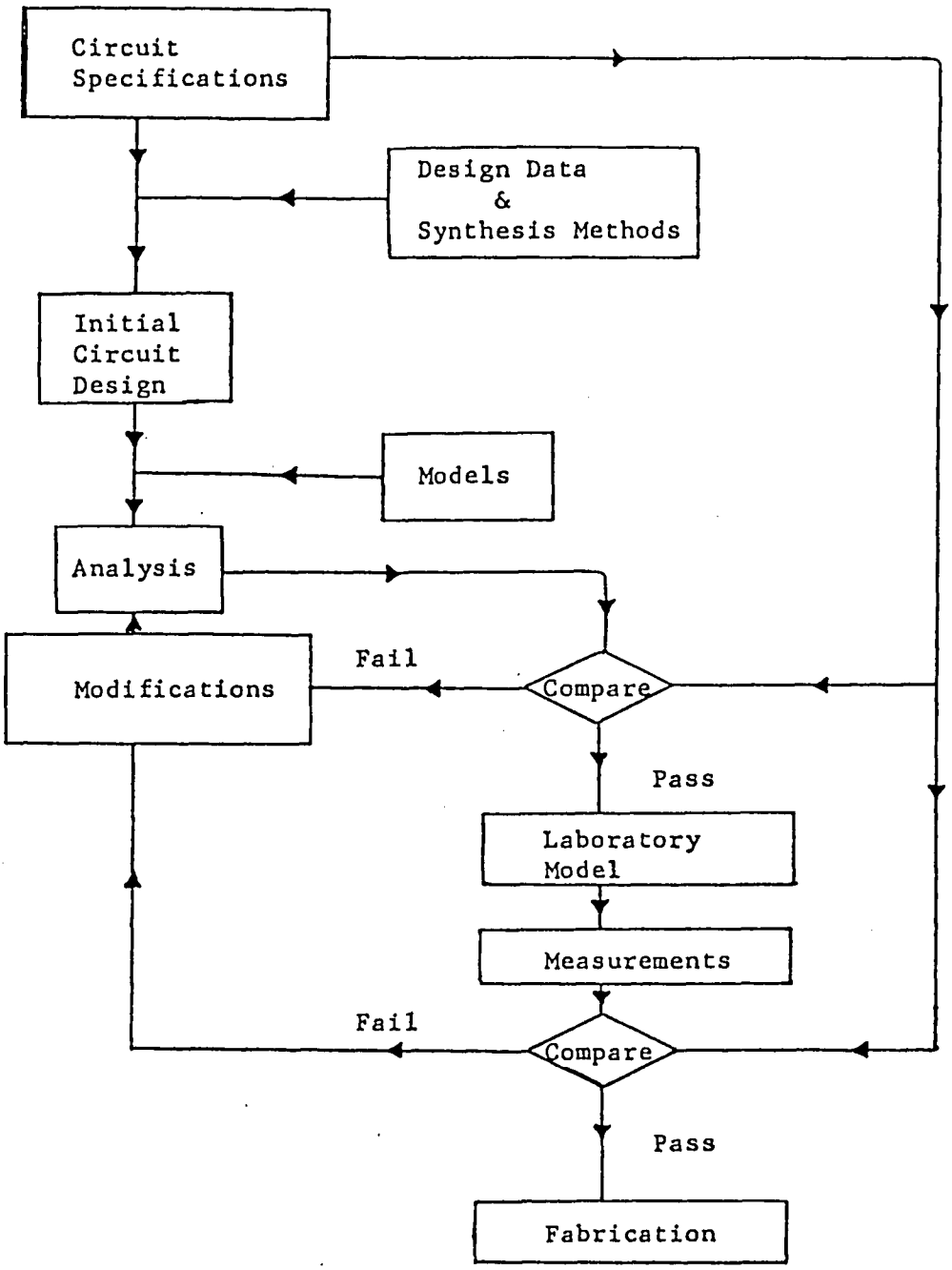

Figure 1-1: Design Procedure

to design the input, interstage, and output matching networks with the load-pull data and an FET model developed previously. This circuit is optimized with OPNODE to obtain gain and flatness over the band.

An AC analysis is performed on SPICE with the circuit developed along with a SPICE model of the FET developed previously to assure the OPNODE and SPICE models of the FET simulate the same behavior. A large-signal (transient) analysis is then performed with SPICE and the circuit is reoptimized to obtain good power out over the band. The circuit is examined to ensure realizability on a substrate.

The next step is the design of the actual substrate. This design is sent to the lab to be cut; and, upon completion, the circuit is assembled on the substrate and tested. Should this circuit meet design specifications immediately, the project is finished. However, this is rare for a first cut. The circuit that fails to meet specifications is analyzed, along with its model, to discover why its behavior deviates from the expected behavior. The substrate is redesigned and the circuit rebuilt and tested until specifications are met. This iterative design procedure should yield a K-band power amplifier.

2. CIRCUIT DESIGN

2.1. LOAD-PULL

2.1.1. What is it ?

Load-pull is a method of characterizing the large-signal behavior of devices or circuits. In dealing with the large-signal excitation of devices, the optimum load impedance is found to be a function of the output power. Thus, for high power devices, small-signal S-parameter matching methods are no longer useful. In load-pull characterization, the load impedance required is measured under actual operating conditions [8].

To measure a device with the load-pull method, an experimental setup described in Appendix III is assembled. A desired input power is applied to the device, and by adjusting the output tuner and observing the output power meter, a maximum power out point is found and plotted on the Smith chart. Keeping the input power constant (by use of the input tuner), and adjusting the output tuner, all the points 1 dB down from the maximum output power are found and plotted. This is repeated for -2 dB and -3 dB points. At each output power, the corresponding points are connected to form power contours as shown in Figure 2-2.

By repeating this procedure at several frequencies within the desired operating range, and superimposing the contours, a desired

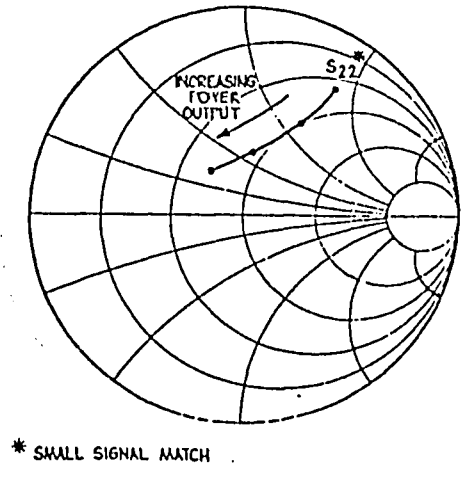

Figure 2-1: Optimum Load vs Output Power

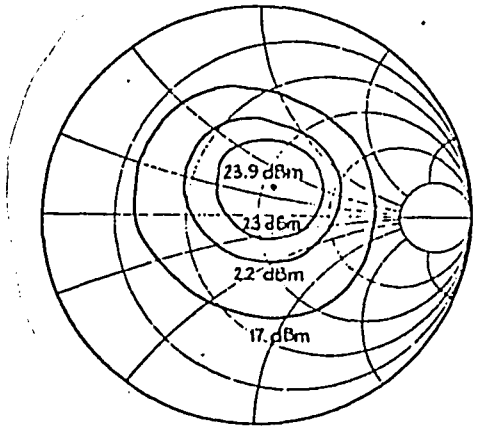

Figure 2-2: Constant Power Out Contours vs Output Load Impedance

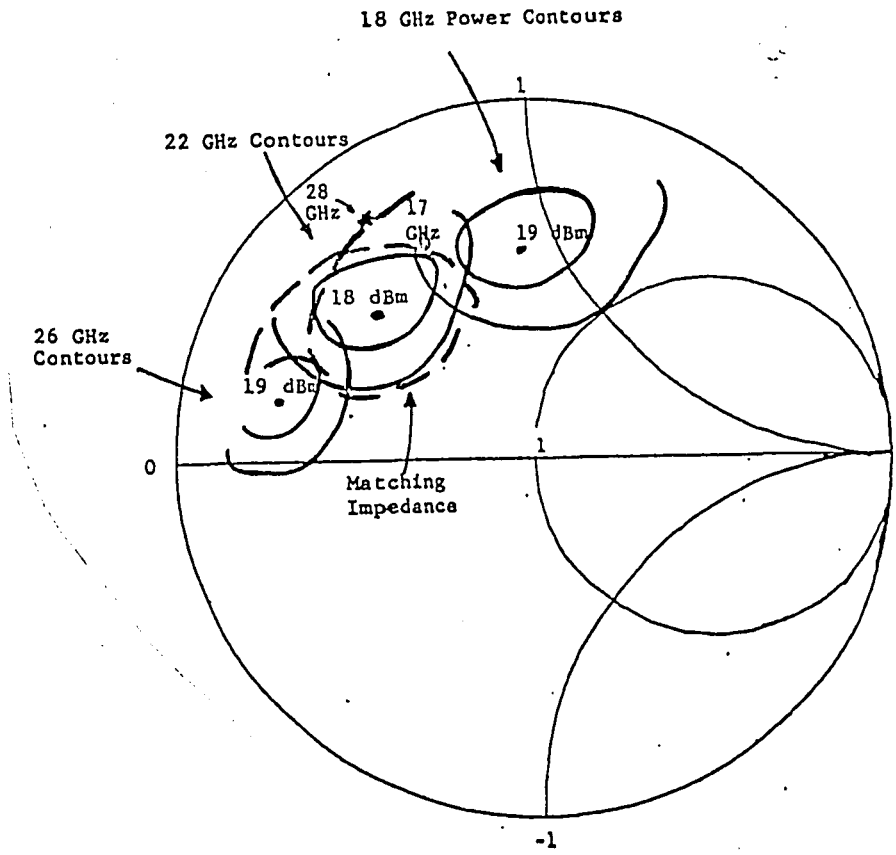

Figure 2-3: Superimposing Contours to Determine A Matching Impedance

matching impedance range can determined. The flatness of the ouput power over the band depends on the exactness of the impedance match (see Figure 2-3)

2.1.2. Device Measurements

Both the single FET's and the paralleled FET's are measured on the load-pull setup. The devices are mounted on 25 mil sapphire substrates as shown in Figure 2-4. The 22 pF MIS capacitors and FET's are epoxy die attached and the capacitors closest to the devices are located a quarter-wavelength from the devices at a midband frequency of 22 GHz. This bias ladder is designed to produce an RF open at the devices such that the ladder does not form an RF path for the signal.

The devices are mounted in an RF fixture for testing. This test fixture has been tested previosly previously with a 50 ohm thru-line mounted in it. It is found to have up to 10 dB return loss near 26.5 GHz. A time domain analysis shows the SMA barrel to be slightly inductive, while the transition from the barrel to the substrate is slightly capacitive; however, for the nature of the measurements, this seems to be acceptable and a 50 ohm transition is assumed.

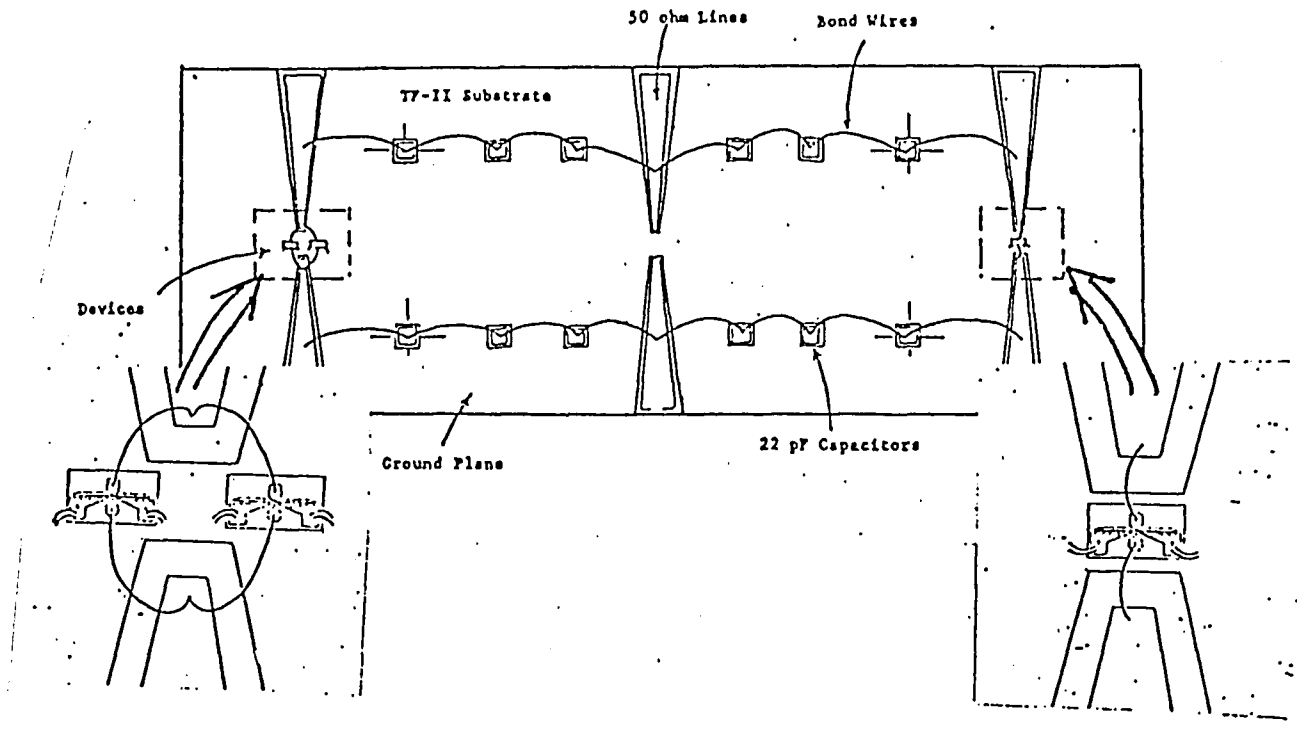

Figure 2-4: Load-Pull Test Substrate

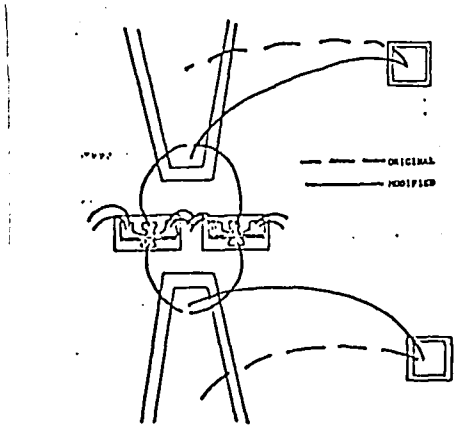

Figure 2-5: Bonding Change

2.1.3. Problems Encountered

In making load-pull measurements, several problems are encountered. The first problem is the DC bias oscillations, and the second is due to the frequency limits of the equipment.

2.1.3.1. DC Bias Oscillations

During the biasing of the parallel FET's, it became apparent that the devices were oscillating (RF power out with no power in). Using an HP Spectrum Analyzer, the oscillations were found to be at 4 GHz. Since the waveguide presents a virtual open below 10 GHz, it was assumed that the oscillations were due to the dc bias paths. Several quick methods were tried to terminate these oscillations, such as:

1. Since the bondwires from the capacitors to the gates and drains of the devices were not bonded directly to the devices, the impedance presented to the devices was not a true open, but a transformed impedance. Therefore, the bond wires were plucked and placed as close to the devices as possible (see Figure 2-5)

2. A 200 ohm chip resistor was placed after the first capacitor on the gate bias ladder to make the impedance following the first capacitor extremely lossy.

3. All of the bond wires were doubled to reduce the inductances.

None of these methods stopped the oscillations.

Finally, with a small-signal model of the FET, the S-parameters were determined for the parallel FET's. These parameters were used to find the input and output stability circles with the equations

shown [9].

For the input stability circle, the center is calculated by:

$$r_{is} = \frac{(S_{11} - D_s S_{22}^*)^*}{|S_{11}|^2 - |D_s|^2}$$

where

$$D_s = S_{11}S_{22} - S_{12}S_{21}$$

and the radius of the circle is

$$\rho = \frac{|S_{12}S_{21}|}{||S_{11}|^2 - |D_s|^2|}$$

For the output stability circle, the center is defined by:

$$r_{os} = \frac{(S_{22} - D_s S_{11}^*)^*}{|S_{22}|^2 - |D_s|^2}$$

and the radius is

$$\rho = \frac{|S_{12}S_{21}|}{||S_{22}|^2 - |D_s|^2|}$$

The impedances which fall within the circle may cause the device or circuit to be unstable.

The instability regions of the input (gate) and output (drain) are shown in Figure 2-7 for 2, 4, and 6 GHz. Since the device is unconditionally stable above 8 GHz, only the range 1-8 GHz was

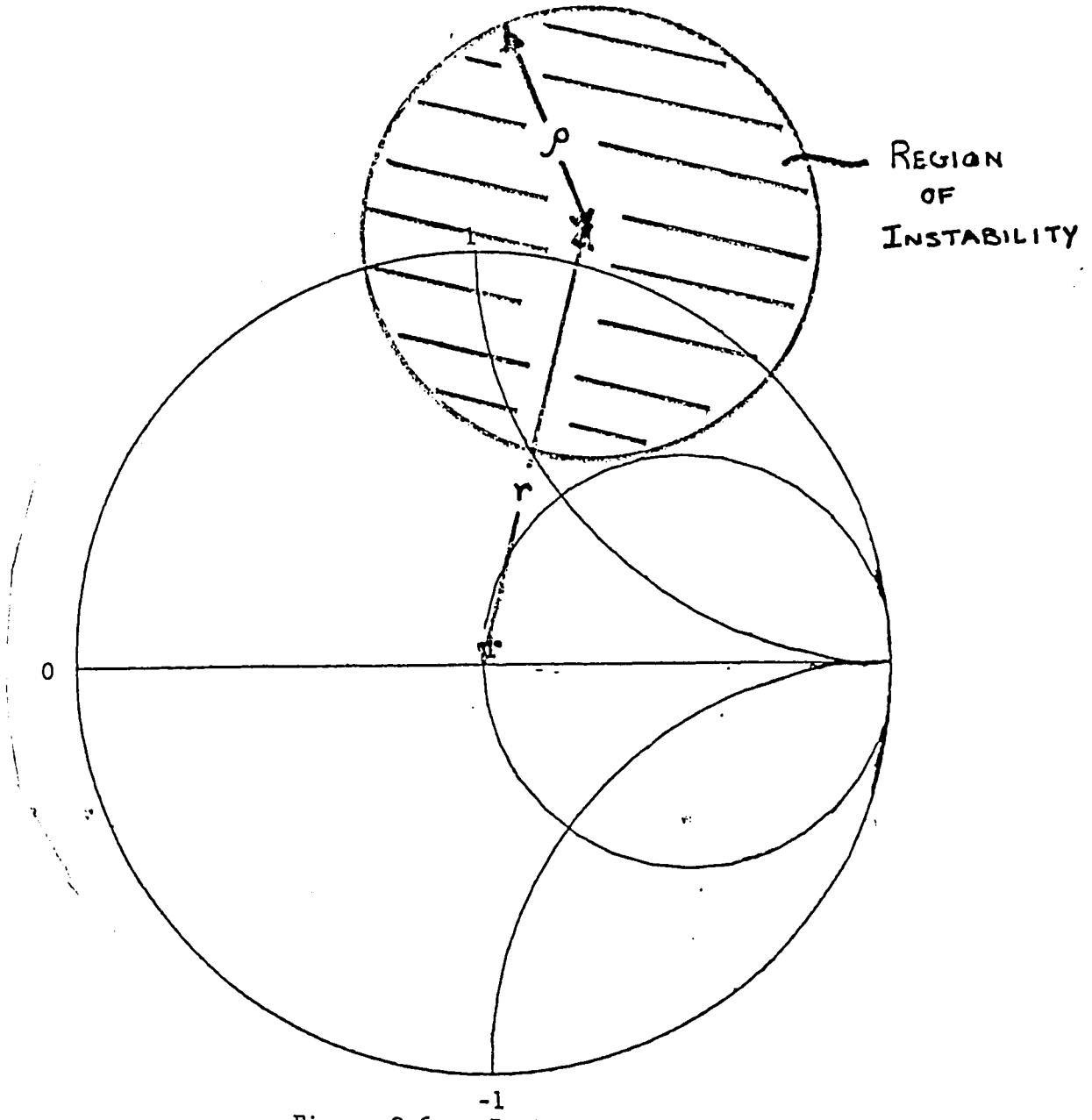

Figure 2-6: Instability Region

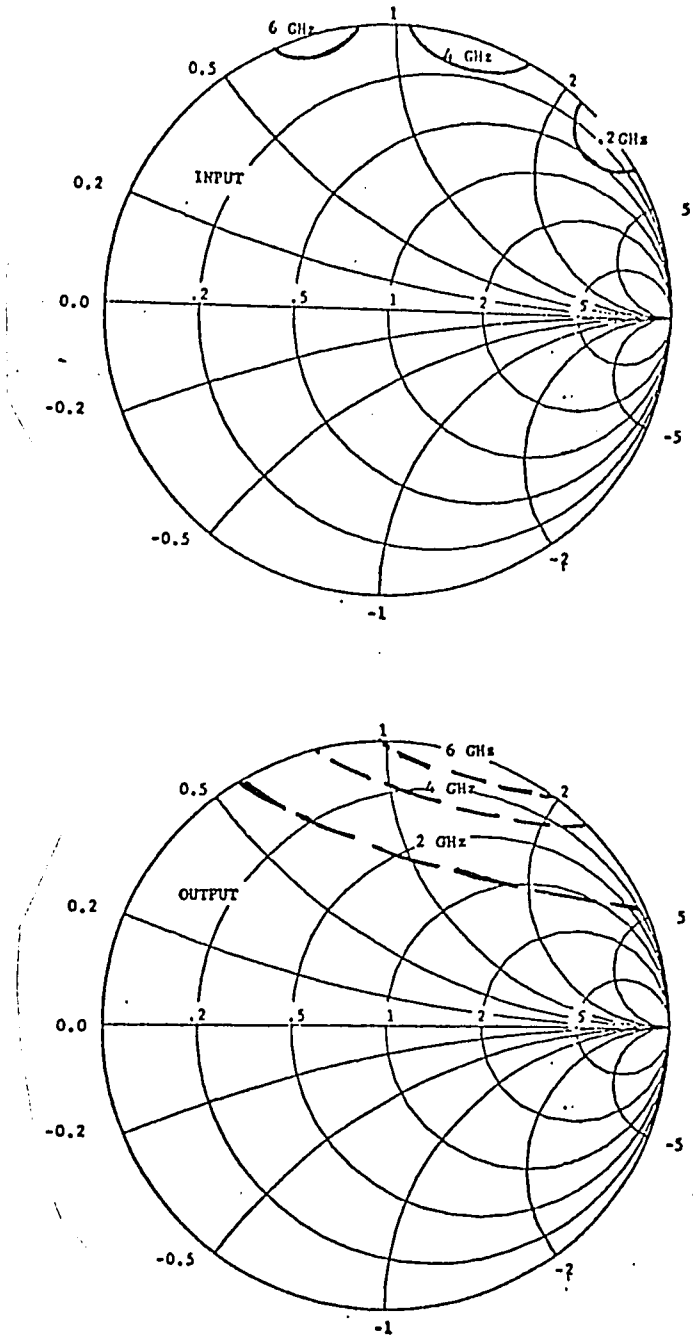

Figure 2-7: Input and Output Stability Circles

investigated.

With the stability circles, the bias ladders were redesigned, and the networks are shown, along with their impedance plots in Figure 2-8. Finally, the test circuits are shown in Figure 2-9.

2.1.3.2. Frequency Limits of Equipment

Once the bias problem was solved, a problem arose in making the load-pull measurements. At the upper end of the band, the HP8411A Harmonic Frequency Converter (which is only rated up to 12 GHz) began to lock on harmonics as well as the fundamental frequency. Because of this, and due to the time needed to assemble more test circuits, modeling was started based on data collected up to this point, and extrapolated to 26.5 GHz. The regions of matching impedances acceptable for the output matching of the single and parallel FET's are shown in Figure 2-10.

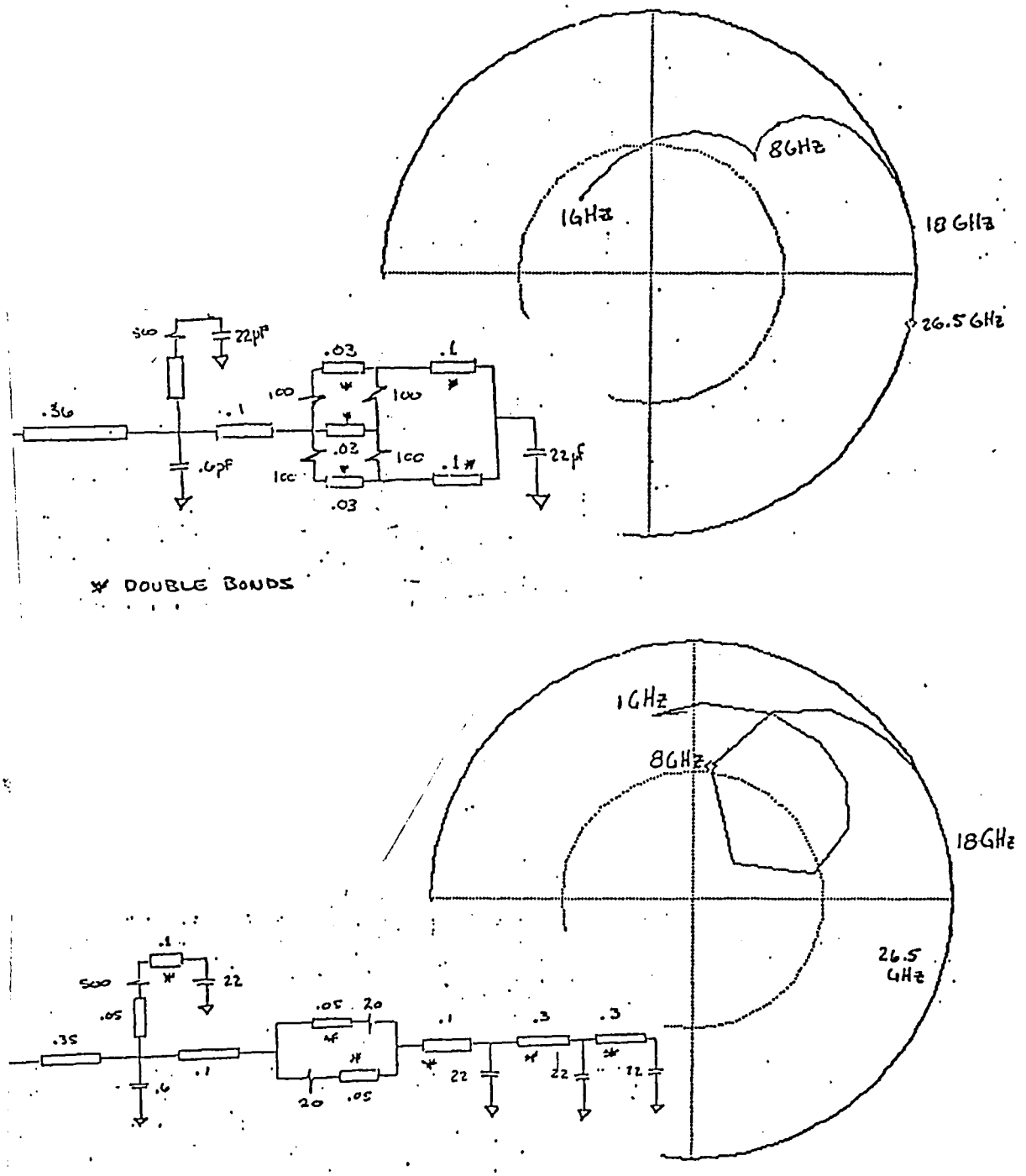

Figure 2-8: Redesigned Bias Ladders and the Corresponding S_{11}'s

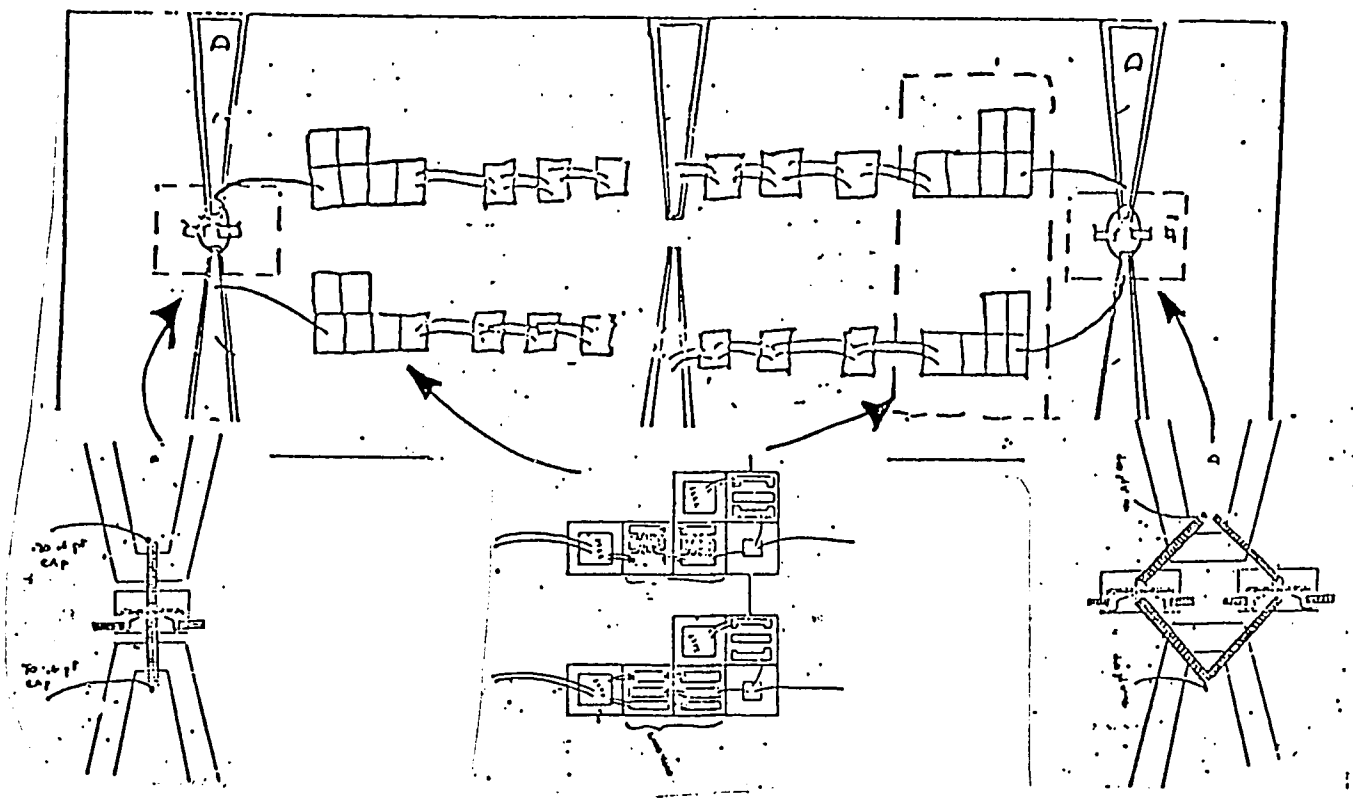

Figure 2-9: Test Circuits

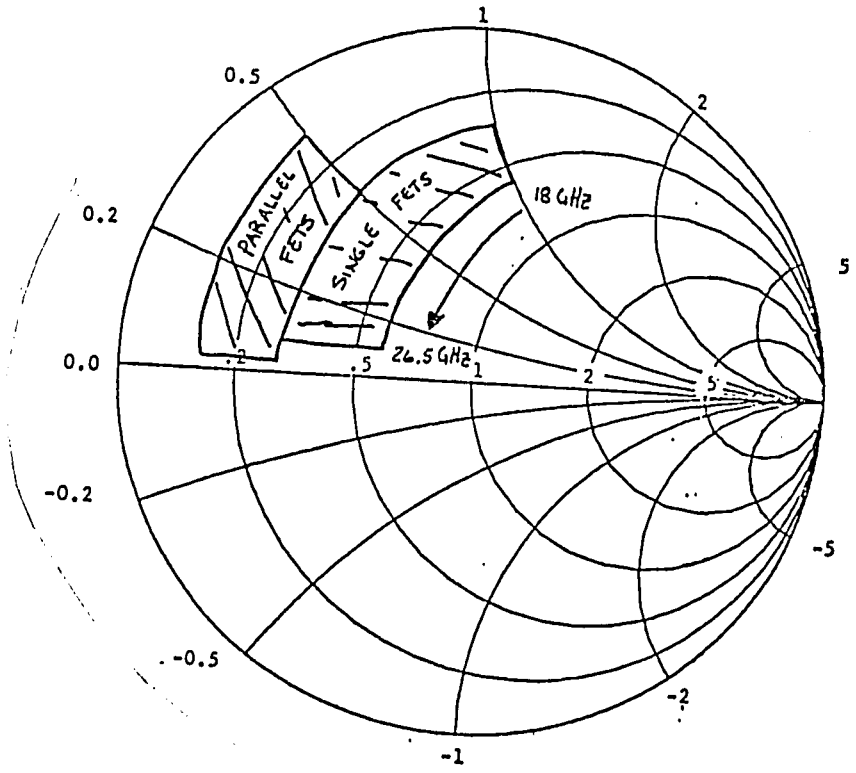

Figure 2-10: Acceptable Impedance Matching Regions

2.2. CIRCUIT SIMULATION

2.2.1. Small-Signal Analysis (OPNODE)

With the load-pull data of the paralleled FET's, an output matching network is developed to transform the 50 ohm termination impedance to the desired matching impedance. The matching network and its corresponding impedance are shown in Figure 2-11. The process used in matching is as follows:

1. A Dolph transformer is used to transform the 50 ohm termination impedance to a lower impedance (see Appendix IV).
2. The series inductance causes a phase shift away from the real axis.
3. The shunt stub causes a resonant circle that causes the impedance to change with frequency in the right direction.

The circuit parameters are optimized for best fit and the impedance calculated and plotted over the range 1-28 GHz to assure stability.

The next step is calculating the input impedance of the paralleled FET's terminated in the output matching network. An interstage matching network is then developed to transform this input impedance to the desired impedance of the single FET. Again, the circuit is optimized to obtain the best fit. The interstage matching circuit and its impedance are shown in Figure 2-12.

With the model of the FET terminated with the interstage network and the second stage, the input impedance is found. An input matching network is developed to match the complex conjugate of this impedance to 50 ohms. Finally, the parameters of the matching networks are varied to obtain gain and flatness over the band. The final circuit and its gain are shown in Figure 2-13.

2.2.2. SPICE Analysis

Once the small-signal circuit is optimized using OPNODE, the same circuit is evaluated with SPICE. The circuit differs only in the model used for the FET. A model developed previously by Hewlett-Packard for the TC-320 is employed (see Appendix II). Both a small-signal (AC) analysis and a large-signal (transient) analysis are performed.

2.2.2.1. AC Analysis

An AC analysis is performed on SPICE and the predicted gain is shown in Figure 2-14. As can be seen, the results are similar to those obtained with OPNODE (see Figure 2-13). It can therefore be assumed that the two models of the FET, although different types of models (see Appendix II), behave nearly the same.

2.2.2.2. Transient Analysis

A transient analysis of the circuit used in the AC analysis is performed at intervals of 500 MHz over the frequency range 17.5-27 GHz, with only the fourier components due to the fundamental frequency being used to calculate power. The results are shown in

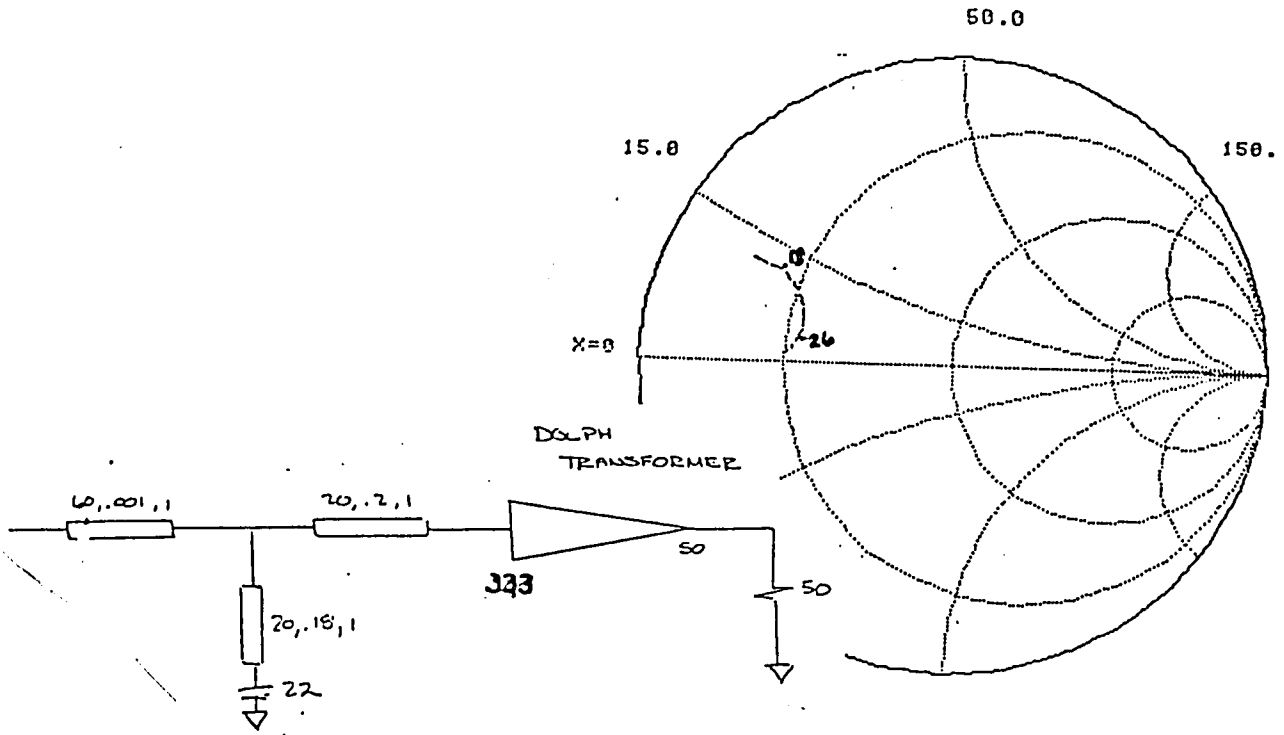

Figure 2-11: Output Matching Network

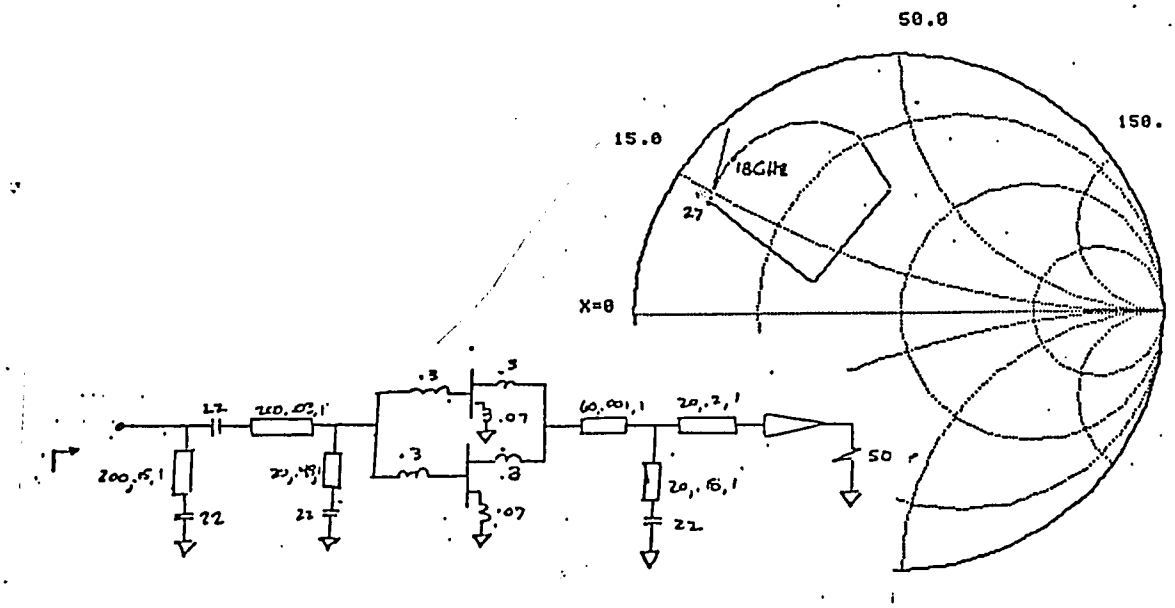

Figure 2-12: Interstage Matching Network

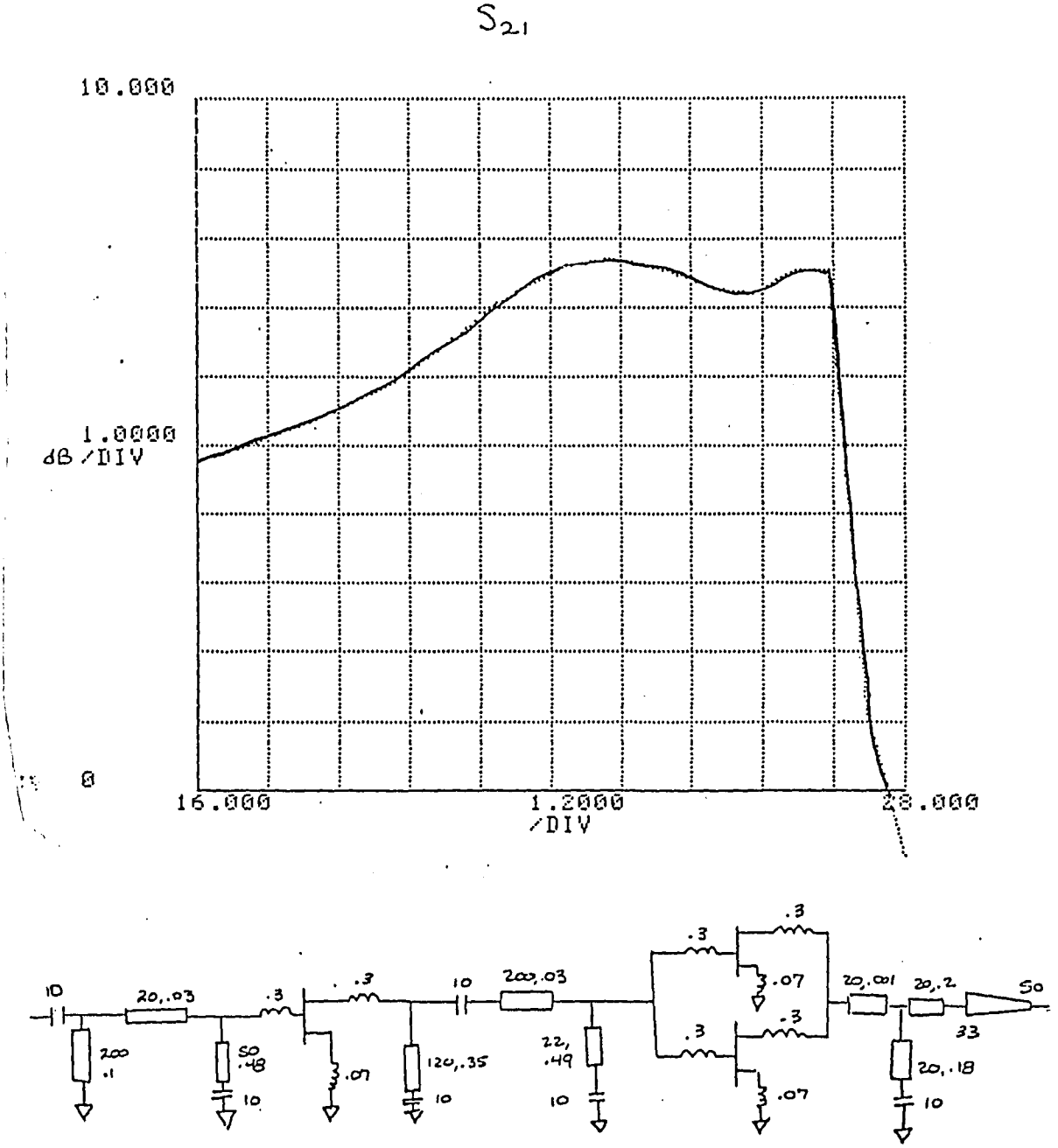

Figure 2-13: Final Small-Signal Circuit and Its Associated Gain

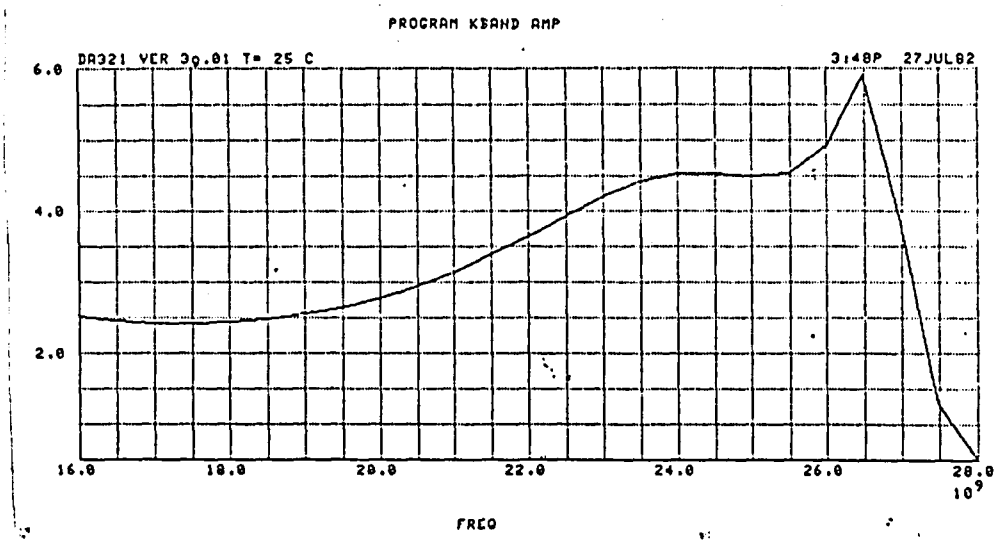

Figure 2-14: Small-Signal Gain Predicted By SPICE

Table 2-1 and plotted in Figure 2-15.

As can be seen, for an average power in of ~10 dBm, a power out of 20 dBm can be expected, where

$$P_{in} = 1/2 \; V_{in} \; I_{in} \; \cos (\Phi_v + \Phi_i)$$

$$P_{out} = (V_{out}/ 2)^2/R_{load}$$

Also, a midband total harmonic distortion of approximately 3.5% can be expected.

Table 2-1: Circuit Transient Results

FREQ (GHz)	Pin (mW)	Pin (dBm)	Pout (mW)	Pout (dBm)	HARMONIC DISTORT (%)	POWER GAIN (dBm)
17.5	13.8	11.41	116.3	20.7	10.3	7.14
18.0	9.5	9.79	97.3	19.9	7.7	6.36
19.0	10.6	10.24	98.1	19.9	7.2	6.40
20.0	11.5	10.61	103.7	20.2	1.3	6.64
21.0	9.3	9.66	100.0	20.0	3.4	6.48
22.0	12.5	10.97	115.6	20.6	3.5	7.11
23.0	11.3	10.51	104.2	20.2	3.5	6.66
24.0	14.6	11.63	128.9	21.1	3.6	7.58
25.0	19.0	12.79	159.0	21.0	1.7	7.49
26.0	21.2	13.26	176.9	22.5	12.3	8.96
26.5	19.6	12.93	132.4	21.2	7.0	7.70
27.0	14.7	11.67	73.6	18.7	2.3	5.15

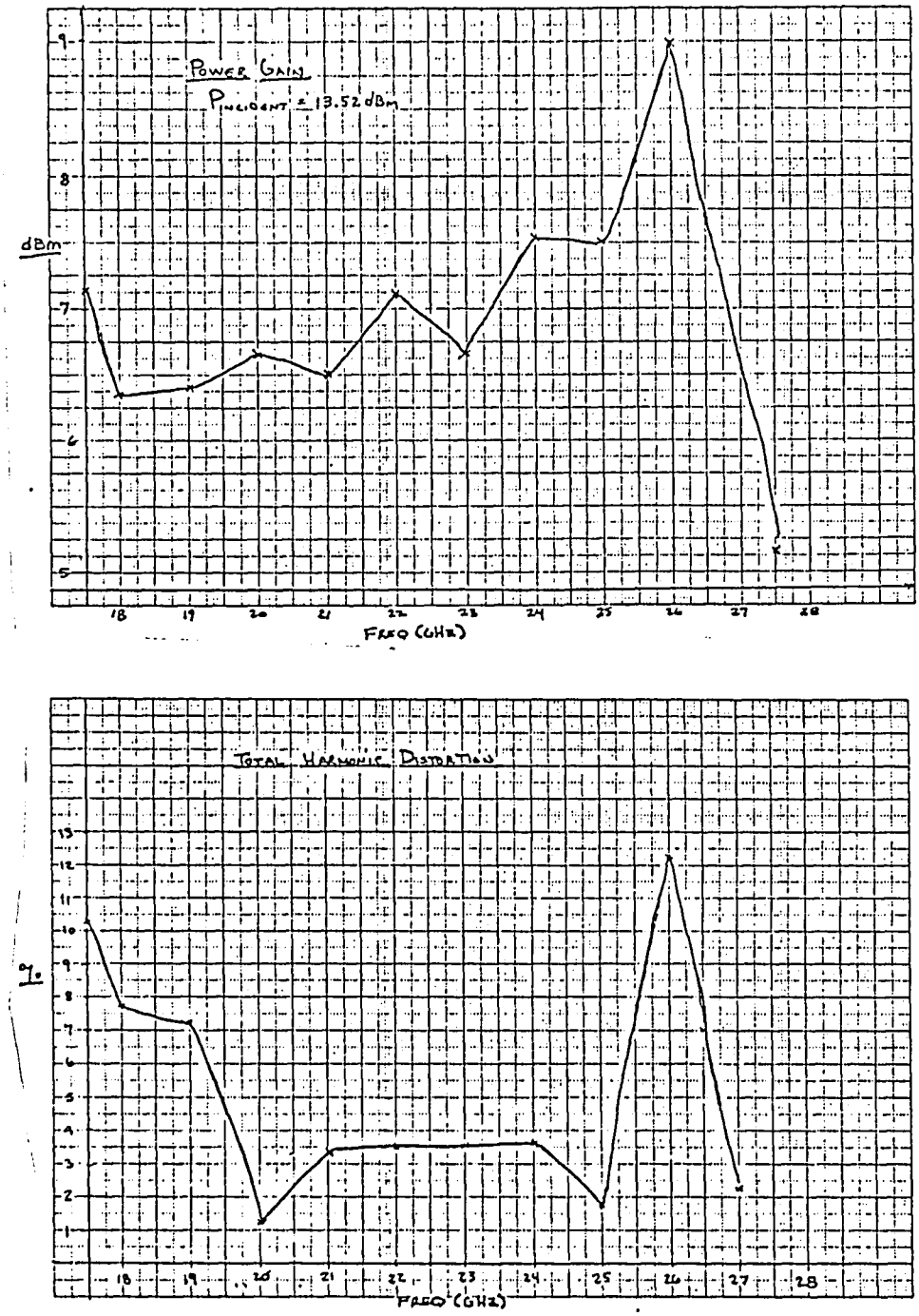

Figure 2-15: Power Gain and Total Harmonic Distortion as Predicted by the SPICE Transient Analysis

3. AMPLIFIER FABRICATION

3.1. Substrate

The circuit is assembled on a Hewlett-Packard TF-II sapphire substrate with dimensions as shown in Figure 3-1. Some of the properties of the sapphire are listed in Table 3-1. The upper limit on the resistance of a transmission line of a given size is set by the minimum line width necessary to bond to (~40μm). The lower limit is set by the minimum distance realizable between conductors (or gap width) of 5-7 μm. These limits are ~120 ohms and ~20 ohms, respectively.

The final substrate drawing is shown in Figure 3-2.

3.2. Assembly

The substrate with components is shown in Figure 3-3. The biggest problem with assembling the circuit was the the small gap width associated with the low resistance lines. Because of the softness of the gold conductor, epoxy die attaching of the components often resulted in a scratch of the substrate which shorted the gap and ruined the substrate. The epoxy die also ran into the gap and, if not seen, resulted in a short when the substrate was heat treated to attach the components. If, by chance, the attaching of the components did not result in a ruined substrate, bonding to the devices often did.

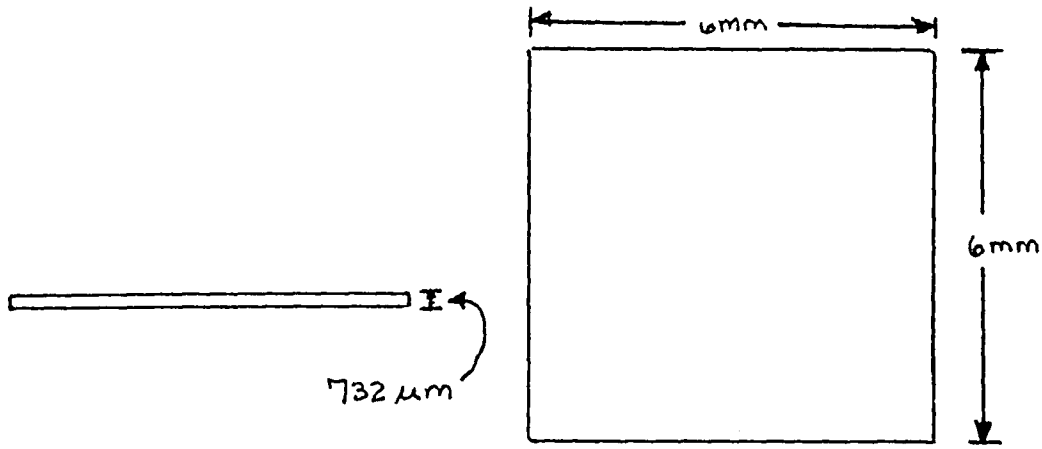

Figure 3-1: Substrate Dimensions

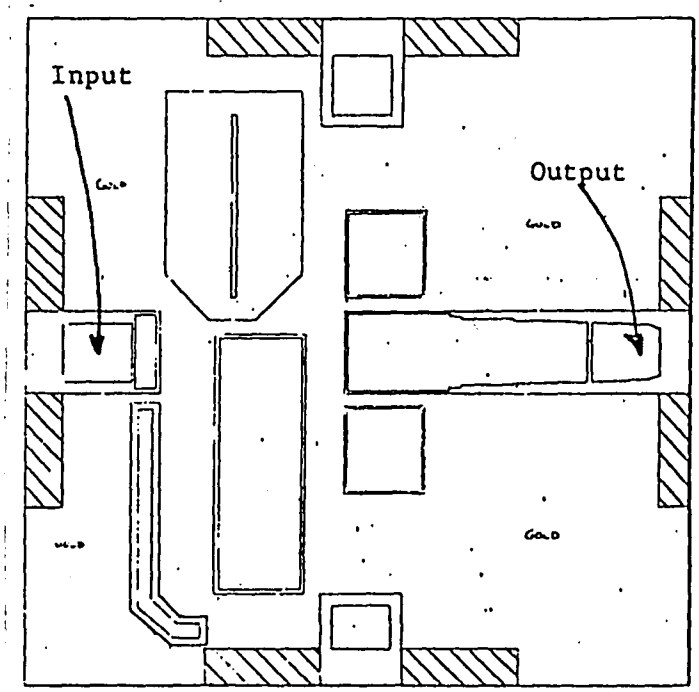

Figure 3-2: Final Substrate Design

Table 3-1: Sapphire Substrate Properties

SINGLE CRYSTAL SAPPHIRE PROPERTIES		
DIRECTIONAL PROPERTIES	PERPENDICULAR TO THE C-AXIS	PARALLEL TO THE C-AXIS
Dielectric Constant @ 25°C up to 8.5 GHz @ 100°C	9.39 9.43	11.58 11.66
Thermal Expansion 20 - 50°C 20 - 500°C	5.0×10^{-6}/°C 7.7×10^{-6}/°C	6.7×10^{-6}/°C 8.3×10^{-6}/°C
OTHER PROPERTIES		
Loss Tangent up to 8.5 GHz	<.0001	
Thermal Conductivity	.46 Watt/cm°C @ 20°C .25 Watt/cm°C @ 100°C	
Density	3.98 gm/cm	
Specific Heat	.18 cal/gram	

Two circuits (of 25 substrates) were eventually completed. The bonded circuit is shown on Figure 3-4. Ribbon mesh was used in place of bond wire wherever possible due to the lower inductance associated with it. This lower inductance was included in the modeling.

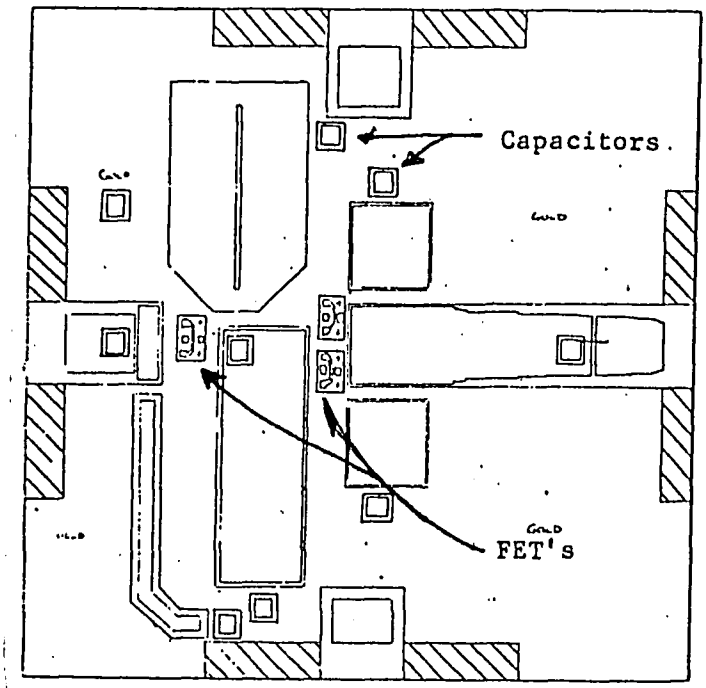

Figure 3-3: Substrate With Components

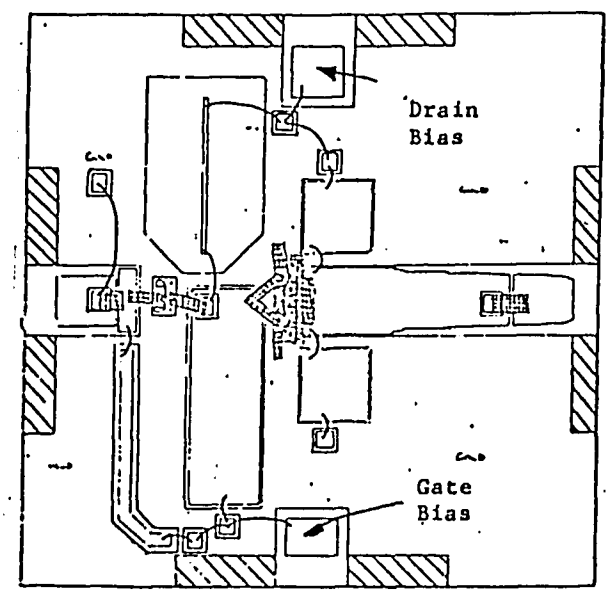

Figure 3-4: Substrate With Bonded Circuit

4. AMPLIFIER TESTING AND ANALYSIS

After a circuit was finally assembled, it was tested on the HP8510 Network Analyzer (not yet released) to determine its small-signal gain, and power measurements were to be taken. However, after seeing the poor gain produced, power measurements were not necessary. The gain of the first circuit is plotted in Figure 4-1.

After reviewing the amplifier fabrication stage, several errors were discovered. First, although the gap between the conductor and ground plane was required to be small on the sides of a transmission line in order to produce a low impedance, the end gaps were not. Because of the small end gaps, bonds to the lines were made a mil or so in to avoid shorting the gap. This resulted in a transmission line several mils shorter than modeled, with open stubs at either end (see Figure 4-2(a)).

Second, it was noted that some of the transmission lines were shorter than they were wide. This, along with uncentered bonds, resulted in transmission lines of higher impedance and longer than modeled (see Figure 4-2(b)).

The third problem involved the continuation of the ground plane. In several instances, the ground plane was continued only through a very thin strip. This strip would transform the short of ground to another impedance at the device. The results of this problem have yet to be investigated.

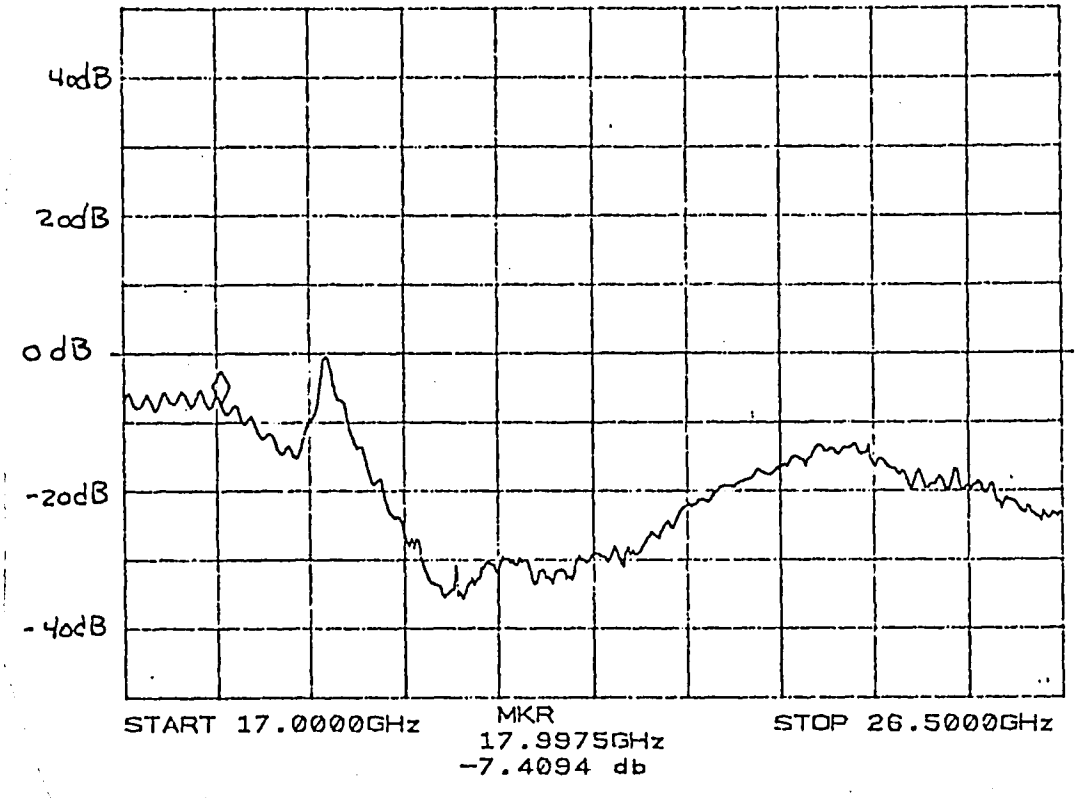

Figure 4-1: Gain of First Circuit

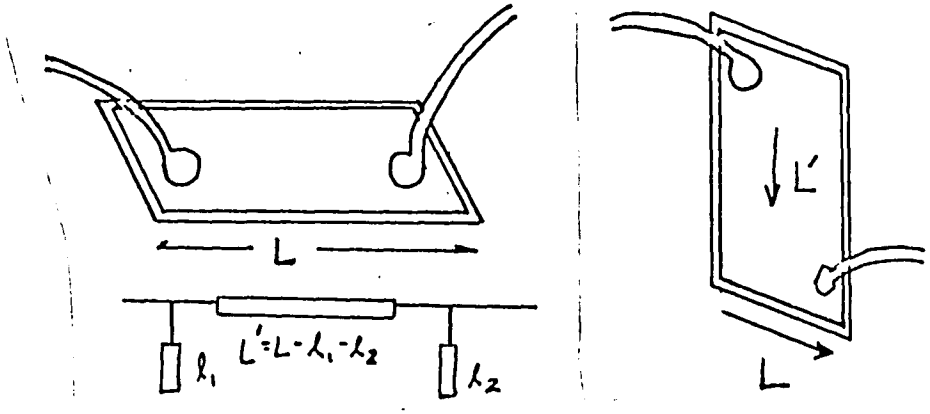

Figure 4-2: Fabrication Errors

The first step in redesigning the amplifier was to adjust the small-signal model to take into account the errors listed above. The gain of the adjusted model was close to the actual results. Since the turn around time on a substrate was atleast two weeks, and not that much time remained, the adjusted circuit was optimized rather than redesigning the substrate. The changes in the original circuit were made by laser trimming some of the transmission lines and the circuit was reassembled. The improved gain is shown in Figure 4-3. A redesign of the substrate would be necessary to achieve predicted results.

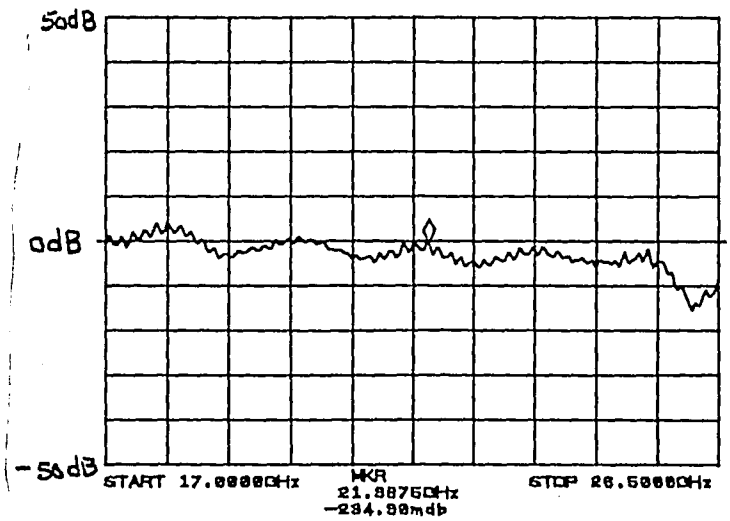

Figure 4-3: Improved Gain

5. FUTURE CONSIDERATIONS

In looking at the design process, several improvements can be suggested. Many of these require steps which will take more time than was available to the author.

In modeling the circuit, the S-parameters of the RF package can be measured, and a model developed. This model can be included in the modeling process.

Also, at each stage of modeling (i.e. output stage, interstage, and input stage), a laboratory model can be built and tested to observe the deviation from predicted behavior.

In designing the substrate, gaps at the ends of the transmission lines can be made large enough to allow bonding to the end of the line. In realizing the substrate, the small gaps can be covered with a scratch protection layer to prevent gapping. Finally, perhaps a larger substrate can be designed to allow for a more continuous ground plane.

And last of all, although all calculations involve determining an effective dielectric constant at midband, perhaps a more rigorous evaluation of the dielectric constant and the phase velocity, taking into account the gap width, will yield much more accurate results. As a last thought, once a working model is obtained, a monolithic circuit as a final product will yield a much more reproducable circuit.

6. CONCLUSION

Although a circuit which meets design specifications is not developed, a promising realizable model is. Also, every stage of an engineering project development is investigated. These stages include device measurement, circuit modeling, computer optimization, substrate design, circuit assembly, testing, and improvement of the original circuit. Only time limitations hinder a successful project completion. However, with the steps mentioned in Chapter 5 and the iterative design procedure introduced in Section 1.3 of this thesis, a circuit which meets design specifications can be developed.

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I. THESIS PROPOSAL

MASTER'S THESIS PROPOSAL
K-BAND POWER AMPLIFIER

April 1982

Jerry Chappell

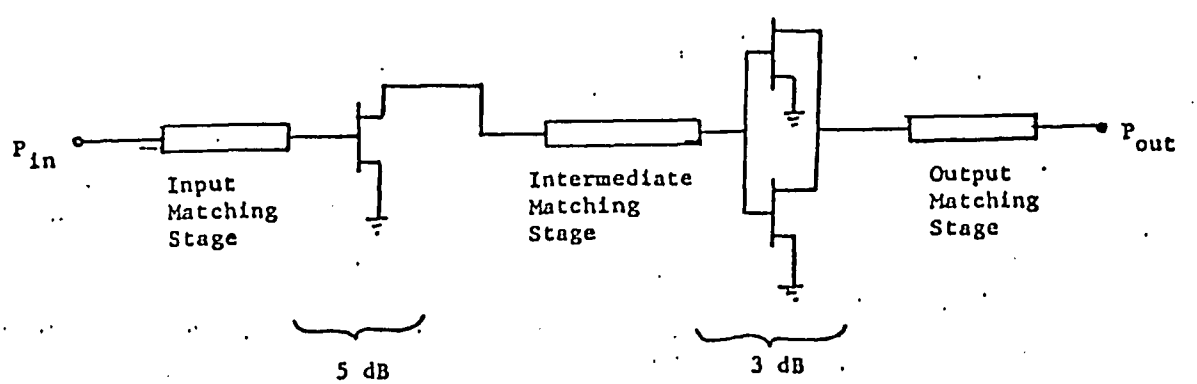
Lehigh University

The object of this thesis is to design a K-band (18-26.5 GHz) power amplifier using FET transistors. The desired specifications are:

- Frequency - 18 to 26.5 GHz
- P_{out} (at P_{in}=13 dBm) = 18dBm (1 dB gain compression)
- Harmonics - less than 20 dBc
- Gain - 8 dB

At this point, Hewlett-Packard's TC-320 transistor is a logical choice. It is a low to medium power FET with typical power out of 16 dBm at 1 dB gain compression. Complete large-signal characterization is not available up to 26.5 GHz; however, a small-signal model exists that should be accurate in K-band. Large-signal "load-pull" data is also available up to 18 GHz. This data can be extrapolated to 26.5 GHz with reasonable accuracy.

A preliminary design is shown:



Since the optimum output match to an FET is strongly dependent on the RF power level, "load-pull" data will be used in the design of the output matching network. The design approach will be as follows:

1. Load pull data will be used to design the output matching network (data adjusted to account for parallel transistors),

2. With this output circuit, design intermediate and input matching circuits with Smith charts and mathematical analysis,

3. These circuits will be optimized with a small-signal circuit simulation program (OPNODE) to achieve desired gain and flatness over the band (input and output blocking capacitors must be included)

4. The results from the small-signal model will be tested on a large-signal model (HPSPICE)

The final design will then be realized on sapphire using a microstrip or coplanar approach. The coplanar approach is the preferred at this time due to ease of assembly and placement of the components on the substrate. Performance data from the circuit will be compared to desired specifications and circuit parameters adjusted as necessary.

Finally, amplifier performance will be related to actual circuit parameters.

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II. TC-320 Transistor

The TC-320 is a GaAs Schottky-barrier field-effect transistor chip with a .5 micron gate length and a gate width of 350 microns. It is a low to medium power chip usable to 26.5 GHz. Common source S-parameters of the intrinsic device are listed in Table 6-1, and the small-signal model used and its corresponding values are given in Figure 6-1[1]. The model has been shown to be good up to 18 GHz and is assumed to be good up to 26.5 GHz. The OPNODE model is listed in Figure 6-2.

The SPICE model for the TC-320 is the confidential property of Hewlett-Packard Company and the equations used to model it cannot be listed. Although the models are of different natures, their predicted performance corresponds extremely well (as seen in Section 2.2.2)

REFERENCES

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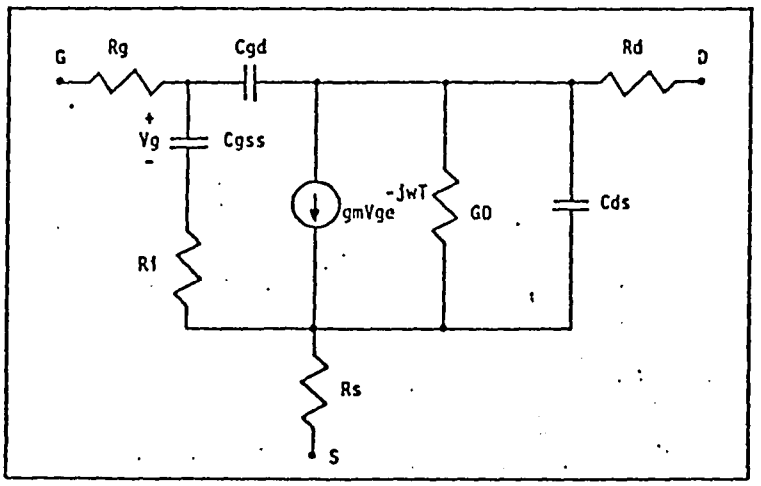
Table 6-1: Typical S-Parameters
(V_{DS} = 5.0 V, V_{GS} = 0.0 V)

FREQ. GHz	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2.00	.988	-18	2.258	162.6	.013	80	.801	-7
3.00	.975	-27	2.205	154.2	.019	75	.798	-10
4.00	.957	-36	2.137	146.1	.024	71	.794	-14
5.00	.937	-44	2.057	138.3	.029	67	.789	-17
6.00	.916	-51	1.971	130.9	.034	63	.785	-20
7.00	.894	-58	1.881	123.9	.038	59	.780	-23
8.00	.873	-65	1.791	117.2	.041	56	.775	-26
9.00	.852	-71	1.702	110.9	.045	53	.771	-29
10.00	.833	-77	1.616	104.9	.047	51	.767	-32
11.00	.815	-82	1.533	99.3	.050	49	.764	-35
12.00	.798	-87	1.456	93.9	.052	47	.761	-37
13.00	.783	-91	1.382	88.8	.054	45	.758	-40
14.00	.769	-95	1.314	83.9	.056	43	.756	-43
15.00	.756	-99	1.250	79.3	.058	42	.754	-45
16.00	.745	-103	1.190	74.8	.059	40	.752	-48
17.00	.735	-106	1.134	70.6	.061	39	.750	-50
18.00	.725	-109	1.081	66.5	.062	38	.749	-52



Typical Values

Rg = 5Ω
Ri = 5Ω
Rs = 2.8Ω
Rd = 5Ω
Cgss = .25 pF
Cgd = .01 pF
Cds = .078 pF
gm = 28 m℧
τ = 4 psec
GD = 2.38 m℧

Figure 6-1: TC-320 Intrinsic Small-Signal GaAs FET Model

```
2000  REM PROGRAM EEM1: TC-320 INSTRINSIC MODEL FROM APPLICATION NOTE
2005  CALL R(2,3,5)
2010  CALL R(4,6,5)
2020  CALL R(6,0,2.8)
2030  CALL R(5,6,420)
2050  CALL R(5,7,5)
2060  CALL C(3,4,.25)
2080  CALL C(3,5,.01)
2100  CALL C(5,6,.078)
2170  CALL DELAY(3,4,10,11,.004)
2190  CALL VDCS(10,11,5,6,.028,0)
2210  CALL R(10,11,10000)
2220  REM A1,A2: INPUT PORTS, B1,B2: OUTPUT PORTS
2230  LET A1=2
2240  LET A2=0
2250  LET B1=7
2260  LET B2=0
```

Figure 6-2: OPNODE TC-320 Model Listing

III. LOAD-PULL

CALIBRATION SCHEME

Refering to Figure 6-1, the calibration scheme is as follows:

1. Connect short to point 1 and tune input tuner for maximum deflection on meters A and B,

2. Connect power meter to point 1 and measure power delivered in watts. Leave this constant from now on. Read power meter A (incident power); meter B (reflected power) should read zero. This gives the calibration factor for meter A, k_A. The actual incident power is:

$$P_{inc} = P_{\text{reading of A}} \, (W/X)$$

where W = power delivered in watts, X = power reading of meter A with a power meter connected to point 1, and the calibration factor k_A is the ratio W/X.

3. Connect a short to point 1. From step 2 we can calculate P_{inc}. Now, the reading of meter B should be equivalent to P_{inc}. Therefore,

$$P_{ref} = P_{\text{reading of B}} \, k_A \, (A/B)$$

where A is the reading of meter A with a short at point 1, B is the reading of meter B with a short at point 1, and the calibration factor of meter B, $k_B = k_A(A/B)$.

4. With the short still connected to point 1, calibrate the input differential meter. This is done by (see Figure 6-2):

   a. zeroing the meter

   b. Adjusting the attenuator (which is placed at the input of either A or B, whichever is larger) until meter zeros

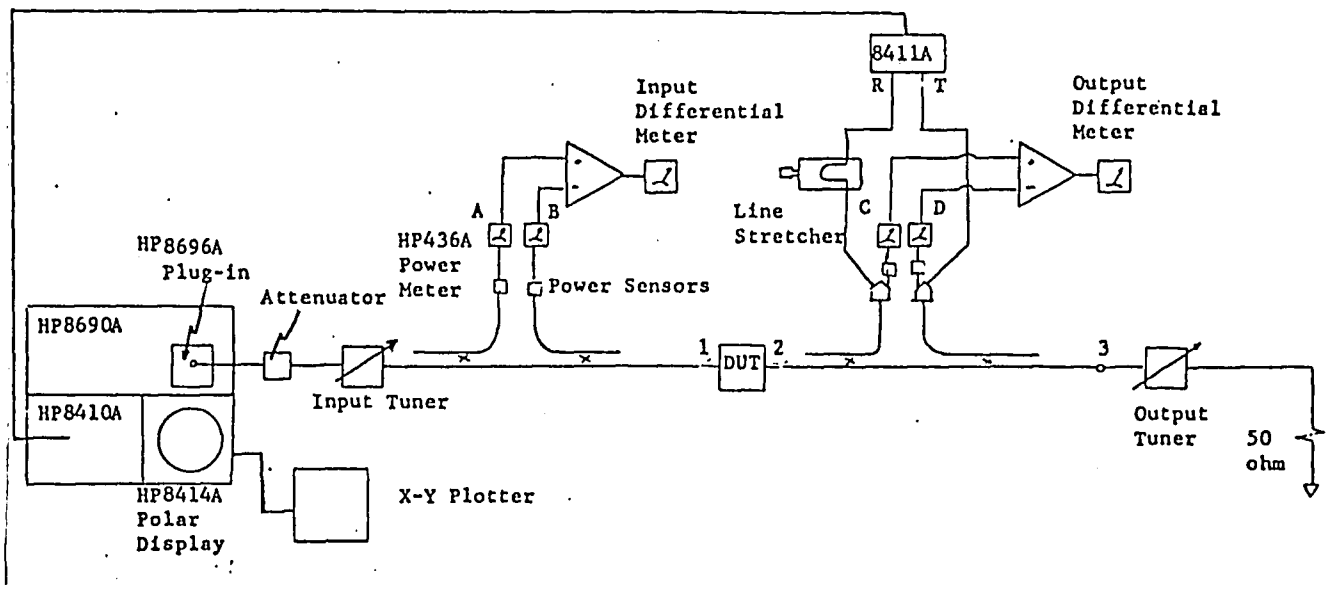


Figure 6-1: Load-Pull Setup

c. Adjust scale factor such that the deflection of the differential meter is approximately that of meter A.

5. For calibration of second stage, place a thru-line between points 1 and 2 and read the power at point 2. Connect the second stage, place a 50 ohm load at point 3, and set meter C equal to the power read at point 2. this gives:

$$P_{inc} = P_{\text{reading of C}} \ (V/Y)$$

where V is the power in watts read at point 2, Y is the meter reading of C, and the calibration factor for meter C is, $k_C = V/Y$.

6. Now, connect point 1 to point 3 and terminate point 2 with a short. Read meter C and calculate P_{inc} from step 5. Meter D should be equivalent to this. Therefore,

$$P_{ref} = P_{\text{reading of D}} \ k_C \ (C/D)$$

where C is the reading of meter C with a short at point 2, and D is the reading of meter D with a short at point 2. The calibration factor for meter D is $k_D = k_C \ (C/D)$.

7. Now with the short still at point 2, calibrate the differential meter on the output according to step 4.

8. With the short still attached, adjust the line stretcher and the phase and gain vernier so that the impedance presented on the polar display is a short. Assemble the setup as shown in Figure 6-1 for measurements.

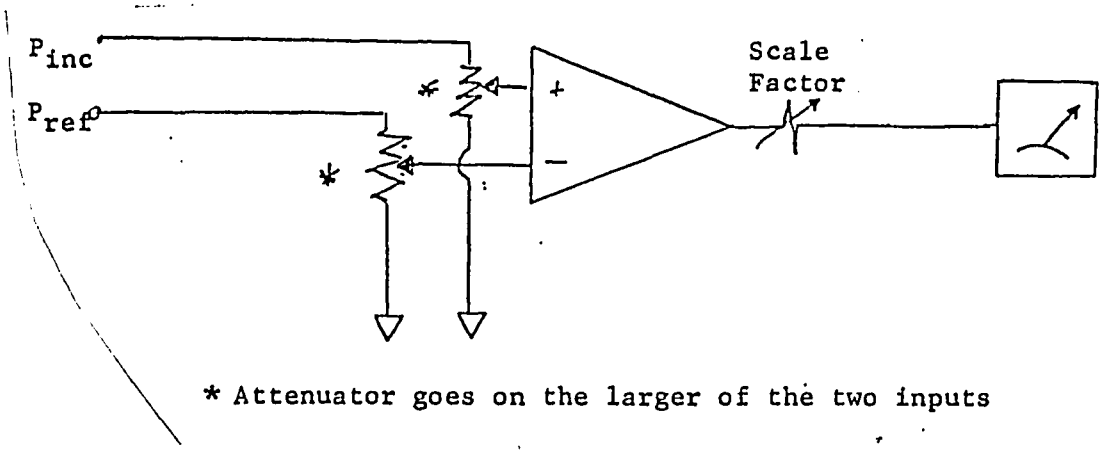


Figure 6-2: Diagram For Differential Meter Calibration

MEASUREMENT SCHEME

1. Adjust output tuner to find maximum output power,

2. Calculate the maximum power out using meter readings for C and D and the calibration factors,

3. Set scale factor on output differential meter to zero dBm,

4. Keeping P_{in} constant, adjust output tuner until output differential meter reads -1 dBm. Find and plot enough points to define a contour.

5. Repeat the above step for -2 dBm and -3 dBm.

IV. DOLPH TRANSFORMER

The Dolph transformer was first simulated by placing a 100 ohm resistor in parallel with the 50 ohm load impedance. However, in order to design the circuit, the transformer had to be analyzed and designed. A computer program was used which, when given the low impedance (Z_o), the high impedance (Z_1), the minimum ripple desired (R_r), and the minimum frequency (f_{min}), calculated the minimum length of the transformer in air by the following equation[1]:

$$L_{air} = \frac{c}{2.54(2\pi f_{min})} \ln\left[R_1 + \sqrt{R_1^2 - 1}\right]$$

where c is the speed of light in a vacuum, $R_1 = R_o/R_r$, and,

$$R_o = \left|\frac{Z_o - Z_1}{Z_o + Z_1}\right|$$

Now, given the groundplane spacing, the dielectric constant, and the substrate thickness, a coplanar realization is calculated using

$$\ln(Z) = .5 \ln(Z_o Z_1) + \frac{R_o}{\cosh(A)} \{A^2 \blacklozenge(2x/L, A) + U(x-L/2) - U(-x-L/2)\} \qquad |x| \leq L/2$$

$$= \ln(Z_1), \quad x > L/2$$

$$= \ln(Z_o), \quad x < -L/2$$

where,

$$A = \ln \left[R_1 + \sqrt{R_1^2 - 1} \right]$$

U is the unit step defined by

$$U(Z) = 0 \quad , \quad Z < 0$$
$$U(Z) = 1 \quad , \quad Z \geq 0$$

and Φ is defined by

$$\Phi(Z,A) = -\Phi(-Z,A) = \int_0^Z \frac{I_1(A\sqrt{1 - y^2})}{A\sqrt{1 - y^2}} \, dy \quad , \; |Z| \leq 1$$

and I_1 is the first kind of modified Bessel function of the first order. The solution of Φ is given by[2] in the form of a Fortran program.

Once the characteristic impedance is known, the ratio of A_1/B_1 is calculated from[3]:

$$Z_o = \frac{30\pi}{\sqrt{\epsilon_{re}}} \frac{K'(k)}{K(k)}$$

and

$$\frac{K(k)}{K'(k)} = 1/\pi \ln \left[2 \frac{1 + k}{1 - k} \right] \quad \text{for } .707 \leq k \leq 1$$

$$\frac{K(k)}{K'(k)} = \pi / \ln \left[2 \frac{1 + k'}{1 - k'} \right] \quad \text{for } 0 \leq k \leq .707$$

where,

$K(k)$ is the complete elliptic integral of the first kind,

$k = S/(S + 2W) = A_1/B_1$

$k' = (1 - k^2)^{1/2}$

Once k and the characteristic impedance Z are known, the effective dielectric constant is calculated according to[3]:

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} \left[\tanh \{1.785 \log (h/W) + 1.75\} + kW/h \{.04 - .7k + .01(1 - .1\epsilon_r)(.25 + k)\} \right]$$

where h is the substrate thickness.

The relative velocity is then calculated by:

$$v_r = 1 / \sqrt{\epsilon_{re}}$$

The length of the transformer is then calculated by:

$$L_{sapphire} = v_r L_{air}$$

Since the sapphire medium is non-homogeneous, the effective dielectric constant is approximately 10 (see Figure 6-2).

The values for a 20-segment Dolph transformer are given in

Table 6-1 for a groundplane spacing of 732 microns, a dielectric constant of 10, and a substrate thickness of 640 microns.

A model of the Dolph transformer was created and the model plugged into the circuit model in place of the 100 ohm shunt resistor. The change produced was negligible.

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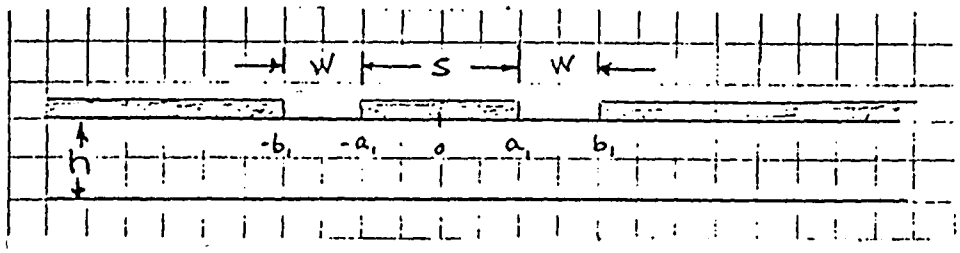

Figure 6-1: Coplanar Waveguide Geometry

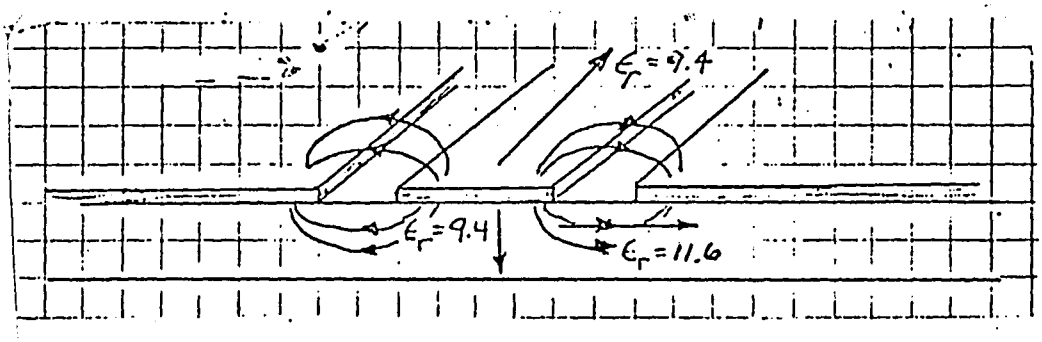

Figure 6-2: Dielectric Constants of the Non-Homogeneous Substrate

Table 6-1:

DOLPH TRANSFORMER

ZO(LOW)=33 ZO(HIGH)=50 RHO=.1 FREQ(MIN)=16 GHZ

ER 10 THICKNESS .64 G= .7

VR	X(MM)	X(IN)	A1/B1	Z0
.44319	0	0	.861303	33.0971
.447353	9.04792E-02	3.56217E-03	.804868	36.8623
.447696	.181416	7.14237E-03	.79909	37.2229
.448043	.272423	1.07253E-02	.792975	37.6007
.44839	.363501	1.43111E-02	.786533	37.9944
.448735	.454649	1.78996E-02	.779775	38.403
.449075	.545866	2.14908E-02	.772718	38.8253
.449405	.637152	2.50847E-02	.765382	39.2597
.449722	.728503	2.86812E-02	.757788	39.7048
.450024	.819917	3.22802E-02	.749965	40.1589
.450308	.911391	3.58815E-02	.741943	40.6202
.45057	1.00292	.039485	.733757	41.0868
.45081	1.0945	4.30906E-02	.725444	41.5567
.451025	1.18613	4.66979E-02	.717044	42.0278
.451214	1.27779	5.03069E-02	.708601	42.4981
.451376	1.3695	5.39172E-02	.700163	42.9654
.451512	1.46123	5.75288E-02	.691768	43.4275
.451622	1.55299	6.11413E-02	.683467	43.8822
.451706	1.64477	6.47546E-02	.675304	44.3275
.451767	1.73656	6.83685E-02	.667326	44.7612
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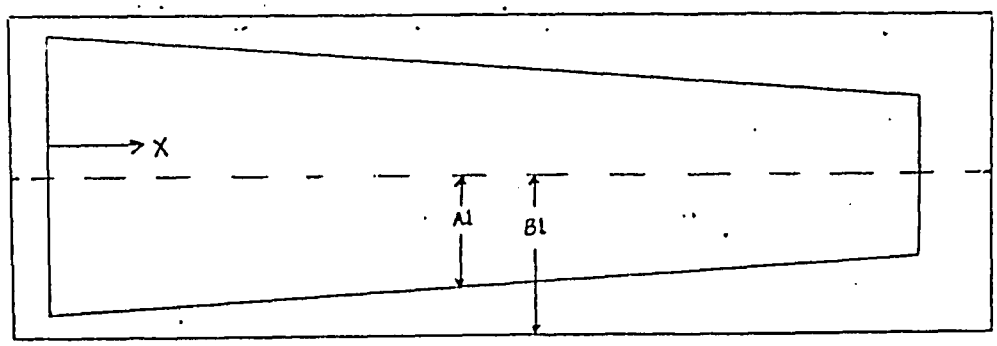

VITA

Gerard N. Chappell Jr. was born on June 27, 1959 in Cherry Point, North Carolina, the son of Gerard and Maureen Chappell. He received his BSEE from Lehigh University in June 1981. His professional experience includes two summers with Hewlett-Packard's Technology Center Device Applications Group in Santa Rosa, California.