A remote energy monitoring power-line carrier system.

Edward T. Wagner

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A REMOTE ENERGY MONITORING
POWER-LINE CARRIER SYSTEM

by
Edward T. Wagner

A Thesis
Presented to the Graduate Committee
of Lehigh University
in Candidacy for the Degree of
Master of Science
in
Electrical Engineering

Lehigh University
1984
This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

5/10/84
(date)

Professor in Charge

Chairman of Department
ACKNOWLEDGEMENTS

The writer wishes to express his gratitude to the following:

- To Professor Carl S. Holzing for his advice and guidance throughout the course of this work.

- To Mr. William P. Haller for his encouragement and assistance.

- To Lehigh University for providing this opportunity and the funding for the writer's Teaching Assistantship.

- To the Scitronics Corporation for their generous support.

- And finally, the writer wishes to thank his parents for their love and inspiration.
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ABSTRACT

The design, implementation, and evaluation of an accurate, low-cost system which remotely monitors electrical energy consumption is described herein. Energy consumption is measured by a number of separate sensors which report to a central computer by means of 131 KHz carrier signals which are superimposed on the 60 Hz power lines. This energy monitoring system computes true energy consumption regardless of power factor or waveform distortion, to an accuracy of 2 percent of full scale, and uses an S-100 based computer to control the reporting function of the remote sensors. This type of system would find use in condominiums, apartment buildings or office complexes where it is desired to distribute the electric bill for the building proportionately based on the energy consumed by the individual tenants.
1. INTRODUCTION

The purpose of this thesis is to develop a system to remotely monitor the electrical energy consumed at any number of separate points in a building, from one central location. This is accomplished through the use of the existing 60 Hz wiring as a communications link between a large number of remote energy measuring units, and one central receiving and control unit. The communication is accomplished by superimposing high frequency carrier signals (131 KHz and 134 KHz) onto the power lines.

This type of system would be useful in an apartment building, condominium or office complex, where the total electrical energy consumption for the building is the only measurement presently made (by the power company). In such a situation, every tenant is billed a fixed amount for electric energy, regardless of the amount actually used. The energy monitoring system described herein would provide a means for the owner of the building to distribute the electric bill proportionately and equitably based on individual use.

The energy monitoring system accurately computes the true energy consumption regardless of power factor or waveform distortion, or type of distribution system. This is accomplished through the multiplication of scaled versions of the actual current and voltage waveforms, and
then integration over time for each of the individual unit loads in the building. The accumulated information is sent in a digital fashion over the power lines to the central receiver, based on the presence or absence of the 131 KHz carrier frequency. Because this signal must be coupled to the power lines, the impedance characteristics of power lines at 131 KHz was studied in detail. The reporting function of the remote units is controlled by the central receiver, which makes use of an S-100 based computer.

Distinct advantages are offered by the remote energy monitoring system over other alternatives. The installation of conventional power meters in each apartment is impractical for a number of reasons. First, more than one meter may be required in each apartment because of the fact that in many cases there will be more than one distribution panel in each apartment. Second, someone must gain physical access to each meter so that they can be read monthly, which might amount to as many as 1000 meters for one building. And third, conventional meters are large, ugly, relatively expensive, subject to vandalism, and difficult to install in an existing structure.

The energy monitoring system described herein utilizes one circuit card (remote unit) to monitor energy
consumption for any number of distribution panels in a particular apartment. The "reading" of these remote units is accomplished by a computer, resulting in a great savings in time and labor. The circuit cards which do the energy measuring will be small, relatively inexpensive, easy to install, and hidden behind the power distribution panels, never needing to be disturbed after the initial installation, except for possible repairs in rare instances. Also, the energy monitoring system has the further advantage of utilizing the existing 60 Hz wiring in the building, so there is no need to run extra wires to provide communication between the remote units and the central receiver.

The complete system design and operation is described in detail in the following sections.
2. SYSTEM OPERATION

The basic energy monitoring system consists of two different parts, the remote measuring unit (RMU), and the central receiving unit (CRU). In a particular application, a large number of RMU's (one for each apartment), and one CRU will be used. The RMU's are linked to the CRU by the 60 Hz power lines, which serve as a communications bus. The central receiving unit is made up of: 1) a computer which contains the capacity to drive a standardized 100 pin bus (S-100 bus), 2) a special circuit card which connects to the S-100 bus and contains circuitry to interface between the computer and the 60 Hz power lines, and 3) software which controls the operation of the CRU. A block diagram of the energy monitoring system is shown in figure 2-1.

One RMU will be placed in each apartment in the building to monitor the energy consumed in that apartment. In some cases, there may be more than one power distribution panel in each apartment. In order to provide the voltage and current inputs for all sources of power in the apartment, wires are run from the RMU which resides in one distribution panel, to all other panels in the apartment.

The current input for the RMU is obtained from a standard current transformer, with a single turn primary
Figure 2-1: System Block Diagram
Figure 2-1: System Block Diagram
and a multiple turn secondary, which provides a scaled version of the actual current waveform. The voltage input for the RMU is obtained by directly dividing down the line voltage through a resistive divider, resulting in a scaled version of the actual voltage waveform.

The RMU computes the real power consumed by multiplying these two waveforms and integrating over time, providing a measure of the total energy consumed. The accumulated energy information is held in a register (accumulator) as a 12 bit binary word. This binary word must, at some point in time, be transmitted to the CRU.

In order to determine that the RMU is functioning properly, a 4 bit constant (preamble) is adjoined to the 12 bit energy data word. Therefore, each RMU reports a 16 bit data word (shown in figure 2-2) to the CRU.

It is the function of the single CRU to initiate a report cycle nightly. During this report cycle, each RMU has a specific time interval (frame) during which it reports energy data to the CPU. The reported energy data is a measure of the total energy consumed in an apartment since the last report cycle. On the RMU, the digital energy data is used to modulate a 131 KHz signal, which is superimposed on the power lines, resulting in an Amplitude-Shift Keyed signal (ASK). The presence of the 131 KHz signal indicates a logic "1", and its absence
Figure 2-2: Energy Data Word
indicates a logic "0". The CRU records the energy data from each RMU, and at the end of the month, computes a bill for each tenant. The bill is based on the actual total energy consumed by the tenant.

In the energy monitoring system, it is desired to minimize the probability that an error will occur in the transmission of data. Since the primary function of the power lines is not to transmit carrier signals, but to deliver 60 Hz power, errors in carrier transmission could occur due to transients on the power lines caused by the switching of loads, the turning on and off of appliances or lights with commercially available power line carrier systems, etc. A minimum of such activity would be expected during the early hours of the morning (e.g. 2:00 A.M.). Therefore, the report cycle is designed to take place during the early hours of the morning to reduce the possibility of interference which could cause errors in the data transmission.

In order to initiate the report cycle, the CRU superimposes a specially configured ASK modulated 134 KHz signal onto the power lines. The fact that there is a 3 KHz difference between this frequency and the RMU reporting frequency serves a specific function, which will be explained further in Chapter 5. As described in detail in Section 5.7, the RMU's have been designed to
Figure 2-3: Report Cycle Initiation Waveform
recognize only a 134 kHz signal having the following form: "on" for 1 second, "off" for 1/4 second, and "on" for 2 seconds. This waveform is shown in figure 2-3, and will be referred to as the "report cycle initiation waveform." The final "on" to "off" transition of the report cycle initiation waveform serves as a time synchronizing mark for all RMU's. At this point, all RMU's simultaneously start counting up to a preset number which is unique to each RMU. When an RMU reaches the preset number, it is its "turn" to send information to the CRU. In this way, the RMU's sequentially send their information to the CRU. An RMU is allotted a 10.667 second frame in which to report its data, as depicted in figure 2-4. The energy data, along with the preamble (the 16 bit data word), is sent five times during this frame to provide redundancy which allows the computer to correct, to a certain extent, possible bit errors by a simple majority vote. For 500 RMU's (a representative number) the total report cycle would take approximately 1-1/2 hours to complete.

It is important that no two RMU's report at the same time, because in that case, two data words would be superimposed upon one another, which would be completely unintelligible to the CRU. Therefore, each RMU has its own individual, 10.667 second reporting frame. Once the
Figure 2-4: RMU Reporting Frames
CRU initiates the report cycle, it must wait and receive information from every single RMU. This is for two reasons. First, the CRU cannot stop the report cycle once it is initiated because it has no control over individual RMU's, except to initiate the report cycle. Secondly, once an RMU has reported, it is designed to automatically clear its accumulator to zero in preparation for accumulating the next day's energy data. Therefore, if the CRU initiates the report cycle, but fails to wait for its completion (by being turned off, or by being interrupted by the operator to perform some other task), the energy data for some RMU's will be totally lost.

Although a nightly report cycle is anticipated, provision has been made so that each accumulator can hold more than three or four days of accumulated energy data. This is done so that in the event that a computer malfunction occurs, which might delay the report cycle for two or three days, the energy data can eventually be gathered intact. Since nightly reporting will take place in most cases, it is possible to accurately determine the proper billing even when tenants move in and out in the middle of the month, simply by providing the computer with the day the move will take place.

The above is a basic description of the operation of
the energy monitoring system as a whole. More specific information on the details of the design and operation of the individual parts of the system (i.e. RMU, CRU) is given in the remaining chapters. For purposes of efficiency in the explanation, the circuits of the RMU and the CRU are broken down into smaller functionally related blocks. It should be noted that these blocks go together to make up the complete RMU or CRU.
3. CHARACTERIZATION OF POWER-LINE IMPEDANCE

3.1 Purpose

The impedance characteristics of 120VAC power lines at carrier frequencies was studied in detail. The reasons for this were twofold: first, to determine the necessary output circuitry to drive the power lines at the carrier frequency, and second, to estimate the optimum carrier frequency which should be used. A mathematical calculation of the expected impedance was performed, SPICE computer circuit simulations were used to test the theory, and physical measurements on power lines were made to compare the results.

3.2 Calculation of Impedance of Two Wire Line

The model of figure 3-1 was used to calculate the impedance of a two-wire line, such as would be used to distribute electric power in a building. The wire size used in the calculations was #12 AWG, which is used as an approximation to the type of wire which might be found in a building where the energy monitoring system might be used. It is desired to calculate the inductance, capacitance, and resistance of this parallel, two-wire transmission line. Lumped circuit parameter approximations are utilized, considering the fact that the wavelength of carrier signals at frequencies of 100
#12 AWG COPPER WIRE (INSULATION NOT SHOWN)

\[ r = 1.027 \times 10^{-3} \text{ m} \]
\[ d = 6.118 \times 10^{-3} \text{ m} \]

**Figure 3-1:** Two Wire Power Line
to 200 KHz is approximately 2 kHz, which is much longer than the expected height of a building in which this system would be used (20 stories = 60 m).

It can be shown [2] that for the two-wire line in figure 3-1, the capacitance per unit length is given by:

\[
\frac{C}{l} = \frac{\pi \varepsilon_0 \varepsilon_r}{\ln((d + \sqrt{d^2 - 4r^2})/2r)}
\]  

(3.1)

This is assuming that the entire space is uniformly filled with the dielectric (insulation) which is a valid approximation considering the highest intensity field will be between the wires, where the insulation does exist.

Similarly, it can be shown [8], that the inductance per unit length of the line is given by:

\[
\frac{L}{l} = \frac{\mu}{\pi} [\ln(d/r) + 1/4]
\]  

(3.2)

This equation accounts for the inductance due to fields both internal and external to the conductors.
To calculate the resistance of the wire at carrier frequencies, it is necessary to account for skin effects. The skin depth in meters for a solid copper conductor is given by [131]:

\[ \delta = \frac{0.066}{\sqrt{f}} \]  \hspace{1cm} (3.3)

And, for an anticipated carrier frequency of 131 KHz, \( \delta = 0.1824 \) mm. Therefore, the ratio of the radius to the skin depth for #12 AWG is equal to:

\[ \frac{r}{\delta} = 5.5 \]  \hspace{1cm} (3.4)

And, for this value, the ratio of high frequency resistance (131 KHz) to D.C. resistance is:

\[ \frac{R}{R_{DC}} = 3.0 \]  \hspace{1cm} (3.5)
from curves given in [13] on page 297.

Therefore using the following values for insulated #12 AWG wire:

\[
R = 5.211 \times 10^{-3} \ \Omega/m
\]

\[
\varepsilon \text{ (insulation)} = 2.5
\]

\[
\varepsilon_0 = 8.854 \times 10^{-12} \ \text{F/m}
\]

\[
\mu = \mu_0 = 4\pi \times 10^{-7} \ \text{H/m}
\]

the following values can be calculated using equations (3.1), (3.2), (3.5).

\[
C = 39.62 \times 10^{-12} \ \text{F/m}
\]

\[
L = 813.8 \times 10^{-9} \ \text{H/m}
\]

\[
R = 15.63 \times 10^{-3} \ \Omega/m
\]

These values were utilized in the SPICE computer simulations presented in section 3.4.
3.3 Power-Line Impedance Measurements

Measurements were made of the driving point impedance of the power lines in a number of buildings. The measurements were made with a dual-trace oscilloscope and a Hewlett-Packard 1111A current probe, which interfaces directly to the oscilloscope. The power line was driven at 131 KHz (into a duplex outlet) with the output circuit of the RMU, and the current and voltage waveforms were displayed on the face of the scope. From magnitude and phase measurements, the driving point impedance of the power lines was calculated. Care must be taken when making such measurements, that the line filters of the measuring equipment, whose purpose is to filter out high frequency noise (>60 Hz), do not affect the measurement. A small inductance could be added in series with the line cords of the measuring instruments to avoid such problems. For the purposes of this work, a Tektronix 922 scope was used, which was determined not to affect the measurements.

The results of the measurements are shown in table 3-1. These values by no means represent the total number of possibilities, as a wide range of impedances would be expected due to variations in loading. However, these values are meant to be typical of the types of impedances which would be observed in applications of the energy
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<tr>
<td>Packard Lab 331 ($\phi$ 1)</td>
<td>$4.5 + j13.0$</td>
</tr>
<tr>
<td>Packard Lab 331 ($\phi$ 2)</td>
<td>$10.0 + j16.0$</td>
</tr>
<tr>
<td>Packard Lab 331 ($\phi$ 3)</td>
<td>$9.0 + j16.3$</td>
</tr>
<tr>
<td>X-mas Saucon B1</td>
<td>$7.9 + j9.6$</td>
</tr>
<tr>
<td>X-mas Saucon 400</td>
<td>$50.0 + j5.5$</td>
</tr>
<tr>
<td>Mudd Bldg. Lobby 3</td>
<td>$45.0 + j5.5$</td>
</tr>
<tr>
<td>751 E. Sixth St.</td>
<td>$19.0 + j6.0$</td>
</tr>
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Table 3-1: Measurements of Driving Pt. Impedance
monitor system, and provide a rough idea of the expected value of the driving point impedance, for design purposes.

The results in the table do show a great variation, both in the resistance and inductance of the power lines. However, in all cases, the impedance is observed to be inductive, with a magnitude on the order of tens of ohms. For design purposes, a value of $8 + j18$ ohms will be chosen as the equivalent driving point impedance (at 131kHz).

3.4 SPICE Simulations

Numerous circuit simulations were performed using the spice circuit simulation program, to determine the impedance characteristics of the power line, utilizing the resistance, inductance and capacitance values calculated previously. The model of figure 3-2 was used in the simulations. The value of $R$ accounts for the resistance in both wires (upper and lower).

In the SPICE simulations, $V$ was a single frequency in (131 KHz) sine wave with magnitude equal to unity, and phase angle equal to zero. The computer simulation determined the current through this ideal source, (magnitude and phase), and from this information, a hand calculation was performed to determine the driving point
ONE 3 METER SECTION
(one of twelve)

FOR 3 METERS:
R = 9.378 x 10^{-2}
L = 2.441 x 10^{-6} H
C = 1.189 x 10^{-10} F

Figure 3-2: Power Line Model - Internal Effects Only
impedance.

The first simulation used the model of figure 3-2, with 12 three meter sections. The driving point impedance was determined to be $0.441 - j84.5$ ohms. This is heavily capacitive and is in large disagreement with physical measurements, so other effects must be considered.

The effects of loads connected across the power line were considered next. Equal resistive loads were added at the end of each 3 meter section, yielding the model of figure 3-3, with the termination resistor, $R_T$, in the figure equal to infinity. These loads were varied from large to small values, and the results are plotted in figure 3-4. It can be seen that the impedance approaches the physical measurement values for loads of around 100 ohms. This would imply a total resistive load of approximately 1728 Watts for a 120V system, which is not an unrealistic number.

Next, the termination of the transmission line was varied, first with no loads connected, then with 500 ohm loads at the end of each section. This termination would represent the impedance that the distribution transformer (high voltage to 120 volts) would present at the 120 V terminals. See figure 3-3. The results for no loads are shown in figure 3-5, and the results for 500 ohm loads
Figure 3-3: Power Line Model With External Loads

ONE 3 METER SECTION
(one of twelve)

\[ \begin{align*}
R_L &= \text{LOAD RESISTANCE} \\
R_T &= \text{TERMINATION RESISTANCE}
\end{align*} \]
Figure 3-4: Effects of Varying Loads

- Magnitude of $Z$ ($\Omega$)
- Phase of $Z$ (degrees)
(12 of them) are shown in figure 3-6.

It can be seen that a termination of approximately 0.1 to 10 ohms yields results which are close to the physical measurements. This is in agreement with Shekel [14], who states that "the distribution circuits present impedances considerably lower than 1 ohm to any pair of terminals at 120 Volts." So, a 1 ohm resistive termination will be adopted as a good approximation for the model.

Next, the 1 ohm termination was utilized, and the load resistors were varied. The results are plotted in figure 3-7. It can be seen, that for large variations in the load resistances, the driving point impedance is relatively constant. This would tend to indicate that the termination is a dominant factor in the determination of the driving point impedance. Shekel [14] is not specific as to the nature (capacitive, resistive, inductive) of the 1 ohm termination, so a 1 ohm inductive termination, and a 1 ohm capacitive termination were substituted into the model in place of the 1 ohm resistive termination. The results were similar, yielding a driving point impedance of 5.4 + j23.8 ohms for the inductive termination, and 4.45 + j22.1 ohms for the capacitive termination. These results are approximately equivalent to the resistive termination.
Figure 3-6: Varying Termination With 500 Ohm Loads

- \( \circ \) = Magn. of \( Z \) (\( \Omega \))
- \( \square \) = Phase of \( Z \) (\(^\circ\))
Therefore, the model of figure 3-3 will taken as representative of the power lines, with $R_t = 500$ ohms, and $R = 1$ ohm, which yields a driving point impedance of $5.81 + 172.6$ ohms. This could be modeled as a 5.81 ohm resistor and a 27.5 $\mu$H inductor in series as shown in figure 3-8. This result is in agreement with Lee [11], who also states that the driving point impedance can be modeled as a resistor in series with an inductor, where the resistor can vary from 2 to 30 ohms, and the inductance can vary from 10 $\mu$H to 30 $\mu$H, depending on the environment (industrial, residential, etc.).

3.5 Frequency Selection

According to Ciarcia [3], carrier current schemes have been successfully utilized in the frequency range of 30 KHz to 500 KHz. The model arrived at in the previous section was analyzed using SPICE simulations over this frequency range to determine the driving point impedance, and the attenuation at the termination for the various frequencies. The results are plotted in figures 3-9 and 3-10. It can be seen that there is a basic tradeoff between attenuation along the line, and driving point impedance, since one would desire small attenuation and large driving point impedance. It is noted however that
Figure 3-7: Varying Loads With 1 Ohm Termination

- o = Magn. of Z (Ω)
- □ = Phase of Z (°)
Figure 3-8: Equivalent Driving Pt. Impedance Model
these quantities (attenuation along the line & driving point impedance) do not vary significantly enough with frequency according to this model to support a choice of operating frequency. Thus, other considerations must be used to determine the carrier frequency.

Higher frequencies of operation are argued to have some advantages over lower frequencies. Higher frequencies permit greater isolation from the 120 V, 60 Hz waveform which is present on the power lines. Higher frequencies also allow faster operation because response times of filters and phase-locked loops will be decreased. However, at very high frequencies, the lumped circuit parameter model breaks down, and it is expected that losses along the line will be increased. Also, if too high of an operating frequency is chosen, it is possible that harmonic distortion of the carrier wave could have significant energy in the range of a commercial AM receiver. This could cause interference with radio reception, which should be avoided.

A very common and reliable carrier-current system in use today, the BSR Home Control System [5], [6], [10], [12], utilizes a 121 KHz carrier frequency. Obviously, it is desired to avoid using this frequency in the energy monitor system to prevent interference from any such units. Therefore, a frequency
Figure 3-9: Driving Pt. Impedance vs. Frequency
Figure 3-10: Attenuation vs. Frequency

$\circ = \text{Attenuation in dB (at Termination)}$
of 131 KHz was chosen because it is close to the industry-proven carrier frequency of 121 KHz, yet far enough away to avoid interference. A frequency higher than 121 KHz was chosen to benefit from the previously stated advantages of higher frequencies. The modelling and SPICE simulations indicate that reliable performance can be expected at this chosen frequency of 131 KHz.
4. OUTPUT CIRCUIT OPERATION

4.1 Output Circuit Transfer Function

Carrier signals are coupled to the power lines at both the RMU and the CPM by means of a tuned amplifier - transformer circuit, a model of which is shown in figure 4-1. A small slug tuned IF transformer with a tapped primary is used, to which a tuning capacitor, \( C \), is added across the primary winding (pins 1 to 3). A resistor is added across pins 2 to 3 to limit the Q. The tuned coil is driven by a square wave current source at the desired carrier frequency. The primary circuit operates like an auto-transformer, with a large sinusoidal primary voltage, \( V_p \), generated from a relatively small supply voltage \( V \). This primary voltage is then stepped down via the secondary winding to a low voltage, and relatively high current signal (at the carrier frequency). High secondary current is necessary because of the particularly low value of load impedance that the power line presents. This is why such power-line carrier systems are sometimes referred to as "carrier-current" systems.

It is desired to determine the parameter values (\( V, R, I \), etc.) for a given output voltage, \( V \). The following simplifying assumptions are made:
Figure 4-1: Model of Tuned Amplifier
1) Since the capacitive reactance of $C$ can be tuned out at the carrier frequency with the appropriate choice of $L$, it will be assumed that $C$ and $L$ can be neglected in the analysis, and that $Z$ is directly attached to line pins 4 and 5. The only consequence of this assumption will be that harmonics of the carrier frequency will be attenuated more than the analysis would indicate - which is desirable in any case.

2) The impedance $Z$ will be modelled as a series line resistance and inductance, as this was found to be an accurate model in the analysis of the preceding chapter.

3) All leakage reactances and winding resistance in the transformer model will be neglected. Only the magnetizing inductance of the transformer will be considered, which will be referred to the primary winding.

4) The current source will be assumed to be ideal.

These assumptions yield the model of figure 4-2, with the transformer being ideal, and $L$ representing the magnetizing inductance of the transformer.

At this point, all impedances in the circuit will be referred to the tapped port of the primary winding (pins 2 to 3), which will yield the circuit in figure 4-3.
Figure 4-2: Simplified Model of Tuned Amp
Figure 4-3: Model With Impedances Referred to Primary
The transformation ratios which apply are as follows:

\[ Z_{\text{line}} = \left( \frac{N_3}{N_2} \right)^2 \]  \hspace{1cm} (4.1)

\[ R_{\text{L}} = \left( \frac{N_3}{N_2} \right)^2 \]  \hspace{1cm} (4.2)

\[ L_{\text{L}} = \left( \frac{N_3}{N_2} \right)^2 L_0 \]  \hspace{1cm} (4.3)

\[ C_{\text{T}} = \left( \frac{N_1}{N_2} \right)^2 C_T \]  \hspace{1cm} (4.4)

\[ L_{\text{M}} = \left( \frac{N_2}{N_1} \right)^2 L_M \]  \hspace{1cm} (4.5)

\[ V_0 = \left( \frac{N_3}{N_2} \right) V_{0*} \]  \hspace{1cm} (4.6)
The Fourier transform of the voltage \( v \) is given by

\[
V_0(\omega) = H(\omega) \cdot I_s(\omega)
\]  

(4.7)

\( I_s \) is given by a 50% duty cycle square wave from zero to \( I \), as shown in figure 4-4.

The Fourier series representation of \( I_s \) will be used to find the steady-state component of the output at the fundamental frequency (the carrier frequency). The Fourier series representation of \( I_s \) is as follows:

\[
I_s = \frac{I_p}{2} + \frac{2I_p}{\pi} \sin(\omega_0 t) + \frac{2I_p}{3\pi} \sin(3\omega_0 t) + \frac{2I_p}{5\pi} \sin(5\omega_0 t) + \ldots + \frac{2I_p}{n\pi} \sin(n\omega_0 t)
\]  

(4.8)

where \( \omega_0 = \frac{2\pi}{T} \)
Figure 4-4: Current Source Waveform
The magnitude and phase angle of the transfer function \( H(\omega) \) are as follows: (Prime notation has been dropped for simplicity.)

\[
|H(\omega)| = \frac{\sqrt{\omega^4 + \omega^2 \left( \frac{R_L}{C_T L_T} \right)^2}}{\sqrt{\frac{R_L}{\frac{1}{M C_T L_T}} - \omega^2 \left( \frac{1}{R L} + \frac{R_L}{L_L} \right)} + \left[ \omega \left( \frac{1}{C_T L_L} + \frac{R_L}{C_T R L_L} + \frac{1}{L M C_T} \right)^2 \right]^{\frac{1}{2}}}
\]

\[
\phi(\omega) = \tan^{-1}\left( \frac{R_L}{\omega L} \right) - \tan^{-1}\left[ \frac{\omega \left( \frac{1}{C_T L_L} + \frac{R_L}{C_T R L_L} + \frac{1}{L M C_T} \right) - \omega^3}{\omega \left( \frac{1}{R L} + \frac{R_L}{L_L} \right)} \right]
\]
And, using the transformation ratios stated earlier, all impedances will be transformed back to the positions shown in figure 4-2. The equations (4.9) and (4.10) now become:

\[
\begin{align*}
|H(\omega)| &= \sqrt{\frac{\omega^4}{C_T^2} \left(\frac{N_2}{N_1}\right)^4 + \frac{\omega^2}{C_T^2} \left(\frac{N_2}{N_1}\right)^2 \frac{R_L}{L_L}} \\
&\sqrt{\frac{R_L}{L_L} \frac{1}{\omega^2 C_T^2} - \omega^2 \left(\frac{1}{R C_T} \left(\frac{N_2}{N_1}\right)^2 + \frac{R_L}{L_L}\right)^2 + \left[\omega \left(\frac{1}{R C_T} \left(\frac{N_2}{N_1}\right)^2 + \frac{R_L}{L_L} \frac{1}{R C_T} \left(\frac{N_2}{N_1}\right)^2 + \frac{1}{L_L} \right) - \omega^3\right]^2}
\end{align*}
\]  

(4.11)

\[
\phi(\omega) = \tan^{-1} \left(\frac{R_L}{\omega L}\right) - \tan^{-1} \left[\frac{\omega \left(\frac{1}{R C_T} \left(\frac{N_2}{N_1}\right)^2 + \frac{R_L}{L_L} \frac{1}{R C_T} \left(\frac{N_2}{N_1}\right)^2 + \frac{1}{L_L} \right) - \omega^3}{\frac{R_L}{L_L} \frac{1}{\omega^2 C_T^2} - \omega^2 \left(\frac{1}{R C_T} \left(\frac{N_2}{N_1}\right)^2 + \frac{R_L}{L_L}\right)}\right]
\]  

(4.12)

Therefore, if the proper values of the components are given, one can calculate the carrier voltage waveform which will appear on the power lines.
4.2 Theoretical Output Voltage

For the output circuit on the RMU, the components have the following values:

\[ M_1 = 154 \text{ Turns} \]
\[ M_2 = 9 \text{ Turns} \]
\[ M_3 = 4 \text{ Turns} \]
\[ L = 738 \mu \text{H} \]
\[ C = 0.002 \mu \text{F} \]
\[ R = 1 \text{ K}\Omega \]

and from chapter 3, "typical" values for \( R \) and \( L \) are:

\[ R = 8 \Omega \]
\[ L = 18 \mu \text{H} \]

However, on the RMU, an inductance was not used to tune out the effects of \( C \) as shown in figure 4-1. Therefore, in order to calculate the expected output voltage, the capacitor \( C \) and inductance \( L \) will be lumped together (for 131 KHz) which reduces the effective inductance of the power line to 11.3 \( \mu \text{H} \). This new value will be used for \( L \) in the equations, as an approximation.
Since $I = 84.8 \text{ mA}$ for the RMU (see section 5.6), the fundamental component of $I$ is the following value:

$$I_s = 54.0 \sin(\omega t) \text{ mA}$$

which, through the use of equations (4.11) and (4.7), yields a theoretical output voltage of $1.09 \text{ V}$ peak.
5. REMOTE MEASURING UNIT

5.1 Overall function

The remote measuring unit (RMU) is one of the two basic parts of the energy monitoring system. A block diagram of the RMU is shown in figure 5-1, and a photograph of the developed RMU is shown in figure 5-2.

The RMU is configured for four pairs of voltage-current inputs. One such pair is shown as V and I in the figure. I would be a measure of the total current drawn from the source of voltage, V. Each pair of inputs is selected, one pair at a time, to be input to the multiplier, which linearly multiplies the current and voltage waveforms together. A sequence is followed whereby each pair of inputs is sampled approximately every 14 seconds via the input selector as shown. This is not a continuous measure of power, however for the predominantly residential application being considered (apartment buildings, etc.), it is assumed that the loads do not change too drastically within the 14 second period, also, any small variations will average out over the long run.

The analog product of the multiplication is converted to digital form and added to the data register. In this way, the data register holds the sum of the power.
Figure 5-1: Block Diagram - RMU
Figure 5-2: Photograph of RMU
computed for each pair of voltage-current inputs, and is increased each time a new pair of inputs is selected. The summing of these power measurements takes place over time, and is therefore analogous to the time integral of power consumption, which yields total energy consumption. The data register therefore holds a measure of the total energy consumed from the four possible sources of power in the apartment.

This energy information is held in the data register until the RMU is instructed by the CRU to report this information. The determination of when the RMU should report entails two processes: 1) receipt of the report cycle initiation waveform, and 2) an up-count to determine the proper output frame for this particular RMU.

As mentioned previously in Chapter 2, when the CRU desires to initiate the report cycle, it sends out a special on-off modulated 134 KHz signal on the power lines. At the RMU, any carrier signals on the power lines are band-pass filtered \( f = 134 \text{ KHz} \), and multiplied by a 131 KHz signal generated on the RMU; thus creating sum and difference frequencies. If the carrier signal is exactly 134 KHz, the difference frequency of 3 KHz will be detected, and if this 3-KHz signal is 2 seconds long (within a small tolerance), the report cycle
Initiation waveform has been received by the RMU. This process is configured as such to prevent the possibility of any spurious carrier signals which may happen to be on the power lines (e.g., from BSR Home Control Units) from creating a false detection of the report cycle. The safe-guard is twofold. The carrier signal must be exactly 134 KHz, and it must be exactly two seconds in duration in order for the RMU to recognize it. It is reasoned that this is a unique enough set of circumstances, so that false detection of the report cycle will not occur in practice.

It should be reiterated here that even if the RMU for some reason "misses" the report cycle one day, because it does not detect the report cycle initiation waveform sent by the CRU, the energy data will remain intact and be reported in the the next day’s report cycle. However, a false detection of the report cycle would be disastrous, as all energy data would be lost after the RMU falsely reports (at some time when the CRU is not receiving).

Upon detection of the report cycle, the RMU starts to count output frames, until it reaches the specific number which is set for that RMU. When this occurs, the output circuitry is enabled, further inputs to the data register are disabled, and a parallel to serial
conversion of the energy data stored in the data register is performed. This serial data is then used to on-off modulate the 131 KHz carrier signal which is superimposed on the power lines. In this way, a serial sequence of digital data is produced on the power lines by means of the presence or absence of the 131 KHz signal.

At the end of this RMU's output frame, the output circuitry is disabled, the data register is reset to zero, the output frame counter is reset, and inputs to the data register are once again enabled. And, the process of accumulating power data is started all over again. The specific details of the various sections of the RMU are described below.

5.2 Power Supply, Battery Back-up, and Power Failure Considerations

The power supply for the RMU is shown in figure 5-3. The D.C. supply voltages necessary are +12 V, -12 V, and +5 V, all derived from a 120 V, 60 Hz line. The RMU design uses almost entirely CMOS circuitry, so relatively low-power supplies are sufficient. The supplies were designed for 200 mA outputs (at 12 V). The two transformers used produce secondary voltages of 12.6 VRMS, at rated current of 300 mA, when their primaries are connected to 115 VRMS.
Figure 5-3: Power Supply & Reset Circuitry - RMU
For the 12 V supplies, a standard 4-diode full-wave rectifier bridge is used, and the 1470 μF capacitance reduces the peak to peak ripple to approximately 1.1 Volts at the input to each regulator. The regulator reduces this to approximately 0.28 mV peak to peak.

The +5 V supply is obtained by regulating down the +12 V supply as shown. All logic and registers on the RMU (the vast majority of IC's) are powered between +12 V and ground. The -12 V supply is used for a small number of op-amps, and the +5 V supply is used in only two places, a tone detector and a D-A converter chip.

A battery back-up supply, V_{BB}, is necessary to retain the information in the energy data register, and insure the proper operation of the reset circuitry in the event of a power failure, in which case the +12 V, -12 V, and +5 V supplies would be lost.

The battery back-up supply is shown in figure 5-3, and is provided by three 1.2 V lithium cells which are trickle charged from the +12 V supply with a current of 0.215 mA. Lithium batteries in this configuration have an almost indefinite useful life—in excess of ten years. V_{BB} is used to power only two chips, and under normal conditions, is slightly less than +12 V. It can be seen from the figure, that when the +12 V supply is not present due to a power failure, D1 is back-biased and V_{BB}. 

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becomes approximately 3 V, which is enough to power the two CMOS chips which need to be powered during a power failure (data register & reset logic).

The reset circuitry is shown in figure 5-3. Under normal operating conditions, it is necessary to reset the data register and to reset and disable the output frame counter at the end of the RMU’s output frame. If a power failure occurs, it is necessary to reset and disable the output frame counter when power is restored, as it might have come up in an enabled state which would mean a false output frame would be generated - causing the energy data to be lost. However, it is necessary to insure that the energy data register is not reset when power is restored, otherwise this data could be lost if no safeguards were made. Two separate RESET lines are therefore provided, RESET1 to reset and disable the output frame counter, and RESET2 to reset the energy data register.

When power has been up for a long period of time, capacitor C2 is fully charged, and both RESET1 and RESET2 provide a short, positive-going pulse at the end of the RMU’s output frame, as a result of differentiating the signal OUTPUT FRAME.

When a power failure occurs, gates A, B, C, and D remain active because they are powered from the backed-up supply Vc. This is the reason for using all NAND gates BB.
in this circuit, so that only 1 IC package need be powered by $V$ to perform the resetting functions. When $B8$ +12 $V$ is lost, the output of gate C goes to a logic high, and capacitor C2 is discharged rapidly through Q1. This prevents any signals from propagating through gate C, maintaining RESET2 in a low state. It is necessary to discharge C2 rapidly in the event that power goes down only momentarily. When power is restored, the output of gate B makes a low to high transition, which provides a short pulse which propagates through gate E regardless of the state of gate E's other input, thereby causing RESET1 to occur as desired.

Capacitor C2 has a long time constant for charging, as it must charge through a 1 $M\Omega$ resistor. This maintains gate C in a disabled condition and does not allow the pulse produced by the rising signal OUTPUT-FRAME to propagate through, which retains RESET2 in a low state. The time constant $R2 \cdot C2$ is sufficiently long to allow all other transients in the circuit associated with power-up to die before the voltage across C2 becomes a logic high. When C2 becomes charged to a logic high, gate C is enabled, and normal reset operation is restored.
5.3 Clocks and Timing

The circuitry which generates all clock signals used by the RMU is shown in figure 5-4. The seven different frequencies necessary for the RMU's operation are as follows: 131.072 KHz, 512 Hz, 60 Hz, 7.5 Hz, 0.9375 Hz, 0.46875 Hz, and 0.09375 Hz. These frequencies are derived from two sources, a 2.097152 MHz crystal oscillator, and the 60 Hz power line. The 131 KHz frequency mentioned previous to this is actually 131.072 KHz as listed here. This is due to the fact that a 2.097152 MHz crystal is the closest value to 2.096000 MHz, which would be required to generate exactly 131 KHz. Any references to 131 KHz throughout this paper will be understood to be actually 131.072 KHz.

The frequencies derived from the crystal are 131.072 KHz and 512 Hz. These are obtained by binary division of the 2.097152 MHz reference, using a 12 bit binary counter. The 131.072 KHz frequency is used as the output carrier frequency and in the detection of the report cycle initiation waveform. The 512 Hz signal is used in the analog to digital conversion of the power data. These two frequencies perform functions that are independent of the other frequencies (60 Hz and below) and so all frequencies need not be derived from the same reference.
Figure 5-4: Clock Generation - RMU
The frequencies of 60 Hz and below are derived directly from the 60 Hz power line. The 120 V waveform is divided down by a resistive divider and then sent to a comparator which yields a 0 V to +12 V square wave at 60 Hz. This is then divided by 8, 64, 128, and 640 to yield 7.5 Hz, 0.9375 Hz, 0.46875 Hz, and 0.09375 Hz respectively. A binary counter is used to perform the divisions by multiples of 2, and a decade counter is used to perform a division by 10.

These 60 Hz derived signals perform functions relating to the counting of output frames and the clocking of data within the output frames. A tremendous benefit is obtained by deriving these frequencies from the 60 Hz power line. In order to maintain synchronism of the entire system (e.g., 500 RMU's and 1 CRU), it must be ensured that all units count output frames and clock output data at the same rate. This could be done with a precision crystal oscillator on each RMU, however even slight differences or drifts between the crystal frequencies of different RMU's would be integrated over the time it takes for all RMU's to report their energy data (one complete report cycle). And if a report cycle took a few hours, which it might do in practice, then the error could be enough to cause a loss of synchronism within the system. That is, the output frames of two
RMU's could overlap, causing them to report data at the same time, which would be unintelligible to the CRU. In addition, the CRU could lose track of the proper time to clock in (accept) the data bits which the RMU's are sending in a serial stream.

What is needed is a way of making all the units (RMU's and CRU) count output frames at exactly the same rate, that is, have the same reference. This is what the 60 Hz power lines provide. All units receive exactly the same 60 Hz signal through the power lines, with the possible exception of a slight phase shift due to different phases of a 3-phase power system, but this phase shift does not affect the frequency of the signal. (This phase shift does have certain implications in the detection circuitry, which will be discussed in section 6.3.7.) Thus, all units will perform the tasks associated with counting output frames and output data at exactly the same rate, even if the 60 Hz frequency of the power lines deviates by even a large amount.

All of the clock frequencies mentioned above are used throughout the RMU for the general purposes noted. Their specific functions will be described in detail in the description of the individual circuit sections.
5.4 Multiplier Section

The function of the multiplier section is to take the voltage and current readings, one pair at a time, multiply the voltage and current waveforms together, and to provide an analog measure of the power being consumed to the A-D conversion circuitry. The input portion of the circuit is shown in figure 5-5. Since the RMU was designed to handle up to four pairs of voltage - current inputs, four voltage dividers and four current transformers are needed (only one of each is shown). The voltage dividers scale the 120 V voltage waveform to +/- 6 V peak. The current transformer secondary is terminated in a resistance and configured to yield at maximum load, a +/- 3 V peak signal. The specific current transformer selection was not performed as a part of this design, as this would be dependent on the particular application.

These scaled voltage and current waveforms are then selected, one pair at a time, to be input to the multiplier. That is, V and I are selected together, then V and I, etc. CMOS analog switches are used for the selection process, along with a circuit which controls the opening and closing of the switches. After passing through the switch, the voltage waveform is low-pass filtered (f ~ 13 KHz) and buffered with a unity c
Figure 5-5: V & I Inputs - RMU
gain stage, then sent to the x-input of the multiplier.

The current waveform, after passing through the switch, is amplified by a factor of 2, low-pass filtered (f ~ 16 KHz), then a.c. coupled and unity gain buffered to the y-input of the multiplier.

The circuit which controls the closing of the CMOS switches is shown in figure 5-6. This circuit generates the sequence shown in figure 5-7. The switches for the voltage waveform V and current waveform I are closed for 2.133 seconds during the "GATE A" portion of the cycle. Half-way into this period of time (or 1.067 seconds after GATE A goes high), the line labeled COUNT becomes a logic high. It is while COUNT is high that the actual A-D conversion of the result of the multiplication takes place. The first 1.067 seconds of GATE A are provided to allow the output of the multiplier to settle. When GATE A goes low, the switches for V and I are opened, and a line labeled NULL becomes a logic high. During the period of time that NULL is high, the output of the multiplier is nulled back to zero volts, and the offsets of the multiplier are automatically compensated for. This will be explained in greater detail further down in this section. When NULL goes low, GATE B goes high, and the switches for V and I are closed, and the cycle continues as with GATE A.
Figure 5-6: Input Selector - RMU
Figure 5-7: Timing Diagram for Input Selector
Thus, the sequence is: Close the two "A" switches, wait 1 second for the multiplier output to settle, make an A-D conversion, open the two "A" switches, null the output of the multiplier to zero, close the two "B" switches, and so on.

One of the NULL periods is twice as long as the other three. There is no technical reason for this, except that it simplifies the circuitry necessary to generate these waveforms. This does not deteriorate the performance of the circuit in any way. The waveforms of figure 5-7 are generated using a Johnson decade counter and some external logic. Basically, an extra stage was added to the counter, and the counter is clocked at a 0.9375 Hz rate up to 12 and then reset to zero.

The actual multiplier and nulling circuits are shown in figure 5-8. It has been shown by Tsuda [16], that regardless of the distortion in the current waveform of a 60 Hz power system, average power is equivalent to the D.C. component of the instantaneous power, and furthermore this D.C. component depends only on the voltage waveform and the 60 Hz component of the current waveform. Thus, in the circuit shown, instantaneous power is obtained from the linear multiplication of the voltage and current waveforms, and the D.C. component is extracted with a low-pass filter. The XR-2208 multiplier
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Figure 5-8: Multiplier Circuit - RMU
is used, which includes an internal op-amp which is used to amplify the differential output of the multiplier and provide a single-ended output.

The multiplier is configured to produce a 10 V D.C. output \( V_{DC} \) when both \( v \) and \( v \) are equal to the maximum DC \( \pm 6 \) V peak sine waves. The D.C. voltage at \( V_1 \) is given by:

\[
V_1(D.C.) = (0.2386) \cdot v \cdot v
\]

This voltage is then multiplied further by a factor of 1.2 in the nulling circuit.

Low pass filtering is accomplished with the 22\( \mu \)F and the 0.15\( \mu \)F capacitors, yielding a cutoff frequency of 0.45 Hz.

The nulling circuit serves two functions: to drive the voltage \( V \) back to zero between multiplications, and to cancel out the effects of any offsets the multiplier circuitry might have. The nulling process occurs each time the NULL line goes high. When this happens, the inputs to the multiplier circuitry are grounded through the appropriate source impedance via the closing of the two switches controlled by the NULL level in figure 5-5. This would cause a certain offset voltage to appear at the output (pin 11) of the XR-2208, which will be called \( V_{os} \). Also, the switch in figure 5-8 controlled by the NULL level closes, and any voltage appearing at \( V \) is multiplied by the open loop gain \( (A_{o}) \) of amplifier A2,
and fed back to A1, thus driving the output, $V_{\text{DC}}$, to approximately zero volts. The voltage necessary to do this is stored on capacitor $C_1$. Then when the nulling period is over, the NULL switches are opened, and the voltage on $C_1$ is summed with the output of the multiplier, automatically cancelling its offset. The discharge time of $C_1$ is very long due to the almost infinite impedance presented by the non-inverting input of A2 and the open switch. The above results are shown mathematically, using the model in figure 5-9, where each op-amp has an open loop gain $A_0$, A1 has an offset voltage $V_{o1}$, A2 has an offset voltage $V_{o2}$, and the output of the multiplier has an offset $V_{os}$, and where $V$ represents the true result of a multiplication.

When the switch has been closed for a "long" time, the output voltage is given by:

$$V_o = \frac{-K_3 V_{os} + K_2 A_0 V_{o1} + K_2 A_0 V_{o2}}{1 + K_1 K_2 A_0} \quad (5.1)$$
Figure 5-9: Nulling Circuit Model
and the capacitor voltage:

\[ V_c = \frac{A_0 K_1 K_3 V_{os} + -K_1 K_2 A_0 V_{o1} + A_0 V_{o2}}{1 + K_1 K_2 A_0} \quad (5.2) \]

where:

\[ K_1 = \frac{R_4}{R_3 + R_4}, \quad K_2 = \frac{R_1 + R_2}{R_1}, \quad K_3 = \frac{R_2}{R_1} \]

Then, when the switch is opened:

\[ V_o = \frac{K_2 V_{o1} + K_2 A_0 V_{o2} - K_3 V_{os}}{1 + K_1 K_2 A_0} - K_3 V \quad (5.3) \]

Substituting in the given resistor values and using the fact that \( A_0 \gg 1 \):

\[ V_o = \frac{V_{o1}}{A_0} + 1.3 V_{o2} - \frac{V_{os}}{A_0} = 1.2 V \quad (5.4) \]

It can be seen that the original intent of eliminating the offset \( V_{os} \) has been accomplished as it is divided by \( A_0 \), however, the offset of \( A_2, V_{o2} \), has been amplified slightly. For this reason, a relatively low
offset op-amp must be used for \( A2 \). The LF412 has a typical input offset voltage of \( 1 \) mV, which is sufficiently smaller than the offset of the multiplier, \( V_{os} \), which is expected to be in the tens of millivolts.

It is expected that the output voltage, \( V \), will drift slowly due to the fact that the leakage current of the open switch, and bias current and input impedance of the op-amp \( A1 \), will tend to discharge capacitor \( C1 \). The LF412 has an input bias current spec. of 50 pA typical, and an input impedance of 10 ohms. The DG308 has an "off" leakage current spec. of 100 pA. It is observed that the leakage current of the analog switch (DG308) and the bias current of the LF412 will dominate, and a drift rate of \((-\frac{I}{C}) = -1.5 \) mV/sec would be predicted. This is consistent with an observed drift rate of \(-1.67 \) mV/sec.

The stability of the nulling circuit is insured by the compensation network of \( R6 \) and \( C2 \). Without \( R6 \) and \( C2 \), the Nulling circuit is inherently unstable, which can be observed in figure 5-10. This figure presents the Bode plots of the loop gain of the nulling circuit (figure 5-9) for the uncompensated case. The phase characteristics of the LF412, taken from the specification sheets, are incorporated into these plots. In the uncompensated case, the magnitude of the loop gain is still greater than unity when the phase of the loop
Figure 5-10: Uncompensated Loop Gain of Nulling Circuit
Figure 5-11: Compensated Loop Gain of Nulling Circuit
gain reaches 180 degrees. This indicates an unstable circuit. The addition of R6 and C2 is a type of phase-lag compensation, which adds one low frequency pole and one higher frequency zero to the transfer function of the loop gain. The low frequency pole has the effect of attenuating the loop gain, causing the magnitude of the loop gain to pass through unity at a lower frequency than in the uncompensated case, where there is greater phase margin. It can be seen from Figure 5-11 that for the compensated circuit, there is 25 degrees of phase margin when the magnitude of the loop gain passes through unity. This indicates a stable circuit.

The output of the nulling circuit \( V_{\text{DC}} \) becomes the input to the A-D conversion circuitry, which is described in the next section.

5.5 A-D Conversion and Accumulation Circuitry

The output voltage of the previous section, \( V_{\text{DC}} \), becomes the input to the A-D conversion circuitry shown in Figure 5-12. The circuit uses a digital to analog converter (DAC 0808), a binary counter, and a 512 Hz clock to convert the D.C. input voltage into digital form.

The DAC 0808 sinks current into pin 4 proportional to the 8 bit digital word presented at its input. The
Figure 5-12:  A-D Conversion Circuit - RMU
maximum sink current is determined by the current supplied to pin 14. This current is produced by connecting pin 14 to an LM 329 precision 6.9 V reference through a 2.2 KΩ resistor and a 1 KΩ potentiometer. The pot is trimmed to yield 2.5 mA into pin 14.

The D.C. voltage from the multiplier circuitry is connected to the output terminal (pin 4) through a resistor, and the voltage at the output (pin 4), drives a comparator. When the output current (current into pin 4) is smaller than \( V \) /\( R_1 \), the voltage at pin 4 is greater than zero and the output of the comparator is zero volts. When the output current is large enough to equal \( V \) /\( R_1 \), the voltage at pin 4 reaches zero volts, and the comparator switches to a high state. A clamp diode is used at the output terminal to sink the current left over after the output (pin 4) sinks the amount of current proportional to the present digital word, and also to prevent the voltage at pin 4 from exceeding ~ 0.5 V, as recommended by the manufacturer.

The analog to digital conversion process works as follows. When COUNT goes high, a 512 Hz clock is enabled, which is applied to the 4040 binary counter. The output of this counter becomes the input to the DAC 0808. Since the counter starts at zero, the output current of the DAC 0808 (current into pin 4) will start
at zero and increase monotonically with time, due to the
512 Hz clock which is incrementing the counter. When the
output current is sufficiently large to cause a voltage
drop of \( V \) across \( R_1 \), the comparator switches high,
which resets the counter and disables the 512 Hz clock.
The number of clock pulses that the counter received up
to that point becomes the digital measure of power
consumption, and is input to the accumulator circuitry
shown in figure 5-13.

The allowable range of \( V \) is from 0 to +10 V, with
+10 V corresponding to the maximum power consumption.
This 10 V range is converted to an 8 bit digital word, or
256 possible levels, yielding a weight of 39 mV per bit.

There is a safety feature included which resets the
counter and stops the conversion if the count goes to the
allowable maximum of 256 without triggering the
comparator. This safety feature is provided by the OR
gate in figure 5-8, which automatically resets the
counter and disables the 512 Hz clock at a count of 256.
This insures that no more than the full scale power can
be added to the data register in any one A-D conversion.
The maximum amount of time it takes to convert the
maximum input voltage \( (V = +10 \text{ V}) \) is \( 256/(512 \text{ Hz}) \) or
0.5 seconds. This is well within the 1.067 second period
that the COUNT level stays high.
Figure 5-13: Energy Data Accumulator
The DAC 0808 is guaranteed to be accurate to +/- 1/2 of one least significant bit, and the entire conversion scheme was tested to verify that this accuracy could be preserved. The results of this test are shown in table 5-1. The table shows that the accuracy is indeed preserved, as all outputs matched the expected results, with the exception of a few cases, which were in all cases just 1 LSB larger than the expected value, indicating an accuracy of +/- 1/2 LSB.

The number of clock pulses that the counter in the A-D conversion scheme receives, becomes the clock for another counter, as shown in figure 5-13. This is the energy data register, as referred to earlier, and serves the purpose of accumulating all the power data over time. The register is composed of two cascaded 4040 12-bit binary counters, so that the 11th bit of the first 4040 becomes the clock of the second 4040. The input clock to the register is disabled under two conditions: 1) when this RMU's output frame occurs, and it is transmitting data to the CRU, which prevents the data word from changing while it is being sent, and 2) when the register is almost full, so as to prevent the register from "rolling over", causing a loss of information. The first case results in a negligible error in the energy measurement for two reasons. First, the report cycle
<table>
<thead>
<tr>
<th>Input Voltage (Vdc)</th>
<th>Theoretical Counts</th>
<th>Actual Counts</th>
</tr>
</thead>
<tbody>
<tr>
<td>11.00</td>
<td>256</td>
<td>256</td>
</tr>
<tr>
<td>10.00</td>
<td>256</td>
<td>256</td>
</tr>
<tr>
<td>9.06</td>
<td>232</td>
<td>233</td>
</tr>
<tr>
<td>8.07</td>
<td>207</td>
<td>207</td>
</tr>
<tr>
<td>7.09</td>
<td>182</td>
<td>182</td>
</tr>
<tr>
<td>6.09</td>
<td>156</td>
<td>157</td>
</tr>
<tr>
<td>5.03</td>
<td>129</td>
<td>129</td>
</tr>
<tr>
<td>4.10</td>
<td>105</td>
<td>106</td>
</tr>
<tr>
<td>3.08</td>
<td>79</td>
<td>80</td>
</tr>
<tr>
<td>2.08</td>
<td>54</td>
<td>54</td>
</tr>
<tr>
<td>1.06</td>
<td>28</td>
<td>28</td>
</tr>
<tr>
<td>0.950</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>0.695</td>
<td>18</td>
<td>19</td>
</tr>
<tr>
<td>0.0656</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>0.0341</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>0.0001</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 5-1: Results of A-D Conversion Test
will occur in the early hours of the morning when a minimum amount of power is normally being consumed, as compared to the rest of the day. And second, the output frame lasts only 10,667 seconds, which is only 0.012% of a 24 hour day.

The second case (the register almost full) will rarely occur in practice, since the register is designed to hold approximately 3 days worth of power data. The absolute maximum number of clock pulses on the data register, which could occur in one day, is 6,380,308 which is 256 times the number of COUNT cycles in 24 hours. The cascaded pair of 4040's can count up to 16,711,680 before disabling itself, yielding 2.6 days total storage capacity at maximum energy use. It is expected that the average energy consumption will be considerably less than the absolute maximum, (perhaps half as much), in which case the data register could hold data for many more days.

The data registers are protected against losing their data during a power failure by the battery back-up supply (V) which powers both 4040's. The 1MΩ resistors are connected to the outputs of the 4040 to limit the current which flows into unprotected chips (those not powered by V), during a power failure. The second 4040 is also protected against a reset at power
up, while the first 4040 is never reset.

The information stored in the second 4040 is the only information reported to the CRU during the output frame. At the end of the output frame, this 4040 is reset to zero, however the first 4040 is not reset. No error is introduced here, except for a small lag caused by the fact that the information on the first 4040 will not be reported until it rolls over into the second 4040. One consideration in the design is the ability to accurately determine a tenant's energy consumption up to the day he moves. Even if the energy data register is read (by the CRU) the day the tenant leaves, the data in the LO register is never recorded, so there is a small error introduced. But the maximum count which could be on the LO register is 2047, and when compared to a month's energy use at 60% of maximum, for example, 2047 represents only 0.0018 percent of the total energy count for the month. This would mean a billing error of less than 18 cents would occur for an electric bill of 100 dollars. Thus, in order to simplify the circuitry involved, and to shorten the report cycle, only the data on the HI register is reported to the CRU. The slight error mentioned above only occurs for the case of moving tenants, and will occur so infrequently and is so small, that it may be neglected.
As for the reporting, the 12 bits of the HI register are input, along with 4 preamble bits, to a parallel in - serial out shift register (two 4021 PISO's cascaded). The preamble is created by logically interpreting the state of a "tamper switch". If the distribution panel is opened, or tampered with, a small mechanical tamper switch will open, and the 4 bit preamble will be set to 1001, otherwise it will remain at 0110 indicating an untampered-with unit. In this way, the CRU can detect if all RMU's are operating properly by looking at the preamble. If the preamble is anything other than 0110, the CRU knows that a tenant has probably attempted to remove a current transformer (or in some other way defeat the system), and that RMU will be pinpointed for maintenance.

At each rising edge of the 0.46875 Hz clock, the 16 bits (12 energy data bits from the HI register, plus 4 preamble bits) are parallel loaded into the shift register, then serially clocked out at a 7.5 Hz rate; preamble first, then energy data MSB to LSB. These clocked-out bits are input to the circuitry which generates the output carrier signal. The parallel loading and serial shifting occurs at all times, however the output circuitry is only enabled during the output frame of the RMU, so the 16 bits generate a carrier
signal only during the actual output frame of the particular RMU.

The 16 bit data word is repeated 5 times during the output frame making a total of 80 bits. This is done to provide redundancy in the data transmission, allowing the CRU to correct small errors which might occur by taking a majority vote of the five 16 bit data words which it receives. This procedure will be able to correct errors in any bit position as long as the error occurs less than 3 times; thus the scheme can tolerate up to 32 errors in an 80 bit transmission. It is expected that the data link will be very reliable, however, and that less than 1 error per 80 bits will be encountered.

The timing diagram for the clocking of the data bits during the output frame of the RMU is shown in figure 5-14. These data bits are sent to the output circuitry which is described in the next section.

5.6 Output Circuitry and Output Frame Generation

The output circuit is shown in figure 5-15. The circuit has three inputs, XMIT ENABLE (from output frame generator), 131 KHz clock (from the crystal oscillator), and the output data bits (from the data register). If either the output bit or XMIT ENABLE is at a logic low, the 131 KHz signal cannot propagate through to produce a
Figure 5-14: Output Timing - RMU
carrier signal. When XMIT ENABLE is high, the 131 KHz signal will propagate through for data bits equal to "1", and will not propagate through for data bits equal to "0".

The two transistors act as a current source, which periodically drives the tuned transformer circuit, the operation of which was described in Chapter 3. When the output of the NAND gate is low, the current source is turned on. For an output bit of "1", the current source would be turned on and off at a 131 KHz rate. The diode in the emitter of Q1 is to insure that Q1 is cutoff when the output of the NAND gate is a logic high (~ 12 V). The value of the current source is given by:

\[ I_s = \beta_1 \cdot \beta_2 \cdot \frac{12 - 2 V_{BE}}{R_1} \]  

(5.5)

Using the values of \( \beta_1 = 160 \), for the 2N4126, and \( \beta_2 = 80 \), for the MJE182, along with \( R_1 = 1.6 \) M-ohms; this yields \( I_s = 84.8 \) mA. This would yield a theoretical output voltage of 1.08 V peak, using equations (4.11) and (4.7) of Chapter 4. The output voltage (V1, in figure 5-15) was observed to be typically 1.25 V peak, which is in close agreement with the expected value.
Figure 5-15: Output Circuit - RMU
The secondary of the transformer is connected to the 120 VAC lines through a .22 F capacitor, which serves to block most of the 120 V, 60 Hz signal, while allowing the 131 KHz carrier to pass through. In practice, the reactance that the capacitor presents to the carrier signal could be tuned out with an inductance, which would cause series resonance at 131 KHz.

The signal XMIT ENABLE is generated by the circuit in figure 5-16. This "output frame counter" uses three 4017 Johnson decade counters in cascade. These counters only provide a high output during their respective time slot (i.e., Q5 is only high during the period of every 5th clock). When in cascade, the first counter acts as the ones place, the second as the tens place, and the third as the hundreds place of a decimal number ranging from 0 to 999. One unique number is chosen for each RMU, and set by dialing the thumbwheel switches to the correct positions. For example, an RMU with S1 set to Q4, S2 set to Q6, and S3 set to Q2, on their respective counters, would mean that this would be RMU number 264.

The counter is initially reset to zero, and when the RMU receives the report cycle initiation waveform, the signal SYSTEM SYNC makes a "0" to "1" transition, which sets the signal REPORT CYCLE to a logic high. This enables the clock to the output frame counter, and starts
Figure 5-16: Output Frame Counter - RMU
to clock the counter at a 0.09375 Hz rate. When the count reaches the preset number on the thumbwheel switches, the output of the NAND gate, which is normally high, goes to a low state, indicating that it is this RMU's turn to output data to the CRU. So the unit set to 264 would report during the 264th output frame. The flip-flop used to generate XMIT ENABLE is used to invert the output of the NAND gate to an active high signal, and also to force the positive transition of XMIT ENABLE to occur simultaneously with the positive transition of the 512 Hz clock, which disables the energy data register clock at the proper time so as to prevent extra counts from being added to the data register.

Since the output frame counter is clocked at a 0.09375 Hz rate, each output frame is 10.667 seconds in duration. At the end of the RMU's output frame, the output of the NAND gate makes a "0" to "1" transition, which is differentiated, and becomes the reset pulse for the energy data register and the output frame counter (RESET1 and RESET2).

It should be noted that even if power goes down during a report cycle, while an RMU is reporting, the energy data in the register will be preserved (to be read again when power comes up), since the energy data register is not reset until the end of the output frame.
The circuit which determines when to start counting output frames by interpreting the report cycle initiation waveform and producing the signal SYSTEM SYNC, is described in the next section.

5.7 Report Cycle Detection Circuitry

The circuit in figures 5-17 and 5-18 is used to detect when the CRU has sent the report cycle initiation waveform, and inform the other circuitry in the RMU of this fact by producing the signal SYSTEM SYNC.

The input to the circuit of figure 5-17 is provided by tapping the primary of the output transformer. This would ideally act as a 38:1 step-up transformer for carrier signals on the power lines. (refer to figure 5-15). The input impedance of the circuit of figure 5-17 is at least 94 kΩ, which prevents loading of the transformer circuit. A test was performed on the output circuitry to determine the effects of a resistance connected in parallel with the primary of the transformer, when the secondary is driven with a 134 KHz signal. It was found that a resistance of 94 kΩ caused an attenuation of only 8% when compared to the signal at the primary when unloaded. Which therefore yields an actual step-up ratio of ~ 35:1.

A "soft" limiter is then used to limit the carrier
Figure 5-17: Report Cycle Detection Circuit - Part A
Figure 5-18: Report Cycle Detection Circuit - Part B
signal input to the differential amplifier A1 to about 1.4 V peak at maximum. The signal is then band-pass filtered at 134 KHz, amplified by a factor of 9.5, high pass filtered by A2, and input to a Plessey SL6270C, which is an automatic gain control circuit.

Since the strength of the 134 KHz carrier signal that the RMU will receive is unknown, this AGC is included to provide a constant amplitude sine-wave input to the remaining part of the circuit, regardless of the strength of the 134 KHz signal. It was explained previously that the 134 KHz signal of the report cycle initiation waveform has a special configuration, that is, "on" for 1 second, "off" for 1/4 second, and "on" for 2 seconds. The first 1 second "on" burst of 134 KHz is used to set the gain of the AGC to the appropriate value by effectively "sampling" the strength of the 134 KHz carrier signal that a particular RMU receives.

The AGC provides a constant 90 mV RMS (typical) output for input signals greater than approximately 1 mV. The attack and decay of the gain is set by C1 and R1, and the values shown in figure 5-6 yield an attack time of 0.4 seconds and a decay of approximately 40 dB/sec. Thus, during the first 1 second "on" period of the report cycle initiation waveform, the AGC will adjust its gain (down from the maximum) to an appropriate value to yield
90 mv RMS at its output. Then, during the 1/4 second "off" period, the gain of the AGC will slowly increase by about 10 db (a factor of 3). When the 2 second "on" portion of the report cycle initiation waveform occurs, the gain will be essentially at the correct value and the AGC will adjust itself (within ~ 0.4 seconds) to the correct value. This way, the integrity of the 2 second portion of the report cycle initiation waveform is insured.

The output of the AGC is then mixed with the 131 KHz clock, using a 1496 balanced modulator, configured for a signal gain of 4.8. The output of the modulator is lowpass filtered to preserve the 3 KHz difference frequency, then band-pass filtered and amplified by a factor of 2 by amplifier A4. Thus, the output of A4 is a 0.764 V peak signal, which is then input to a 567 tone detector which is set for a center frequency of 3 KHz, and a bandwidth of 270 Hz.

The output of the 567 (pin 8) is pulled low when a 3 KHz signal is present at its input. The last portion of the circuit measures the duration of the 134 KHz signal and, if it is the proper length, gives an output pulse (SYSTEM SYNC) signifying initiation of the report cycle.

The circuitry after the 567 checks for a 2 second long, logic low output from the 567. When the output of
the 567 goes low, C1 is discharged quickly, disabling the reset of the 4040 counter, and at the same time enabling the 60 Hz clock. So, the 4040 starts counting up, and if Q7, Q6, Q5, and Q4 are all high at the time the 567 output makes its "0" to "1" transition (at the end of the 134 KHz signal), the output of the NAND gate goes low. For Q7, Q6, Q5, and Q4 to all be high, the output of the 567 must be low for between 2.000 and 2.117 seconds. A high at the output of the 567 disables the 60 Hz clock from incrementing the register further. The reset of the 4040 is still enabled for a time after the high on the output of the 567, because the capacitor C1 takes a long time to charge through the 1M resistor. Then, at the next rising edge of the 60 Hz clock, the 4040 is reset, the output of the NAND gate goes high, and the differentiation of this "1" to "0" transition becomes the SYSTEM SYNC pulse.

Now, if for some reason, the detected signal is not 2 seconds in length, then the NAND gate is prevented from ever making a "0" to "1" transition (and therefore a "1" to "0" transition). If the detected signal is too long, (> 2.117 seconds), Q8 goes high, disabling the 60 Hz clock and causing Q4, Q5, Q6, and Q7 to all be low when the 567 output makes its "0" to "1" transition, which prevents the NAND gate output from going low. If the
detected signal is too short, ( < 2.000 seconds), the counter will never have reached the state of Q4 through Q7 all high, and again the NAND gate output will never go low. During the time that the 567 output is high, the 4040 is continuously reset. Since the 4040 is a ripple counter, a capacitor is added at the output of the NAND gate to eliminate glitches, which would cause erroneous SYSTEM SYNC pulses.

Note that the SYSTEM SYNC pulse is synchronized with the rising edge of the 60 Hz clock. In this way, all RMU's are guaranteed to start counting output frames within 16.7 ms of one another. This uncertainty is based on the fact that all RMU's may not be on the same phase of a 3 phase power system and therefore their 60 Hz crossings are out of phase. The importance of this will be discussed in the explanation of the CRU circuitry. Figure 5-19 displays the sequence of events which occur at the initiation of the report cycle.

This completes the description of the RMU circuitry.
Figure 5-19: Report Cycle Sequence
6. CENTRAL REceiving UNIT

6.1 Overall Function

The Central Receiving Unit consists of three parts: The Interface Circuit Card, an S-100 based computer, and the controlling software. These can be seen in the block diagram of figure 6-1. Most of the work associated with the collection of the data from the RMU's is performed on the Interface Circuit Card (ICC), while the computer (and software) performs minor control functions and records the data.

The purpose of the CRU is to generate the proper waveform to initiate the report cycle, to receive and detect the serial stream of data bits which the RMU's send, and to convert this data to parallel form and provide it to the computer.

In order to initiate the process, the operator runs a BASIC program which instructs the computer to set a control signal on the ICC at some preselected time. This causes the ICC to generate the proper report cycle initiation waveform, which is superimposed onto the 60 Hz power lines. The RMU's detect this waveform and begin to send serial data (one RMU at a time) over the power lines via a 131 KHz carrier signal. The ICC must detect this data, so signals on the power lines are band pass...
Figure 6-1: Block Diagram - CRU
filtered at 131 KHz, and sent to detection circuitry
which determines the presence or absence of a 131 KHz
carrier. These detected bits of data are then clocked
into a register at the proper rate. During its output
frame, an RMU will send a 16 bit data word 5 times in
succession, so when 16 bits have been clocked into the
register, a parallel to serial conversion is made, the
data is latched, and a control signal is sent to the
computer instructing it that data is ready to be read.
The computer than reads the energy data by performing a
peripheral input operation at certain specific addresses,
which correspond to port addresses of the peripheral
interface adaptors on the ICC. At this time, the
computer also reads data from other ports on the ICC,
which corresponds to the unit number of the RMU (or
equivalently the number of the present output frame,
e.g., RMU #12 reports in the 12th output frame). This
number is generated by a counter, which counts each
output frame from the time the report cycle was
initiated. The computer keeps a running count (in
software) of the number of times that it receives an
instruction to read data. When this count equals 5 times
the total number of RMU’s in the building, the computer
sends another control signal to the ICC which instructs
the ICC that there is no more data to be collected, and
resets the hardware in preparation for the next day's data collection.

The computer then proceeds to process the data and provide a report for each RMU in the form of a video display. The report lists all data collected during the RMU's output frame. This would consist of 5 sets of power data and unit number data, which should be 5 identical sets of data. However, because of the possibility of bit errors in the transmission, all 5 sets are shown for comparison. When all reports have been read, the program ends, and the process is ready to be initiated again the next day. In practice, the entire process of daily initiating the report cycle and "reading" the reports could be performed by the computer, so that no operator intervention would be required. But for the purposes of this work, manual initiation of the process was used.

The description of the individual parts of the CRU can be found in the following sections.

6.2 The Computer and the S-100 Bus

The ICC was designed to interface directly with the S-100 bus, with no particular computer in mind. Any computer that could drive the S-100 bus properly and could interpret the BASIC program which was used, would
be sufficient. For development purposes, a Sorcerer computer made by Exidy, Inc. was utilized. The computer was attached to an Exidy S-100 Expansion Unit, which allows the Sorcerer to communicate with S-100 peripheral devices. The ICC is plugged into an S-100 slot in this expansion unit. The ICC is shown in figure 6-2, and figure 6-3 shows its positioning in the expansion unit. A television type video monitor was used for the display, and a cassette recorder was used for permanent storage of the BASIC program. The complete CRU is shown in figure 6-4.

The S-100 bus is a standardized, 100 pin bus used in many computers today. An S-100 card contains one row of 50 pins on each side of the card. A list of the S-100 pins utilized in this design, along with their functions, is shown in table 6-1. Unused pins have been omitted for simplicity. As can be seen in the table, the S-100 bus contains two 8-bit uni-directional data buses, one for input data, and the other for output data. For this design, the S-100 bus is used only to perform I/O Read or Write functions (to read or write information to or from the ICC). The timing diagrams of the signals used for an I/O Read and an I/O Write are shown in figures 6-5 and 6-6 respectively. All timing during an I/O Read or Write is automatically controlled through the execution of the
Figure 6-2: Interface Circuit Card
Figure 6-3: Positioning of the ICC in the CRU
Figure 6-4: Central Receiving Unit
BASIC instructions INP or OUT, respectively, which greatly simplifies the programming task.

Aside from reading from and writing to the ICC, the computer is used for some minor computations and to display the information received from the ICC. A further discussion of the computer functions is given in section 6.4, System Software.

6.3 Interface Circuit Card

6.3.1 Power Supply

Power is supplied to the circuitry of the ICC by regulating down the supply lines provided on the S-100 bus, as shown in figure 6-7. Supplies of +/- 12 V and +5 V are used. The +5 V supply is used for all logic on the ICC, and is provided by regulating the +8 V on pin 1 of the S-100 bus. The +/- 12 V supplies are used for a few op-amps on the ICC. Pin 2 on the S-100 bus provides +16 V, which is regulated to +12 V, and pin 52 provides -16 V, which is regulated to -12 V. All supplies are heat-sinked and can each provide a maximum current of approximately 1.5 A.
<table>
<thead>
<tr>
<th>PIN #</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+8V</td>
<td>Unregulated input to +5 V regulators.</td>
</tr>
<tr>
<td>2</td>
<td>+16V</td>
<td>Unregulated input to +12V regulators.</td>
</tr>
<tr>
<td>29</td>
<td>A5</td>
<td>Address Bit</td>
</tr>
<tr>
<td>30</td>
<td>A4</td>
<td>Address Bit</td>
</tr>
<tr>
<td>31</td>
<td>A3</td>
<td>Address Bit</td>
</tr>
<tr>
<td>35</td>
<td>D01</td>
<td>Data-Out Bit</td>
</tr>
<tr>
<td>36</td>
<td>D00</td>
<td>Data-Out Bit</td>
</tr>
<tr>
<td>38</td>
<td>D04</td>
<td>Data-Out Bit</td>
</tr>
<tr>
<td>39</td>
<td>D05</td>
<td>Data-Out Bit</td>
</tr>
<tr>
<td>41</td>
<td>DI2</td>
<td>Data-In Bit</td>
</tr>
<tr>
<td>42</td>
<td>DI3</td>
<td>Data-In Bit</td>
</tr>
<tr>
<td>43</td>
<td>DI7</td>
<td>Data-In Bit</td>
</tr>
<tr>
<td>45</td>
<td>SOUT</td>
<td>Indicates Status of Output Bus.</td>
</tr>
<tr>
<td>46</td>
<td>SINP</td>
<td>Indicates Status of Input Bus.</td>
</tr>
<tr>
<td>50</td>
<td>GND</td>
<td>Signal &amp; Power Ground</td>
</tr>
<tr>
<td>51</td>
<td>+8V</td>
<td>Same as Pin #1</td>
</tr>
<tr>
<td>52</td>
<td>-16V</td>
<td>Unregulated input to -12V regulators.</td>
</tr>
<tr>
<td>54</td>
<td>RESET</td>
<td>Reset from Sorcerer.</td>
</tr>
<tr>
<td>77</td>
<td>PWR</td>
<td>Write Enable</td>
</tr>
<tr>
<td>78</td>
<td>PDBIN</td>
<td>Data Bus In</td>
</tr>
<tr>
<td>79</td>
<td>A0</td>
<td>Address Bit</td>
</tr>
<tr>
<td>80</td>
<td>A1</td>
<td>Address Bit</td>
</tr>
<tr>
<td>81</td>
<td>A2</td>
<td>Address Bit</td>
</tr>
<tr>
<td>82</td>
<td>A6</td>
<td>Address Bit</td>
</tr>
<tr>
<td>83</td>
<td>A7</td>
<td>Address Bit</td>
</tr>
<tr>
<td>88</td>
<td>D02</td>
<td>Data Out Bit</td>
</tr>
<tr>
<td>89</td>
<td>D03</td>
<td>Data Out Bit</td>
</tr>
<tr>
<td>90</td>
<td>D07</td>
<td>Data Out Bit</td>
</tr>
<tr>
<td>100</td>
<td>GND</td>
<td>Same as Pin #50</td>
</tr>
</tbody>
</table>

Table 6-1: S-100 Bus Pin Definitions
Figure 6-5: Timing For I/O Read
Figure 6-6: Timing For I/O Write
Figure 6-7: Power Supply - CRU
6.3.2 Clock Signals and Timing

All clock signals necessary for operation of the ICC are generated on the ICC itself and are derived from two sources. A 2.949120 MHz crystal oscillator is used to generate the 134 KHz clock for the output circuitry. The 60 Hz power line is used to provide frequencies of 60 Hz, 7.5 Hz, 4 Hz, and 0.09375 Hz, which are used for the clocking of input bits and counting of output frames.

Figure 6-8 shows the 2.9491220 MHz crystal oscillator, which is then divided down by a factor of 22 to provide 134.0509 KHz. Division by 11 is accomplished with a 4018 "Divide by N" counter to which an extra stage is added, since the 4018 by itself can only divide by a maximum of 10. The 4018 can be used to divide by an odd number less than 10 by feeding the AND function of two of the counter outputs back to the data input. For example, division by 7 is accomplished by feeding Q3·Q4 back to D; division by 9 is accomplished by feeding Q4·Q5 back to D. So, division by 11 is accomplished in this case by effectively feeding back Q5·Q6 to D. The use of the 4018 in this fashion does reliably provide division by 11, however, this principle is not reliably extended past division by 11 without additional gating. The output of the division by 11 circuit is divided by 2 with a D flip-flop as shown, providing a 134.0509 KHz signal at
50% duty cycle. The 134 KHz clock is disabled at all times except during the actual generation of the report cycle initiation waveform, by the signals REPORT CYCLE and SYSTEM SYNC. These signals will be described in more detail in the following sections.

Figure 6-9 shows the generation of all 60 Hz based clocks. As in the RMU, the 120 V, 60 Hz waveform is divided down through a resistive divider and input to a comparator whose output is then limited to between +5 V and ground with two clamp diodes, thus providing a 0 V to +5 V, 60 Hz square wave. A 4024 binary counter then divides this 60 Hz signal by 8 and 64 to provide 7.5 Hz and 0.9375 Hz clocks respectively. The 0.9375 Hz clock is then divided further by a factor of 10 with a 4017 decade counter, providing a 0.09375 Hz clock.

Also shown in figure 6-9, is the generation of a 4 Hz clock by dividing down the 60 Hz clock using two 4018 "Divide by N" counters configured to divide by 5 and 3. This results in a 4 Hz clock which does not have a 50% duty cycle; but this is unimportant since only the leading edge of this clock is utilized.

The particular use of each of these clock signals will be described in detail in the section describing the circuitry in which they are used.
Figure 6-8: Crystal-Based Clocks - CRU
Figure 6-9:  60 Hz Based Clocks - CRU
6.3.3 Interface Circuitry to the S-100 Bus

The circuitry to interface the ICC with the S-100 Bus is shown in figures 6-10, 6-11, and 6-12. At the heart of this circuitry are two Intel 8255 Peripheral Interface Adaptors (PIA), as shown in figure 6-12, which enable the computer to read and write 8 bit data words to the ICC. The 8255 is a very complex and powerful device, but simply stated, each PIA contains 3 data ports (A, B, and C) which can be configured as either input or output, with an added feature that port C can be split and used as half input and half output, if desired. Input refers to data which is input to the computer (CPU) from the PIA, and output refers to data which is output from the computer to the PIA. The 8 bit word at a port is put on the data bus and read by the CPU during an input operation, and data on the 8 bit data bus is written and latched to a port during an output operation. The ICC uses 4-1/2 ports for input and 1/2 port for output (of the 6 available ports on 2 PIA’s). One port is unused. Port C of PIA #1 is split and used as 1/2 input and 1/2 output. This port provides the control signals to the ICC from the computer, and vice-versa. The other 4 ports are used to hold the data which is to be reported to the computer (a 16 bit energy data word and a 16 bit unit number word). The details of the reading and writing to
the PIA's will be discussed in the software section.

Each port on the PIA's is assigned a different address (one of 256 possible I/O addresses). The six highest order address bits (A2-A7) are decoded to provide the CHIP SELECT (CS) for each PIA, and the two low order address bits (A0-A1) are used to select a particular port on the PIA. The address decoding is shown in figure 6-11. PIA #1 is assigned the address (01000000), and PIA #2 is assigned the address (10000000). The signals CS are driven low if a valid address is present on the address lines, and either one of the signals Status Output (SOUT) or Status Input (SINP) are high. That is:

\[ CS = \text{Valid Address} \cdot (\text{SINP} + \text{SOUT}) \]

Since the PIA data bus is bidirectional, while the S-100 data buses are unidirectional, 74LS241 tri-state buffers are used to isolate the S-100 input and output buses from one another and still provide communication to the PIA (refer to figure 6-12). It is important that the PIA not drive the S-100 input data bus except when it is being read from, otherwise it could be competing with another peripheral device or the CPU. So, the S-100 input data bus is enabled (i.e., connected to the PIA data bus) only when either PIA #1 or PIA #2 is required to put data on the bus during a read operation. The
Figure 6-10: Peripheral Interface Adaptors - CRU
Figure 6-11: Address Decoding - CRU
Figure 6-12: Data Bus Buffering - CRU
signal PDBIN is high at this time, so the signal INPUT BUS ENABLE is provided by the following function:

$$\text{INPUT BUS ENABLE} = (\overline{CS1} \cdot \overline{CS2}) \cdot \text{PDBIN}$$

At all other times, the S-100 output data bus is enabled (i.e., connected to the PIA data bus) which presents no problems since the PIA is not driving the bus at these times (see figure 6-12).

The Read, Write and Reset lines, and low order address bits are buffered and connected to the PIA's. The functional relationship between the signals at the PIA and the signals on the S-100 bus is shown below:

<table>
<thead>
<tr>
<th>PIA SIGNAL</th>
<th>S-100 SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>RD</td>
<td>PDBIN</td>
</tr>
<tr>
<td>WR</td>
<td>PWR</td>
</tr>
<tr>
<td>RESET</td>
<td>RESET</td>
</tr>
<tr>
<td>AO</td>
<td>AO</td>
</tr>
<tr>
<td>A1</td>
<td>A1</td>
</tr>
</tbody>
</table>

These functions are provided by the circuitry shown in figure 6-12.
6.3.4 Report Cycle Initiation Circuitry

The report cycle is initiated by running the BASIC program described in section 6.4. This program causes the computer to write a "1" to Bit 7 on Port C, PIA #1. This control signal is called INITIATE REPORT CYCLE. This is synchronized to the 60 Hz clock with a D flip-flop as shown in figure 6-13, creating the signal REPORT CYCLE. The rising edge of REPORT CYCLE is differentiated and used to parallel load a shift register made up of two 4021 parallel-in, serial-out shift registers cascaded. The loaded data is (011101111111)\(^2\). This data is then shifted out (MSB first) at a 4 Hz rate, causing the output to be high for 1 second, low for 1/4 second, and high for 2 seconds. The leading zero is just to insure the accuracy of the 1 second high regardless of the time that REPORT CYCLE comes high with respect to the 4 Hz clock. The output of the shift register (Q8) is then sent to the output circuitry, and is used to modulate the 134 KHz carrier signal, thus creating the report cycle initiation waveform shown in figure 2-3. The last 3 bits of the 4021 are available as outputs, and these are utilized to determine the end of the 2 second high level. The last 3 bits of the second 4021 (Q6, Q7, and Q8 of 4021-2) are input to an OR gate. The output of this OR gate will normally be high during
Figure 6-13: Generation of the RCIW - CRU
the shifting-out of the register, and will only make a "1" to "0" transition when the last "1" of the 2 second interval is clocked out of the register (zeros are clocked in behind the 2 second interval of ones). When the output of the OR gate goes low, a monostable is triggered which simulates the length of time required for the 567 tone detector on the RMU to drop out of lock at the end of the 2 second burst of the 134 KHz carrier. For the configuration of the 567 as shown in figure 6-13, this "drop-out" time was measured to be repeatable and approximately equal to 25 ms. So the monostable is set to yield a positive going pulse with a pulsewidth of slightly less than 25 ms, triggered on the falling edge of the output of the OR gate. It was found that a pulsewidth of 15 ms, gave the desired results. When the monostable's output goes low, the input of the D flip-flop (after the mono) is caused to go low. This low level is then synchronized to the next 60 Hz rising edge, causing the signal SYSTEM SYNC to go low. This is analogous to how a signal of the same name on the RMU is synchronized to the rising edge of the next 60 Hz clock after the 2 second burst of the 134 KHz carrier. Ideally the two SYSTEM SYNC signals should occur simultaneously (hence the name). This signal (SYSTEM SYNC) is actually the precise beginning of the first output frame (RMU #1).
An analysis of the effects caused by the two SYSTEM SYNC signals (on the RMU and the CRU) occurring at different times is performed in section 6.3.7, in the discussion of the clocking of input bits.

The signal SYSTEM SYNC on the ICC is used to hold a number of counters in the reset position, until the beginning of the first output frame. In this way, all timing is synchronized with the beginning of the first output frame.

6.3.5 Output Circuitry

The bits from the shift register of the previous section are used to modulate the 134 KHz clock and create the report cycle initiation waveform, which is superimposed on the 60 Hz power lines with the circuit shown in figure 6-14. This circuit is very similar to the output circuit of the RMU which was discussed in sections 4.1 and 5.6, so a detailed discussion will not be performed here. A relatively low-power output stage (+5 V and ground) is used on the ICC, because the main purpose of this prototype was to prove the concept of sending and receiving the necessary data over the power lines. No attempt was made to idealize this output stage for use over long distances, as would be required in an apartment building.
Figure 6-14: Output Circuit - CRU
If the output bit is a "1", the 134 KHz signal propagates through the NAND gates shown in figure 6-14, driving the 2N2222 transistor which acts as a 25 mA current source for the tuned transformer. Which would yield a theoretical output voltage of 0.32 V peak. The output voltage, \( V_{out} \), was experimentally measured to be 0.35 V peak, in relatively close agreement with theory.

As in the RMU, the primary of the output transformer is tapped and used as the input to the Bit Detection circuitry, which is described in the next section.

6.3.6 Bit Detection Circuitry

The purpose of the bit detection circuitry is to detect the information sent to the CRU by the RMU. This information is encoded in a 131 KHz carrier whose presence indicates a "1" and whose absence indicates a "0". The transformer of the output circuitry is used to step up carrier signals on the power lines, which are then presented to the input of the bit detection circuitry as shown in figure 6-15. The step-up ratio from secondary to primary in the circuit of figure 6-14, was measured to be 32:1.

Some soft limiting is then performed on the stepped-up carrier which is then converted from a differential signal to single-ended by amplifier A1.
Figure 6-15: Bit Detection Circuit - CRU
Amplifier A2 is used to band-pass filter the carrier signal and amplify it by a factor of 2. The signal is then input to a 567 tone detector set to a center frequency of 131 KHz with a bandwidth of 2%. The output of the 567 (pin 8) is pulled low if the 131 KHz signal is present, so this output is inverted which then becomes the input bit stream, which is then sent to the energy data receiving circuitry, which is described in the next section.

6.3.7 Energy Data: Receiving Circuitry

The detected bits from the Bit Detection circuitry are input to the circuit shown in figure 6-16. The bits are clocked into a pair of cascaded 4094 shift registers. These shift registers are serial-in, parallel-out, with an output latch. The bits are clocked in at a 7.5 Hz rate, corresponding to the bit time of 133.33 ms. The 7.5 Hz clock obtained in section 6.3.2 and figure 6-9 is offset to provide a positive-going edge at 83.33 ms after the beginning of the bit (or 5/8 the total time for the bit). This is done to allow the detection circuitry to settle into the proper "1" or "0" state, and also to allow for possible time shifts caused by RMU's which are not on the same phase of the 60 Hz power system. The offset of the 7.5 Hz clock is accomplished by clocking
the 7.5 Hz clock into a shift register at a 60 Hz rate as shown in figure 6-16. The output is taken at the 5th stage of the shift register, and so is delayed by 5/8 the period of the 7.5 Hz clock. A timing diagram of the clock signals is shown in figures 6-17 and 6-18.

The data word that the RMU sends to the CRU is 16 bits long (repeated 5 times). The cascaded pair of 4094's provides space for 16 bits, and at the time when the 16th bit is clocked in, a pulse is applied to the strobe inputs, which allows the data in the shift registers to propagate to the outputs while the strobe is high, and be latched there on the falling edge of the strobe pulse. The strobe pulse is generated by counting the number of clock pulses that the 4094's receive. The timing of this strobe pulse is also shown in figure 6-17.

Each time that the strobe pulse occurs, a flip-flop is set which provides the control signal DATA READY to the computer. During the collection of data, the computer continuously checks the status of this bit. When the computer observes that this bit is high, it reads the energy data by reading ports A and B on PIA #1. Since the data is sent by the RMU in a most significant bit to least significant bit form, Port B contains the high order bits, while port A contains the low order bits. Recall that the 4 most significant bits are
Figure 6-16: Energy Data Receiving Circuit - CRU
Refer to Figure 6-18 (Part B)

Figure 6-17: Timing For Clocking of Input Data - Part A
Figure 6-18: Timing For Clocking of Input Data - Part B
actually the preamble, which is sent along with the 12 bits of energy data.

At the time that the energy data is read, the computer also reads the RMU number, or equivalently the frame number, by reading Ports A and B on PIA #2, Port B being the most significant bits.

After all four ports are read, the computer pulses the control signal DATA TAKEN high, then low, which resets the DATA READY signal. At this time, the computer resumes its monitoring of the DATA READY signal until it goes high once again, at which time the process of reading data is repeated.

The RMU number (frame number) is generated by clocking a 4040 binary counter at a 0.09375 Hz rate (the reciprocal of the 10.667 second output frame time), beginning at the time when SYSTEM SYNC goes low. The clock signal for this counter is shown in the timing diagram of figure 6-17.

In the design, consideration had to be given to two problems of synchronization within the system. First, all RMU's may not all be on the same phase of the 60 Hz power system, and second, all RMU's may not create the SYSTEM SYNC signal at exactly the same positive-going 60 Hz zero-crossing, due to component variations, especially in the 567 tone detector circuitry. The maximum possible
Figure 6-19: Analysis of Synchronization Errors
time error due to different phases is +/- 11.11 ms, and the time error due to different 60 Hz zero crossings will be 16.67 ms per period of the 60 Hz waveform. As is shown in figure 6-19, for a bit time (length of one bit) equal to 133.33 ms, a synchronization error of +/- 2 cycles of 60 Hz plus variations due to different phases can easily be tolerated and still reliably detect the transmitted bits. In the worst case, the data bit will be clocked in at 29% or 96% of the nominal frame. Neither case presents a problem with detection, since 29% of the bit time is 39 ms which is longer than the 25 ms worst case lock-up time of the 567 tone detector; and the 567 will definitely be locked at 128 ms (96%) into the nominal frame.

There is also no problem with the possible overlap of output frames due to these worst case variations, for two reasons. First, because any overlap of output frames would cause at most a 1 bit error in both transmissions which would easily be corrected because of the 5 redundant sets of data for each RMU. And second, the first bit of each 16 bit data word (and hence the first bit of each output frame) that the RMU sends is forced to be a zero because of the preamble (0110 in a properly functioning unit), and therefore would not cause any interference with the last bit of the previous output
frame, even if the frames should overlap by the worst case error.

The details of the data reading and the control of the ICC are described in the next section, System Software.

6.4 System Software

A BASIC program was implemented to control the operation of the ICC and of the data reading process (report cycle). A flow chart of the program is shown in figures 6-20 and 6-21. The program has been named "REPORTCONTROL", and the actual program listing has been filed with the Department of Computer Science and Electrical Engineering.

To initiate the report cycle, the operator runs the program REPORTCONTROL, with the ICC plugged into the S-100 expansion unit of the computer, and the line cord of the ICC plugged into a 60 Hz power outlet. The program asks the operator to input the total number of RMU's in the system. After this information is supplied, the program initializes the two PIA's on the ICC, setting them for the proper mode of operation, by writing a data word to the control register of each PIA. The two PIA's are set to mode 0 (basic input/output) with ports A, B, and the lower half of Port C (4 LSB's), set as
Figure 6-20: Software Flow Diagram - Part A
RESET "DATA READY"
WRITE A "1" TO PIA#1, PORT C, BIT 6

SMALL DELAY

WRITE A "0" TO PIA#1, PORT C, BIT 6

HAVE ALL RMU'S REPORTED 5 SETS OF DATA?

YES

END REPORT CYCLE
WRITE A "0" TO PIA#1, PORT C, BIT 7

PROCESS DATA

GENERATE REPORT

END

Figure 6-21: Software Flow Diagram - Part B
input ports; and the upper half of port C set as an output port, on both PIA's. (Port C on PIA #2 is unused, but is set the same as PIA #1 for simplicity).

Writing to a port is accomplished with the BASIC instruction: (OUT address, data) which performs a peripheral device output. In a similar fashion, reading a port is accomplished with the BASIC instruction: (INP(address)) which performs a peripheral device input.

After the PIA's are initialized, the program waits for the operator to indicate the start of the report cycle. When this is done, the program sets INITIATE REPORT CYCLE high by writing a "i" to bit 7, port C, PIA #1. This causes the ICC to send the report cycle initiation waveform and prepare for the receipt of data. The program continuously reads bit 0, port C, PIA #1, which is the signal DATA READY. When this bit goes high, the computer then reads four 8 bit data words: HI energy data from PIA #1, port B; LO energy data from PIA #1, port A; HI output frame number from PIA #2, port B; and LO output frame number from PIA #2, port A. It is not necessary for the computer to read the output frame number from the ICC (and therefore no need to generate this number on the ICC), as this could just have been generated more easily in software by counting the number of DATA READY signals. However, by reading this number
from the ICC, proper operation of the ICC is verified. Also, it was planned that in the final system, it might be desired to add some type of LED display to the ICC to display the energy data and the output frame number for each RMU as it is reported, in which case, the output frame number would have to be generated on the ICC.

After all four ports of data have been read, the computer creates a RESET DATA READY pulse, by writing a "1", then a "0" to Bit 6, Port C, PIA #1. Then the computer monitors the DATA READY signal again, until it again goes high. The process is repeated until all RMU's have reported 5 times. When this occurs, the computer informs the ICC of this fact by bringing REPORT CYCLE low (by writing a "0" to Bit 7, Port C, PIA #1). This automatically resets the circuitry on the ICC, in preparation for the next day's report cycle.

Next, the program generates a report for each RMU which shows all the data which was received during that RMU's output frame. All 5 redundant transmissions are shown for comparison. A sample report used for test purposes is shown in figure 6-22. After all reports have been read, the program ends, and the report cycle may be repeated at any time thereafter.
REMOTE ENERGY MONITORING SYSTEM
REPORT FOR RMU #2

<table>
<thead>
<tr>
<th>RMU NO.</th>
<th>PREAMBLE (6=O.K.)</th>
<th>ENERGY DATA (DECIMAL)</th>
<th>ENERGY DATA (BINARY)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>6</td>
<td>1673</td>
<td>0110010001001</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
<td>1673</td>
<td>0110010001001</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
<td>1673</td>
<td>0110010001001</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
<td>1673</td>
<td>0110010001001</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
<td>1673</td>
<td>0110010001001</td>
</tr>
</tbody>
</table>

PRESS CARRIAGE RETURN FOR NEXT REPORT.

Figure 6-22: Sample Report
7. SYSTEM PERFORMANCE

7.1 System Accuracy

There are four possible sources of error in the energy monitor system. They are:

1. Errors due to non-linearities of input current transformers.
2. Errors due to non-linearity of the analog multiplier.
3. Errors due to the A-D conversion circuitry.
4. Errors due to data transmission between RMU and CRU.

Although an analysis of current transformer error has not been performed herein, Tsuda [16] has determined that this error can be reduced to 1 LSB of an 8 bit A-D conversion scheme, for some minimum value of primary current.

The Exar analog multiplier employed has a maximum output error of 1% of full scale, which represents 2.6 bits of an 8 bit conversion.

The A-D conversion scheme itself causes +/- 1/2 LSB error due to the non-linearity of the D-A converter, plus a 1 LSB error due to quantization error.

Errors due to the data transmission between the RMU and CRU will be taken to be negligible because of the quintuple redundancy and the expected infrequency of even...
a 1 bit transmission error.

Thus, the total possible error is 5.1 bits out of a possible total energy count of 256 at full scale, which is an absolute error of 2% of full scale. Approximately half of this error is caused by the non-linearity of the multiplier, and therefore could be reduced by utilizing a more accurate multiplier than the XR-2208. Further gains in accuracy could be provided by using more than 8 bits in the A-D conversion, and/or further advances in instrument current transformer technology.

7.2 System Tests

Each section of the circuitry of the RMU and the CRU was determined to function correctly as the various sections were built and connected together. Although a current measurement was not actually made, the proper operation of the input, multiplier, and A-D conversion circuitry was verified by using a scaled version of the voltage waveform for both the "current" and voltage inputs.

The major purpose of the system test was to determine the feasibility and reliability of the data link between the RMU and CRU. A specific energy data word was permanently set on the RMU for these purposes. Two locations were used for testing. The first tests
were performed in Packard Lab, Lehigh University, with the RMU and the CRU plugged into separate outlets (same phase) in the same room. These two outlets derived their power from the same distribution panel in the room.

The BASIC program used to control the system was run in excess of 50 times, resulting in over 50 "report cycles" during which the preset data word on the RMU was transmitted to the CRU, making a total of 4000 reported bits. Not one bit in these 4000 was transmitted in error, thus the contention that single bit errors will occur very infrequently seems reasonable.

A test was performed to determine if in fact the two signals SYSTEM SYNC (one on the RMU, one on the CRU) occurred at the same 60 Hz zero crossing. Initially, the CRU SYSTEM SYNC occurred 1 cycle of 60 Hz after the RMU SYSTEM SYNC. This was corrected by trimming the monostable delay on the CRU to the value specified in figure 6-13, after which the two signals occurred at the same 60 Hz crossing.

Next, a test of the distance over which communication could be carried out was performed. The RMU was plugged into an outlet in the same room as the CRU, which was known to derive power from a different distribution panel (but on the same phase as the CRU). Repeated attempt were made to initiate the report cycle,
and all failed. Then the RHU was moved to the 2nd floor, while the CRU was kept on the 5th floor. Outlets on the same phase of the power system were used, and repeated attempts were made to initiate the report cycle. Again, all attempts failed.

These failures are believed to be caused by the relatively hostile environment presented to carrier signals in Packard Lab. Large numbers of computers, computer terminals, oscilloscopes, etc. are present in Packard Lab, which contain capacitive power-line filters which are especially good at shorting out any high frequency signals on the power lines. A carrier which had to travel over any great distance in the Lab would most likely run into one of these pieces of equipment somewhere along the line, and would probably be trapped (shorted out) by its line filter. Since the output stage of the developed CRU is relatively low-power (for test purposes), it is not expected that the carrier would be able to compete with this type of environment. In an actual system, the output circuit of the CRU would be very high power, which would enable the carrier signals to propagate to all parts of a building. Also, if particular problems are known to exist (such as the line filter of the computer in the CRU), small chokes can be added in series with the line cords of such instruments.
This would alleviate the problem of the capacitive line filters shorting out carrier signals, while assisting in the purpose for which the line filter was designed, since the choke would present a high impedance to carrier signals.

The second test location was a single-family, split level dwelling located in River Vale, NJ. This location is more typical of the designed use of the energy monitor system, in that it is a residential dwelling, and equipment which would cause the shorting-out of the carrier is most likely not prevalent. The CRU was placed at one location in the house, and the RMU was tested in every other circuit in the house. Approximately 20 report cycles were initiated, and not a single bit error occurred. Proper operation was observed from every circuit in the house. Then, as a further test of the distance performance of the system, the RMU was plugged into the house of a neighbor, across the street from the house which contained the CRU. Both houses derive power from the same side of a distribution transformer. The total distance between RMU and CRU (along the power lines) was estimated to be approximately 40 meters. Numerous report cycles were initiated, and proper operation occurred, without a single bit error. From this test, it is observed that system operation over even
large distances (in a residential setting) is reliable.

One last observation which was made concerns a slight problem with the RMU's receipt of the report cycle initiation waveform. There were a few instances (~2% of the time) where the RMU would not accept the report cycle initiation waveform as sent by the CRU. It is believed that this is due to variations in the lock-up time of the 567 tone detector on the RMU, which caused the RMU to sense that the 2 second carrier burst sent by the CRU was either shorter or longer than the allowed tolerance. This does not present a tremendous problem, because if the RMU does not sense the report cycle initiation waveform, it simply holds its data until the next day's report cycle, as was stated previously. However, in the interest of increased system reliability, this problem could be eliminated through closer attention to the lock-up and drop-out transients of the 567 tone detector.

For the most part, the system performed the anticipated functions properly, with no errors in data transmission, and was observed to have an operable range of at least 40 meters distance.
8. CONCLUSION

Remote energy monitoring by means of a power-line carrier system has been demonstrated. Measurement of electrical energy consumption is performed by a number of Remote Measuring Units (PMU's) which report digital data to the Central Receiving Unit (CRU) via an amplitude-shift keyed (ASK) 131 KHz carrier signal. System operation was observed to be reliable over a distance of at least 40 meters (between RMU and CRU). Not a single bit error occurred during any of the test transmissions. The remote energy monitoring system provides an accurate, low-cost means for the owner of a building to distribute the electric bill according to the energy consumed by the individual tenants.

Further research and work could be done on the subject of the lock-up and drop-out transients of the tone detector phase-locked loops, which were found to cause some slight problems. In addition, further investigation could be made into optimizing the frequency of operation, and also the possible interference effects (T.V., radio reception) which this remote energy monitoring system might cause at certain operating frequencies.

Overall, the remote energy monitoring system performed its designed functions properly and reliably.
If put into use, such a system would provide the proper accountability for electrical energy consumption, which would encourage energy conservation, reduce energy costs, and thereby enhance the attractiveness of an apartment building or condominium to prospective tenants.
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VITA

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