A model for oxide isolated substrate fed I2L.

Clarence E. Williams

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A MODEL FOR OXIDE ISOLATED SUBSTRATE FED I^2L

by

Clarence E. Williams, Jr.

A Thesis
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April 24, 1979
Date

Professor in Charge

Chairman of the Department
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ABSTRACT

An oxide isolated substrate fed $I^{2}L$ cell\(^{(4)}\) has been developed which has a higher packing density and a lower power-delay product than conventional $I^{2}L$. The cell consists of an updiffused, Schottky clamped, NPN transistor and a vertical PNP transistor which acts as a current source at the base of the NPN. The inherent high gain of the NPN structure has greatly reduced the problem of limited fanout encountered with conventional $I^{2}L$. These two transistors are integrated together to form a compact logical inverter.

A charge-control model is introduced to describe the behavior of the $I^{2}L$ cell. Measurements of the parameters required for the charge-control model are given for fabricated devices and the techniques used to obtain them are discussed. A computer simulation of the power-delay product of the $I^{2}L$ cell was made using the charge-control model. Power-delay results from the simulation agree well with measurements made on a ring oscillator. At low power the cell delay was 76 nsec at 12 uwatts of power per cell. At an increased power of 200 uwatts per cell the delay decreased to 10 nsec. An increase in the gain and a decrease in the reverse transit time of the PNP transistor, accomplished by decreasing the impurity concentration in
the PNP base region, will improve the performance of the cell. Simulations show this would result in a cell delay of approximately 21 nsec at 12 µwatts of power per cell. Increasing the power to 100 µwatts per cell reduced the delay to 8 nsec.
I. INTRODUCTION

Due to the increasing size and complexity of Large-Scale Integrated (LSI) logic circuits, a small and simple gate structure is needed. This gate must have a low power-delay product and should be compatible with an already existing technology. A proposed method\(^{(1, 2)}\) of achieving these goals was Integrated Injection Logic (I\(^2\)L), also called Merged Transistor Logic (MTL).

The I\(^2\)L cell is made with the standard bipolar technology, requiring a minimum of four mask steps through metallization. It consists of complementary NPN and PNP transistors and requires no ohmic load resistors. The PNP device is a lateral structure, while the NPN device is operated in the inverse mode. The self-isolating nature of the cell leads to packing densities on the order of 40-80 gates/mm\(^2\) with 10\(\mu\) design rules.

Since the I\(^2\)L structure contains only transistors, power and delay can be traded off directly on the same chip, giving excellent design flexibility. A power-delay product of 2 pJ is possible with a minimum propagation delay time of 25 nS at high currents.

An improvement in both size and speed of the basic I\(^2\)L cell is needed for future logic circuits. An extension of the basic I\(^2\)L cell, which provides the desired improvements, is the oxide isolated substrate
fed $I^2L$ structure.\(^{(3,4)}\) The structure fabricated by Blatt, et al is formed from two epitaxial layers on a heavily doped P-type substrate. The structure fabricated by Agraz-Guerena, et al uses a single epitaxial layer and an updiffused NPN profile. In this paper a model will be developed to predict the operation of the latter structure and experimental data taken on these devices will be presented. A brief background of how oxide isolated substrate fed $I^2L$ evolved is given first. Following this, the basic operation and the structure of the cell are discussed. Then a charge-controlled model is presented which adequately describes the operation of the $I^2L$ cell. Next, experimental results are discussed along with the methods used to obtain them. Finally, the model will be simulated using the measured parameters and the results will be compared to the measurements of a ring oscillator contained on the same chip with the $I^2L$ cell.
II. EVOLUTION TO OXIDE ISOLATED SUBSTRATE FED I²L

The realization of bipolar LSI circuitry has been largely made possible by the development of I²L. As first proposed, I²L had the potential of achieving densities comparable to those of metal-oxide semiconductors (MOS) but not of achieving higher speeds.

The I²L cell layout eliminates the need for current sources and load resistors which consume both space and power. The standard cell is made up of a complementary transistor pair, a vertical NPN transistor and a lateral PNP transistor, merged into the same semiconductor region. The NPN transistor has multiple collector outputs and acts as an inverter while the PNP transistor serves as a current source load, eliminating the need for ohmic resistors. In comparison, a typical TTL gate requires six or eight transistors along with source and load components.

The power-delay product of a typical cell is 2.0 pJ per cell with a minimum cell delay of approximately 30 nS with 10 µm tolerance. This allows use of the cell at speeds near the speed of TTL but with a much higher packing density, 40-80 gates/mm². Where speed isn't essential, such as in watch circuits, the I²L chip can operate with only microwatt dissipation (1 µA per
gate) while providing high-current drive capability for light-emitting diodes.

This form of bipolar logic is also very versatile since it is made with conventional bipolar processing. This allows both digital and analog functions on the same chip without the need of special circuit techniques required with MOS. Resulting designs include CODECs, digital-voltmeter chips, frequency dividers for electronic organs, and linear circuits for radio and television. Buffers which allow interfacing to other forms of logic such as TTL are also easily implemented, as well as high speed logic including Schottky TTL and ECL circuitry for critical delay paths.

To expand the number of applications of \( I^2L \) circuits, the performance needs to be improved. The power-delay product is limited by parasitic capacitances in the low current region of operation. Thus, a reduction in area of the cell will not only increase the packing density but will also lower the power-delay product by decreasing parasitic junction capacitances. With 5 \( \mu \)m design rules the power-delay product is reduced to 1 pJ per cell with a minimum cell delay of 25 nS with a packing density of 30-160 cells/mm\(^2\).

Another method of reducing the power-delay product is to reduce the logic voltage swing. To
accomplish this, Schottky diodes are formed in the multicolectors of the NPN switching transistor.\(^{(5)}\) This is done by forming the active base using a deep boron implantation and a phosphorus implantation in the collector contact region. The resulting top surface is $n^-$ for forming PtSi Schottky diodes with a barrier height tailored to provide a 250 mV signal swing at room temperature.\(^{(6)}\) This is done by a phosphorus ion implantation which enhances the epitaxial doping in the parasitic Schottky collector. The power-delay product for Schottky $I^2L$ is 0.3 pJ per cell with a minimum cell delay of 15 nS with no change in packing density from that of conventional $I^2L$. This technique has the disadvantage of reducing noise margin, which makes the use of a single-level metal system with diffused crossunders marginally acceptable. An alternative is to use a two-level metal interconnect system which has an added benefit of increased packing density.

To further increase the packing density, the lateral PNP transistor may be replaced with a vertical PNP transistor.\(^{(3,4)}\) This form of $I^2L$, where the p-type substrate is the PNP emitter or common injector for all $I^2L$ cells, is referred to as substrate fed logic (SFL). The packing density is increased by 50\% (120-240 cells/mm\(^2\) with 5\(\mu\) tolerances). The decrease in cell area
causes a reduction in the parasitic junction capacitances. This results in the power-delay product being reduced to 1 pJ per cell with a minimum cell delay of 20 nS.

An additional advantage of substrate fed \( I^2L \) is that the NPN transistors are automatically equidistant from the injector, which allows the transistors to be oriented in any desired fashion, giving a very flexible layout. This is in contrast to the conventional \( I^2L \) where the base region is laid out perpendicular to the injector. As a result, the lateral voltage drop in the base resistance causes the current density in the base to decrease from the nearest output to the injector to the most remote output, allowing only the collector nearest to the injector to switch at maximum speed. Each succeeding output, moving away from the injector, switches at progressively slower speeds.

The use of dielectric isolation instead of the conventional junction isolation will further improve both the power-delay product and intrinsic delay.\(^{(7)}\) Silicon dioxide is used as the isolating dielectric which causes a significant drop in the parasitic junction capacitance. There is also an increase in packing density in the non-\( I^2L \) circuitry since the required large spacing from the active device to the isolation
region has been eliminated. The power-delay product is 0.1 pJ with a minimum cell delay of 5 nS and a packing density of 200-300 cells/mm².

A summary of the performance of the various forms of I²L is given in Table I. To make I²L competitive as a high speed bipolar technology while attaining a high packing density, a combination of the above improvements is used. This paper will present a model of an oxide isolated substrate fed I²L cell with Schottky diodes on the outputs. A ring oscillator built on the chip to measure the power-delay product contains only single-level metal.
III. STRUCTURE AND OPERATION OF I²L CELLS

The structure of the conventional I²L cell, using the standard bipolar process, will be discussed first. The logic circuit equivalent of a cell having three outputs is shown in Figure 1 and its topology and cross section in Figure 2. The NPN transistor is formed by a double diffused structure operated in the inverse mode. The N-type epitaxial layer forms the grounded emitter and the shallow n⁺ diffusion provides the multiple collector outputs. The need for isolation between cells is eliminated since they are operated in the common emitter mode. For the topology shown, an input and a maximum of five outputs are available with any unused tracks being available as wiring channels between cells. The emitter and collector of the lateral PNP transistor are formed by the P-type base diffusion with the collector being common to the base of the NPN transistor. The n⁻ epitaxial layer is the base of the PNP transistor and is thus in common with the emitter of the NPN transistor. The PNP transistor, though relatively inefficient, is well suited for cell layout since the emitter or injector can be made as a long "injector rail". This permits rows of cells to be placed on both sides of this rail, resulting in two rows of cells. The n⁺ collar,
shown in Figure 2, surrounding the base region suppresses unwanted lateral hole injection. This provides a marked increase in the NPN upward gain, through an improvement in the injection efficiency of the emitter-base junction, and permits cell-to-cell isolation with minimum separation.

The $I^2L$ cell is a single input, multiple output circuit. Outputs of several cells going to the same input are wire-ANDED and then inverted by the NPN transistor, thus performing the NAND function. This is illustrated in Figure 3 where outputs (A and B) of two $I^2L$ gates are wire-ANDED and then inverted, giving the Boolean function $\overline{A \cdot B}$ at the output of the inverter. Each output must be able to sink the current supplied to the base of the following $I^2L$ cell.

The conventional NAND logic diagram and the conversion to multiple output NAND representation are shown in Figure 4 for a D-type flip-flop. The layout technique using conventional $I^2L$ is demonstrated in Figure 5. The logic units are placed parallel to one another and perpendicular to the injector. The input and output connections are represented by "X" and "0", respectively. In the design of this figure, the input and output connections can be made in any of the six available wiring tracks.
The topology and cross section of an oxide isolated substrate fed I$^2$L cell$^{(4)}$ is shown in Figure 6. The vertical impurity profile of both the NPN and the PNP are shown. The substrate is the emitter of the vertical PNP transistor. A shallow buried layer in the substrate forms the base of the PNP transistor. A diffused p$^+$ region serves as the collector of the PNP as well as the ohmic contact to the input of the cell. The base region of this PNP transistor is quite narrow, 1 $\mu$m, relative to previous$^{(3)}$ substrate fed devices where the base region was a 3 $\mu$m n-type epi layer. Therefore, this PNP transistor should be compatible with faster I$^2$L circuits. It should be noted that leaving the buried layer out permits a contact to be made to the substrate.

The NPN transistor in the cell of Figure 6 is formed as an upward structure.$^{(7)}$ After the n$^+$ buried layer has been implanted in the substrate, boron is selectively diffused into this buried layer. The boron impurities diffuse ahead of the antimony from the n$^+$ buried layer into the n-type epitaxial layer, forming an active, upward profile. The device has a highly doped emitter and a favorably graded base region and is not sensitive to the thickness of the epi layer. The N-type doped epi layer forms the lightly doped collector. The profiles of both the NPN and PNP devices are shown in Figure 7.$^{(4)}$
The size and capacitance of the device is greatly reduced by the use of oxide isolation. Since this is done near the end of the processing schedule, a problem arises with junction movement due to any high temperature oxidation techniques. This was solved by using a high-pressure, low-temperature scheme (300 psi steam, 700°C) which has no effect on the updiffused base profile.

As shown in Figure 6, the emitter and base of the NPN transistor are electrically common to the base and collector of the PNP transistor, respectively; the same as for conventional $I^2L$. A Schottky diode contact will be formed at the collector output for the device as shown. For an ohmic contact, a shallow, low dose donor implant may be made in the collector region. Multiple outputs can be formed by expanding the base region and adding as many outputs as required, with all outputs being equidistant from the injector.

The layout technique of the D-type flip-flop shown in Figure 4 is demonstrated for oxide isolated substrate fed $I^2L$ in Figure 8. The packing density is not only increased due to fabrication techniques but also because of the freedom in orientation and the elimination of unused input/output sites.
IV. CHARGE-CONTROL MODEL

A charge-controlled model will be used, to describe the operation of the oxide isolated substrate fed I^2L gate following the approach of Searle.\(^{(10)}\) Charge is stored in a device as minority carriers in the neutral regions and as space charge in the junction regions. Expressions can be developed relating this charge to measurable physical parameters such as junction areas and concentrations. An analysis of the switching operation can be made once the charge storage of the device and the currents that transport the charge have been determined. Charge-controlled analysis has a drawback in that fine details of waveforms and the exact physics involved in charge removal may be lost. This proves to be of little importance since the on-off nature of operation of switching circuits does not require knowledge of these details for most practical design work.

A. Current Flow

First, the current in a charge neutral segment of silicon with a nonuniform doping profile will be examined. This will correspond to the base region of the NPN transistor in the I^2L gate. With proper substitutions this can be applied to the emitter and collector as well.

The derivation of the current will follow the approach of Leenov\(^{(11)}\) and Gray.\(^{(12)}\) The electron and
hole current densities can be expressed in terms of their drift and diffusion components by:

\[ J_e = q\mu_n E_x + qD_e \frac{dn}{dx} \quad (4.1) \]

\[ J_h = q\mu_h pE_x - qD_h \frac{dp}{dx}. \quad (4.2) \]

If we consider the base region of an NPN transistor, \( J_h \ll J_e \), the minority carrier current is much greater than the majority carrier current with no external field applied. Thus, \( J_h \) in Equation (4.2) may be set equal to zero giving:

\[ 0 = q\mu_h pE_x - qD_h \frac{dp}{dx}. \quad (4.3) \]

Solving for \( E_x \):

\[ E_x = \frac{D_h}{\mu_h} \frac{dp}{dx}. \quad (4.4) \]

Substituting Equation (4.4) into Equation (4.1), \( J_e \) is found to be

\[ J_e = q\mu_e n \frac{D_h}{\mu_h} \frac{dp}{dx} + qD_e \frac{dn}{dx}. \quad (4.5) \]
Using the fact that \( \frac{D_n}{\mu_n} = \frac{D_e}{\mu_e} \) resulting from the Einstein relationship, the current density is given by:

\[
J_e = qD_e \left[ \frac{n}{p} \frac{dp}{dx} + \frac{dn}{dx} \right].
\]  \( (4.6) \)

Since this is a p region (\( n \ll p \)), making \( n/p \ll 1 \), Equation (4.6) reduces to:

\[
J_e = qD_e \frac{dn}{dx}.
\]  \( (4.7) \)

For an NPN transistor with a junction area \( A \), the resulting current would be:

\[
I_e = -qAD_e \frac{dn}{dx}.
\]  \( (4.8) \)

To solve for \( n_B(x) \), the diffusion equation will be used:

\[
\frac{\partial n_p}{\partial t} = D_e \frac{\partial^2 n_p}{\partial x^2} - \frac{(n_p - n_{p0})}{\tau_e}.
\]  \( (4.9) \)

For the DC case, Equation (4.9) may be set equal to zero, since \( \frac{\partial n_p}{\partial t} = 0 \), and rearranged giving:

\[
\frac{\partial^2 (n_p - n_{p0})}{\partial x^2} = \frac{n_p - n_{p0}}{D_e \tau_e}.
\]  \( (4.10) \)
where the subtraction of \( n_{po} \) on the left-hand side of the equation has no effect since the derivative of a constant is zero. The excess electron concentration is defined as the difference between the total concentration and the corresponding equilibrium, that is:

\[
n_p' = n_p - n_{po} .
\]  

(4.11)

Also, the diffusion length for minority-carrier electrons is:

\[
L_e = \sqrt{ \frac{D_e}{\tau_e} } .
\]  

(4.12)

Substituting Equation (4.11) and Equation (4.12) into Equation (4.10) yields:

\[
\frac{\partial^2 n'}{\partial x^2} = \frac{n'}{L_e^2} .
\]  

(4.13)

The general solution to this linear differential equation is:

\[
n'(x) = C_1 e^{-x/L} + C_2 e^{x/L}
\]  

(4.14)

The solution can be found by looking at the boundary conditions for a base width \( w \).
At $x = 0$:

$$n'(0) = 0 = C_1 e^0 + C_2 e^0 = C_1 + C_2 \quad (4.15)$$

or

$$C_2 = n'(0) - C_1 \quad (4.16)$$

And at $x = w$:

$$n'(w) = C_1 e^{-W/L} + C_2 e^{w/L} \quad (4.17)$$

By substituting Equation (4.16) into Equation (4.17) and rearranging, $C_1$ is found to be:

$$C_1 = \frac{n'(0) e^{w/L} - n'(w)}{e^{w/L} - e^{w/L}} \quad (4.18)$$

and $C_2$ is:

$$C_2 = n'(0) - C_1 = \frac{n'(w) - n'(0) e^{-w/L}}{e^{w/L} - e^{-w/L}} \quad (4.19)$$

The values of $C_1$ and $C_2$ may now be substituted into Equation (4.14), and after rearranging the value of $n'(x)$ is given by:
\[
n'(x) = n'(0) \frac{\sinh \frac{w-x}{L_e}}{\sinh \frac{w}{L_e}} + n'(w) \frac{\sinh \frac{x}{L_e}}{\sinh \frac{w}{L_e}}. \tag{4.20}
\]

Writing the emitter current, \( I_E \), using Equation (4.8) with \( x = 0 \) results in:

\[
I_E = qA_D e \left. \frac{dn}{dx} \right|_{x=0}
\tag{4.21}
\]

and substituting into Equation (4.20) gives:

\[
I_E = \frac{-qA_D e}{L_e \sinh \frac{w}{L_e}} \left[ n'(0) \cosh \frac{w}{L_e} - n'(w) \right]. \tag{4.22}
\]

Similarly, the collector current, \( I_C \), can be found with \( x = w \):

\[
I_C = -qA_D e \left. \frac{dn}{dx} \right|_{x=w}
\tag{4.23}
\]

\[
= \frac{qA_D e}{L_e \sinh \frac{w}{L_e}} \left[ -n'(0), + n'(w) \cosh \frac{w}{L_e} \right]. \tag{4.24}
\]

With a positive potential applied to the base, the value of \( n'(x) \) at the boundaries for \( V_{BE} \) and \( V_{BC} \) having any value is:

\[
n'(0) = n_{BO} \left[ \exp \left( \frac{qV_{BE}}{kT} \right) - 1 \right] \tag{4.25}
\]
\[ n^-(w) = n_{Bo} \left[ \exp(qV_{BC}/kT)-1 \right]. \quad (4.26) \]

The substitution of Equation (4.25) and Equation (4.26) into Equations (4.22) and (4.24) results in:

\[ I_E = -I_1 \left[ \exp(qV_{BE}/kT)-1 \right] + I_2 \left[ \exp(qV_{BC}/kT)-1 \right] \quad (4.27) \]

and

\[ I_C = I_2 \left[ \exp(qV_{BE}/kT) \right] - I_1 \left[ \exp(qV_{BC}/kT)-1 \right] \quad (4.28) \]

where

\[ I_1 = \frac{qAD e n_{Bo}}{L_e \sinh \frac{w}{L_e}} \cosh \frac{w}{L_e} \quad (4.29) \]

and

\[ I_2 = \frac{qAD e n_{Bo}}{L_e \sinh \frac{w}{L_e}} \quad (4.30) \]

A comparison with the Ebers Moll equations:

\[ I_E = -I_{es} \left[ \exp(qV_{BE}/kT)-1 \right] + \alpha I_{cs} \left[ \exp(qV_{BC}/kT)-1 \right] \quad (4.31) \]
\[ I_C = \alpha N I_{es} \left[ \exp\left(\frac{qV_{BE}}{kT}-1\right) - I_{cs} \left[ \exp\left(\frac{qV_{BC}}{kT}-1\right) \right] \right] \quad (4.32) \]

shows that:

\[ I_l = I_{es} = I_{cs}. \quad (4.33) \]

With \( V_{BC} = 0 \) in Equation (4.31) and \( V_{BE} = 0 \) in Equation (4.32) the equations for \( I_E \) and \( I_C \) become:

\[ I_E = -I_{es} \left[ \exp\left(\frac{qV_{BE}}{kT}-1\right) \right] \quad (4.34) \]

and

\[ I_C = -I_{cs} \left[ \exp\left(\frac{qV_{BC}}{kT}-1\right) \right]. \quad (4.35) \]

**B. Charge Stores In The Neutral Regions**

Minority carrier charge storage occurs primarily in the neutral portions of the transistor. The collector and emitter currents are proportional to the gradient of the excess-carrier distribution. A plot of excess minority-carrier concentration for a base of width \( w \) is shown in Figure 9 for an NPN transistor. An excess of "forward" minority-carrier charge (electron charge), \( q_F \), is set up in the neutral base region with
a forward biased emitter-base junction and the collector-base junction at zero volts as illustrated in Figure 9a. Similarly, as shown in Figure 9b, there is a "reverse" excess minority-carrier charge \( q_R \), where the collector-base junction is forward biased and the emitter-base junction is at zero volts.

The time rates of change of the terminal-pair voltages and terminal currents are assumed small enough for the internal base-region charge distribution to change as a succession of static distributions. Using Equation (4.8) and assuming no recombination, the collector and emitter currents are found to be:

\[
I = -I_c = I_E = -qAD_e \left( \frac{-n'(0)}{w} \right) \tag{4.36}
\]

where \( n'(0) \) is the injected excess electron concentration at the space-charge layer boundary.

The total excess charge, \( Q_B \), is the area of the triangle and may be found by integrating across the base giving:

\[
Q_B = qA \int_0^w n_B(x)dx \tag{4.37}
\]

which yields:
A factor, \( \tau \), relating the current and charge is given as:

\[
\tau = \frac{Q_B}{I}
\]  

(4.39)

with \( \tau \) having the dimensions of time. To find an expression for \( \tau \) in terms of parameters of the transistor structure, Equation (4.36) and Equation (4.38) are substituted into Equation (4.39). This results in

\[
\tau = \frac{w^2}{2D_e}.
\]  

(4.40)

Applying this to both the forward and reverse injection of the NPN transistor of Figure 9, assuming a uniform doping profile, both the forward and reverse transit times are obtained:

\[
\tau_F = \tau_R = \frac{w^2}{2D_e}.
\]  

(4.41)

C. Charge Stores In The Space Charge Region

There is a dipole layer of charge that straddles the plane at which the impurity concentration
changes. The electrostatic potential drop across the space charge layer determines the amount of charge in either half of the space charge layer. This results in a transition capacitance \(^{(14,15)}\) defined as:

\[ C_T = \frac{dQ_j}{dV_j}. \]  

(4.42)

The voltage drop, \( V_j \), is equal to the contact potential, \( \psi_0 \), under equilibrium conditions and for an applied voltage, \( V_{app} \), it becomes:

\[ V_j = \psi_0 - V_{app}. \]  

(4.43)

The depletion approximation can be used for the diffused junctions of the I\(^2\)L structure being studied. The impurity distribution is assumed to be linearly graded with the depletion layer spreading equally in both directions to a width \( w \) as shown in Figure 10.

By evaluating the charge at \( x = w/2 \), the charge in either half of the depletion layer can be written as:

\[ Q_j = Aq \frac{w}{2} \left( \frac{N_D - N_A}{2} \right). \]  

(4.44)
where $A$ is the cross-sectional area. The carrier concentration is related to the grade constant, $a$, by:

$$N_D - N_A = ax \quad (4.45)$$

which when substituted in Equation (4.44) results in:

$$Q_j = \frac{Aqaw^2}{8}. \quad (4.46)$$

By using Poisson's equation, the junction voltage, $V_j$, may be expressed in terms of carrier concentrations:

$$\frac{\partial E}{\partial x} = \frac{qp(x)}{\varepsilon_s} \quad (4.47)$$

where $E$ is the electric field in the junction, $p(x)$ is the charge density, and $\varepsilon_s$ is the dielectric constant of silicon. Due to the linear grade of the impurities, the net charge density will also be a linear function:

$$p(x) = ax. \quad (4.48)$$

An expression for $E(x)$ can now be found by substituting
Equation (4.48) into Equation (4.47) and integrating from \(-w/2\) to \(x\):

\[
E(x) = -\frac{aq}{2\varepsilon_s} \left[ \left(\frac{w}{2}\right)^2 - x^2 \right]. \tag{4.49}
\]

The junction potential is related to \(E_x\) by:

\[
\frac{dV_j}{dx} = -E(x) \tag{4.50}
\]

and integrating Equation (4.50) across the entire depletion region gives the total junction voltage:

\[
V_j = \frac{qaw^3}{12\varepsilon_s}. \tag{4.51}
\]

To obtain an equation relating the charge to the junction voltage, Equation (4.51) is solved for \(w\) and substituted into Equation (4.46) resulting in:

\[
Q_j = A\left(\frac{9qaw^2}{32\varepsilon_s}\right)^{1/3} V_j^{2/3}. \tag{4.52}
\]

Using the definition of transition capacitance as given in Equation (4.42), the derivative of \(Q_j\) with respect to \(V_j\), the transition capacitance is found to be:
\[ C_T = A\left(\frac{9qac^2}{32}\right)^{1/3} (V_j)^{-1/3}. \]  \hspace{1cm} (4.53)

Charge and voltage can be related directly from Equation (4.52) by defining a parameter \( K \):

\[ K = A\left(\frac{9qac^2}{32}\right)^{1/3} \hspace{1cm} (4.54) \]

such that

\[ Q_j = K(V_j)^{2/3}. \hspace{1cm} (4.55) \]

By substituting Equation (4.54) into Equation (4.53), \( K \) can also be used to relate the capacitance to the junction voltage:

\[ C_T = (2/3) K(V_j)^{-1/3}. \hspace{1cm} (4.56) \]

D. Gain

The transistor gain is not an intrinsic part of the charge control model, but its theoretical development will be included because of its importance in the operation of the \( I^2L \) gate.

The ratio of the collector current to the base current is defined as the short-circuit common-emitter...
current gain, $\beta_F$. In Figure 11 the currents of an NPN transistor are shown.\(^{(12)}\)

The base current results from the flow of the majority-carrier holes in the base region and is comprised of two components. The first of these components are the holes that are injected back into the emitter. For an emitter that is several diffusion lengths wide, this current is:

$$I_{BE} = \frac{qAD_h p_n}{L_h} [\exp(qV_{BE}/kT)-1] \quad (4.57)$$

where $D_h$ is the hole diffusion constant in the emitter, $L_h$ is the majority-carrier diffusion length, and $p_n$ is the minority-carrier concentration in the emitter at equilibrium. The second component of base current is due to holes recombining in the base. This current is proportional to the total number of excess carriers in the base and can be written as

$$I_{RB} = \frac{Q_B}{\tau_B} \quad (4.58)$$

where $Q_B$ is as defined in Equation (4.38) and $\tau_B$ is the minority carrier lifetime in the base. When the transistor is operated in the active region the current becomes:
\[ I_{RB} = \frac{Q_F}{\tau_B} [\exp(qV_{BE}/kT) - 1]. \quad (4.59) \]

The gain of the transistor can now be written as:

\[ \beta = \frac{I_C}{I_B} = \frac{I_C}{I_{BE} + I_{RB}}. \quad (4.60) \]

The collector current can be written as:

\[ I_C = \frac{qAD_e n_{b0}}{w} [\exp(qV_{BE}/kT) - 1] \quad (4.61) \]

and a general expression for the transistor gain results from the substitution of Equations (4.57), (4.59), and (4.61) into (4.60);

\[ \beta = \frac{qAD_e n_{b0}}{w} \frac{1}{\frac{qAD_h p_{no}}{L_h} + \frac{Q_F}{\tau_B}}. \quad (4.62) \]

E. Composite Model

Now that all of the necessary charge-controlled parameters have been defined, a model must be formulated which utilizes these parameters. The NPN transistor
model shown in Figure 12 and the PNP transistor model shown in Figure 13 follow the approach used by Searle.  

The nonlinear dependence of the current on the applied voltage is controlled by the emitter and collector diodes through the diode equation:

\[ I = I_S \left[ \exp\left(\frac{qV_j}{kT}\right)-1 \right]. \]  

(4.63)

Nonlinear capacitors are used to hold the excess charge storage, \( q_F \) and \( q_R \), which control the dependent current generators \( (q_F/\tau_F \) and \( q_R/\tau_R \), respectively. Finally, the charge in the junction space-charge layer, \( Q_{je} \) and \( Q_{jc} \), are represented by nonlinear capacitors across each junction.

As a final step, the transistor models must now be applied to the oxide isolated substrate fed \( I^2L \) gate. A composite gate model using these models is shown in Figure 14. Noting that the emitter-base junction of the NPN is also the base-collector junction of the PNP, only a single parameter, \( Q_{js} \), is required for the junction charge storage. All other parameters relate directly to the individual characteristics of either the NPN or PNP device and must be modeled separately.
V. MEASUREMENTS

This section deals with the measurement of the parameters needed for the charge-control model of the oxide isolated substrate fed $I^2L$ gate. A description of the measurement techniques is given and the results are tabulated in Table II. All data was taken with a wafer temperature of 25°C.

The cell used for analysis purposes, using 5μ design rules, is shown in Figure 15. It is a two output cell with a Schottky diode contact on each output. The total cell dimension, determined by the buried layer, is 39μ by 58μ. The outdiffusion of the buried layer will cause a reduction in the size of the PNP, approximately 2.5μ per edge, to 45μ². The size of the Schottky contacts on the outputs will also decrease due to the lateral growth of the oxide isolation, approximately 2μ per edge, to 32μ² or less, depending on the alignment of the contact window to the oxide isolation.

A. Gain

The NPN transistor in a standard $I^2L$ gate is operated in the inverse direction, which results in a low gain (in the range of 2 to 10), limiting the drive capability. In the oxide isolated substrate fed $I^2L$ cell, the NPN transistor is optimized for upward operation and, therefore, a higher gain is expected.

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The gain measurement was made using the test circuit shown in Figure 16. The Keithley Model 225 current source was used to vary the emitter current with the Keithley 615 Digital Electrometer being used to measure the base current, collector current, and base-emitter voltage. The gain was calculated according to:

\[ \beta_F = \frac{I_E}{I_B} - 1 \]  

The gain of the NPN transistor was measured on a separate NPN transistor on the same chip as the \( I^2L \) cell. This transistor has the same dimensions as the NPN transistor in the \( I^2L \) cell but eliminates the effects of the PNP transistor. The reverse gain was also measured on the separate NPN transistor in the same manner as the forward gain, except the emitter and collector leads are reversed. The forward and reverse gains, for an emitter current of 30 \( \mu \)A, were found to be 166 and 147, respectively. A plot of \( \beta_F \) and \( \beta_R \) versus \( I_C \) is shown in Figure 17 for the NPN transistor.

A separate PNP transistor was also made, but it was smaller than the one used in the cell. Thus, some form of scaling is required to obtain the value...
of gain for the PNP in the cell. The current gain of the transistor is given as:

$$\alpha_F' = \frac{I_C'}{I_C + I_B'}$$  \hspace{1cm} (5.2)

where the prime is used to denote the PNP transistor. The value of $\alpha_F'$ is also proportional to the ratio of the vertical PNP transistor active area to the total buried layer-to-substrate junction area:

$$\alpha_F' \propto \frac{A_{PNP}}{A_{total}}.$$  \hspace{1cm} (5.3)

The product of the reciprocal of this area ratio with $\alpha_F'$ will give a scale factor, C, which will allow $\alpha_F'$ to be scaled for various device geometries, i.e.:

$$C = \alpha_F' \frac{A_{total}}{A_{PNP}}.$$  \hspace{1cm} (5.4)

The value of C was found to be 2.4 on two different PNP structures. The scaled value of $\alpha_F'$ resulted in a value of 0.085 for the value of $\alpha_F'$ of the PNP transistor in the cell. The common emitter current gain can be related to the common base current gain by:
\[ \beta = \frac{\alpha}{1-\alpha} \quad (5.5) \]

The value of \( \alpha_R \) will be found in conjunction with the measurement of \( I_{es} \) and \( I_{cs} \), which is discussed in the next section.

B. \( I_{es}, I_{cs} \)

The values of the saturation currents, \( I_{es} \) and \( I_{cs} \), cannot be measured directly. An indirect method can be used which takes advantage of the relationship between current, junction voltage, and \( \alpha_F I_{es} \) or \( \alpha_R I_{cs} \) as expressed by:

\[ I_E = \alpha_R I_{cs} \left[ \exp \left( \frac{qV_{BC}}{kT} \right) - 1 \right]; \quad V_{BE} = 0 \quad (5.6) \]

\[ I_C = \alpha_F I_{es} \left[ \exp \left( \frac{qV_{BE}}{kT} \right) - 1 \right]; \quad V_{BC} = 0. \quad (5.7) \]

If the junctions are under forward bias such that \( \exp \left( \frac{qV}{kt} \right) \gg 1 \), Equations (5.6) and (5.7) reduce to:

\[ \alpha_R I_{cs} = I_E \left[ \exp \left( -\frac{qV_{BC}}{kT} \right) \right]; \quad V_{BE} = 0 \quad (5.8) \]

\[ \alpha_F I_{es} = I_C \left[ \exp \left( -\frac{qV_{BE}}{kT} \right) \right]; \quad V_{BC} = 0. \quad (5.9) \]
Using Equation (5.9) it can be seen that a plot of log $I_C$ vs. $V_{BE}$ will result in a straight line whose intercept is $\alpha_F I_{es}$. A typical curve for the test gate is shown in Figure 16. This curve demonstrates the linear relationship between log $I_C$ and $V_{BE}$ permitting the extrapolation to $V_{BE} = 0$, resulting in a value for $\alpha_F I_{es}$. At higher currents the experimental curve departs from the straight line due to the effects of ohmic resistances and high-level injection. A disadvantage of graphical extrapolation is that the extrapolation takes place over many magnitudes of current, where a small graphical error can cause a large error in saturation current. Therefore, an arithmetic extrapolation is preferred using data points picked from a linear portion of the curve. Dividing $\alpha_F I_{es}$ by the value of $\alpha_F$ measured in the previous section results in a value for $I_{es}$. The test circuit used for obtaining $I_{es}$ is the same as that used for measuring gain, Figure 16. A value of $3.085E-16A$ was found for $I_{es}$ of the NPN transistor from measurements of the $I^2L$ cell. The value of $I_{cs}$ can now be determined by using the reciprocity relationship (17):

$$\alpha_F I_{es} = \alpha_R I_{cs} .$$  

(5.10)
The value of $I_{cs}$ for the NPN transistor was $3.090E-16A$.

The value of $I'_{cs}$ for the PNP transistor was found in the same manner as for the NPN transistor, resulting in a value of $10.3E-17A$. When measuring $I'_{cs}$ in the $I^2L$ cell it should be remembered that the collector of the PNP is in common with the base of the NPN transistor on the input lead of the cell. The input current can be written as the sum of the NPN base current and the PNP collector current:

$$I_{IN} = (1-\alpha_F) I_{es} \left[ \exp \left( \frac{qV_{BE}}{kT} \right) \right] + I'_{cs} \left[ \exp \left( \frac{qV_{BC}}{kT} \right) \right]$$

Assuming $\alpha_F \approx 1$ for the NPN transistor, which was found to be true for this structure, Equation (5.11) reduces to:

$$I'_{cs} = I_{IN} \left[ \exp \left( -\frac{qV_{BC}}{kT} \right) \right]$$

(5.12)

which allows one to use the approach used to find $I_{es}$ of the NPN transistor, resulting in a value of $1.46E-17A$ for $I'_{cs}$.

Finally, the value of $\alpha_R$ can now be found by again applying the reciprocity relationship, Equation
(5.10), since the other three parameters have already been determined. The value of $\alpha_R$ was found to be 0.602.

C. $\tau_F$, $\tau_R$

The value of $\tau_F$ is obtained from its relationship with $f_T$, the transistor's unity-gain bandwidth. This represents the frequency at which the common-emitter small-signal current gain, $\beta(f)$, becomes equal to one. Again, the separate NPN transistor was measured, eliminating the effects of the PNP transistor contained in the cell. First, a plot of $(2\pi f_T)^{-1}$ vs. $I_C^{-1}$ or $I_E^{-1}$ (for $\tau_F$ and $\tau_R$, respectively) is made as shown in Figure 19 for the NPN transistor. The decrease in $f_T$ at high currents is caused by an increase in $\tau_F$ at high currents, while the decrease in $f_T$ at low currents is caused by the junction capacitances $C_{TE}$ and $C_{TC}$. The intercept of the extrapolated straight line portion of the curve, at $I_C^{-1} = 0$, is called $f_A^{-1}$ and is related to $\tau_F$ by:

$$\tau_F = (2\pi f_A)^{-1}. \quad (5.13)$$

The value of $f_T$ can be measured using the method devised by Pritchett. For non-microwave applications, $\beta(f)$ can be modeled as a single pole function of frequency according to:
\[ \beta(f) = \frac{\beta_0}{1 + j \frac{f}{f_\beta}} \] (5.14)

where \( \beta_0 \) is the low frequency small-signal current gain and \( f_\beta \) is the pole frequency.

Defining \( f_T \) in terms of the magnitude of \( \beta(f) \) and \( \beta_0 \) for \( f \neq f_T \) yields:

\[ f_T = \frac{f|\beta|}{\sqrt{1 - 1/\beta_0^2}} \] (5.15)

\[ \sqrt{1 - \frac{\beta^2}{\beta_0^2}} \]

The task now is to measure the magnitude of \( \beta \) at a frequency greater than \( f_\beta \), which is given by:

\[ f_\beta = \frac{f_T}{\sqrt{\beta_0^2 - 1}} \] (5.16)

This is easier than measuring at a frequency near \( f_T \) which is required in other measuring techniques.

An arrangement of a current source and load such as that shown in Figure 20 can be used to measure \( \beta \) in the 20 MHz to 200 MHz range. This RLC network is a current source at resonance with a shunt impedance of \( L/RC \). The parasitics of the test fixture are included in the RLC model and their effects are canceled out at resonance.
The test circuit used, Figure 21, was built directly on a probe card to have the critical parts of the circuit as close as possible to the device being measured, thus reducing parasitic inductance and capacitance.

First, the test circuit is calibrated by taking the probes out of contact and detecting the resonance of the RLC network by tuning for a null in the voltage at TP1. Next, a shunt is inserted between TP2 and TP3 and the reference voltage, $V_2(\text{REF})$, is measured at TP2. Finally, the transistor is reconnected and $V_2$ is again measured where:

$$ |\beta| = \frac{V_2}{V_2(\text{REF})}. \quad (5.17) $$

Once $|\beta|$ has been determined, Equation (5.15) can be used to determine $f_T$. Using this procedure a value of 0.521E-9 sec. was measured for $\tau_P$ of the NPN transistor.

If the value of inverse beta, $\beta_R$, is significantly greater than one, the value of $\tau_R$ can be obtained in the same way as $\tau_P$, but with the emitter and collector terminals interchanged. Since the value of $\beta_R$ is large for this structure, the value of $\tau_R$ was measured to be 1.25E-9 sec. using this method.

Measurement of $\tau_F^*$ and $\tau_R^*$ for the PNP transistor in the $I^2L$ cell could not be made directly because of the
NPN transistor's effects and also because of the low PNP transistor gain. However, if the cell is considered as an NPN transistor, its emitter time constant, \( \tau_{NC} \), is an average of \( \tau_F \) and \( \tau_R \) weighted by the saturation currents, \( I_{es} \) and \( I_{cs} \), i.e.:

\[
\tau_{NC} = \frac{I_{es} \tau_F + I_{cs} \tau_R}{I_{es} + I_{cs}}.
\]  

(5.18)

Solving for \( \tau_R \) results in:

\[
\tau_R = \frac{(I_{es} + I_{cs}) \tau_{NC} - I_{es} \tau_F}{I_{cs}}.
\]  

(5.19)

The resulting value of \( \tau_R \) was 18.2E-9 sec. The value of \( \tau_F \) was assumed to be equal to \( \tau_R \) and should have little effect on the cell performance since the emitter-base junction of the PNP transistor is not switching.

D. \( K_e, K_c \)

The emitter-base and collector-base junction capacitances are related to the applied voltages by the parameters \( K_e \) and \( K_c \) according to:

\[
C_{TE} = \frac{2}{3} K_e (V_{je})^{-1/3}
\]  

(5.20)

\[
C_{TC} = \frac{2}{3} K_c (V_{jc})^{-1/3}
\]  

(5.21)
where $V_j$ is related to the applied voltage, $V_{app}$, and the contact potential, $\psi_0$, by:

$$V_j = \psi_0 - V_{app}.$$  \hfill (5.22)

A Boonton Model 75 Capacitance Bridge was used to make the capacitance measurements, being careful to null out all the stray capacitances. Once the capacitance values have been measured, the values of $K_e$ and $K_c$ can be determined from Equations (5.20) and (5.21). A characteristic curve obtained for the common junction of the NPN transistor and the PNP transistor is shown in Figure 22.

The emitter-base and collector-base junction charges are also related to the applied voltage by the parameters $K_e$ and $K_c$ according to:

$$Q_{je} = K_e(V_{je})^{2/3}$$  \hfill (5.23)

$$Q_{je} = K_c(V_{jc})^{2/3}. \hfill (5.24)$$

For the NPN transistor the measured values of $C_{TC}$ and $C_{TE}$ at zero bias were $0.020E-12F$ and $0.393E-12F$, respectively. The value of $C_{TC}$ is very small due to the small collector
area inherent with the updiffused structure. There is also no collector-to-substrate capacitance for this structure. Since $C_{TE}$ of the NPN transistor is the same as $C_{TC}$ of the PNP transistor, only $C_{TE}$ had to be measured for the PNP transistor and was found to be $1.64E-12F$ at zero bias.

E. **Schottky Diode**

Since the Schottky diode is formed by making contact to an isolated N$^+$ doped collector output, a direct measurement of the diode is impossible. A type 576 Tektronix curve tracer was used to display $I_C$ vs. $V_{CE}$ for the NPN transistor. With a small base drive, all the voltage drop was assumed to be across the Schottky diode. The current at this point was extrapolated back to zero voltage drop across the diode, resulting in a value of $2.36E-14A$ for $I_S$ of the diode.

F. **Power-Delay Product**

The efficiency of a transistor can be expressed in terms of its power-delay product and is mentioned here due to its importance in evaluating the merits of the oxide isolated substrate fed $I^2L$ gate. As the power-delay product decreases, the amount of power required to attain a given propagation delay is decreased.

The power-delay product was measured on a twenty-five stage ring oscillator contained on the
same chip with the test gate. The period of oscillation of the ring oscillator is fifty times the average propagation delay time of a single gate and the power consumed is twenty-five times the average gate dissipation. A plot of propagation delay vs. power dissipation is shown in Figure 23, displaying a power-delay product less than 1.0 pJ/volt. At high current levels the curve becomes nonlinear because the diffusion capacitance becomes significant.
VI. SIMULATION

In this section a comparison will be made between the speed obtained from the simulation of the charge-control model to the speed obtained from measurements of the ring oscillator. The program used for the circuit simulations is SPICE. (19)

For the simulation, seven $I^2L$ cells were connected in cascade as shown in Figure 24. Each cell represents a two output $I^2L$ cell, using the model shown in Figure 14, with a Schottky diode connected to the outputs. One output was connected to the input of the following cell while the second output was connected through 100 MΩ to $V_{CC}$ to represent the floating output of the ring oscillator. A voltage ramp was applied to the input and the transient response was measured at the output nodes of cell 4 and cell 6. At the output of cell 4, the effect of the input ramp was insignificant. Taking half the time between the two responses gives the average rise and fall time for one cell. By varying the emitter current of the PNP transistor in the cells, a power-delay curve can be obtained. The power-delay results of the simulation are plotted on the same graph as those of the ring oscillator, Figure 23, and show very good agreement. A delay of 76 ns was obtained for 12 μwatts of power per cell. At an increased power of
200 μwatts per cell the delay reduced to 10 nsec. To verify the earlier assumption that $\tau_R'$ of the PNP would have little effect; its value was varied from 1.0 nsec to 25 nsec, resulting in no change in the delay time of the cell.

A reduction in the reverse transit time of the PNP transistor would increase the speed of the cell. The time constant of the PNP collector, $\tau_R'$, is given by the stored electrons and holes associated with the electron and hole currents ($I_e$ and $I_h$, respectively) shown in Figure 25 and can be written as the weighted average of the associated electron and hole transit times ($\tau_e$ and $\tau_h$, respectively), i.e.:

$$\tau_R' = \frac{I_e \tau_e + I_h \tau_h}{I_e + I_h}.$$  \hspace{1cm} (6.1)

The reverse gain of the PNP transistor can be written as:

$$\beta_R' = \frac{I_h}{I_e}.$$  \hspace{1cm} (6.2)

which allows Equation (6.1) to be reduced to:

$$\tau_R' = \frac{\tau_e + \beta_R' \tau_h}{1 + \beta_R'}.$$  \hspace{1cm} (6.3)
The value of $\tau_h$ can be approximated using Equation (4.41), giving a value of approximately 1 nsec for this structure. Substitution of this value of $\tau_h$ and the measured values of $\tau_R^*$ and $\beta_R^*$ into Equation (6.3) gives a value of 44 nsec for $\tau$. Thus, if the hole current could be increased to make the $I_h \tau_h$ term dominate in Equation (6.1), the value of reverse transit time would decrease. The value of hole current is given by:

$$I_h = \frac{qD_n^2}{w} \left[ \exp \left( \frac{qV_{CB}}{kT} \right) \int_0^{N_D(x)} dx \right].$$

(6.4)

This shows that decreasing the impurity concentration in the base region would increase the hole current. Another significant improvement in the cell would be to increase the power efficiency of the PNP transistor by increasing its very low value of gain.

To implement these improvements in the simulation, the value of $I_{cs}^*$ of the PNP transistor was increased. The value of $I_{cs}^*$ must remain significantly smaller than the value of $I_{es}$ of the NPN transistor, otherwise current would be robbed from the NPN transistor, degrading the gain performance of the $I^2L$ cell.
To implement the increase of $I'_{cs}$ in the model and find the corresponding value of $\tau_R$, other model parameters will have to be adjusted from the measured values. Assuming that the only change is a reduction of the Gummel number in the PNP and defining $I'_{s}$ as

$$I'_{s} = \alpha'_{F} I'_{es} = \alpha'_{R} I'_{cs} \quad (6.5)$$

a relationship between the measured values ($\beta_{Fm}'$ and $I'_{sm}$) and new values of these parameters ($\beta_{F}'$ and $I'_{s}$, respectively) can be written as:

$$\frac{\beta_{F}'}{I'_{s}} = \frac{\beta_{Fm}'}{I'_{sm}} \quad (6.6)$$

Similarly,

$$\frac{\beta_{R}'}{I'_{s}} = \frac{\beta_{Rm}'}{I'_{sm}} \quad (6.7)$$

Solving Equation (6.7) for $\beta_{R}'$ and substituting for $I'_{s}$ using Equation (6.5) results in an equation which allows the new value of $\beta_{R}'$ to be found.

$$\beta_{R}' = \frac{\beta_{Rm}'}{I'_{sm}} I'_{cs} - 1 \quad (6.8)$$
Once $\beta_R^-$ is known the value of $I_s^-$ can be calculated using Equation (6.7), a new value of $\beta_F^-$ can be calculated using Equation (6.8), and, finally, a new value of $\tau_R^-$ can be calculated using Equation (6.3).

The best power-delay product for the cell occurred when $I_{cs}^-$ was approximately $1/5$ of $I_{es}^-$. A plot of the power-delay curve for the increased value of $I_{cs}^-$ is shown in Figure 26. A substantial improvement can be seen in the power efficiency with a delay of approximately 21 nsec at 12 μwatts of power per cell, and at an increased power of 100 μwatts per cell the delay decreased to 8 nsec.
VII. CONCLUSIONS

Oxide isolated substrate fed integrated injection logic has been shown to be an effective extension of the conventional I^2L structure to achieve higher packing density and increased speed required for future large-scale integrated circuits. The low currents required for operation result in a power-delay product much smaller than the best state of the art MOS or bipolar logic forms.

The evolution to oxide isolated substrate fed I^2L has been given, describing the various improvements over the conventional I^2L cell. A charge-control model was introduced to relate the physical parameters of the cell to its actual operation. Fabricated devices, containing Schottky diodes on the outputs, were measured to obtain the parameters required for the charge-control model. The measurement techniques used to obtain the parameters were also discussed. The forward and reverse values of gain for the NPN transistor were well above 100 over many magnitudes of collector current. This greatly reduces the fanout problems encountered with conventional I^2L. The gain of the PNP transistor, measured in the available devices, was very low (less than 0.1) and the value of its collector time constant was large (18.2 nsec). These results arise from less than
optimum fabrication conditions that yield a very large Gummel number for the vertical PNP transistor. The measured models, therefore, show a larger than expected power-delay product.

A computer simulation of the cell was made using the charge-control model and the measured parameters. A power-delay curve was made from the simulation and compared to a power-delay curve made from measurements of a ring oscillator on the same chip as the cell, resulting in very close agreement. At low power the cell delay was 76 nsec at 12 μwatts of power per cell. Increasing the power to 200 μwatts per cell decreased the delay to 10 nsec.

The gain and the reverse transit time of the PNP transistor can be improved by reducing the impurity concentration in the base region of the PNP. The basic limitation is that the value of $I_{cs}$ of the PNP transistor must be significantly smaller than the $I_{es}$ of the NPN transistor or the operation of the latter, and subsequently the gate, will be degraded. A near optimum value of $I_{cs}$ was found to be $1/5 I_{es}$. An adjustment of the parameters in the model to reflect this change resulted in a cell delay of approximately 21 nsec at 12 μwatts of power per cell. At an increased power of 100 μwatts per cell the delay reduced to 8 nsec.
TABLE I

PERFORMANCE OF VARIOUS FORMS OF I$^2$L

<table>
<thead>
<tr>
<th>I$^2$L Form</th>
<th>Power-Delay Product (pJ)</th>
<th>Cell Density (cells/mm²)</th>
<th>Intrinsic Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional I$^2$L</td>
<td>2.0</td>
<td>40-80</td>
<td>25-35</td>
</tr>
<tr>
<td>(10 µm tolerance)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conventional I$^2$L</td>
<td>1.0</td>
<td>80-160</td>
<td>20-30</td>
</tr>
<tr>
<td>(5 µm tolerance)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Schottky I$^2$L</td>
<td>0.3</td>
<td>80-160</td>
<td>10-20</td>
</tr>
<tr>
<td>(5 µm tolerance)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Substrate Fed I$^2$L</td>
<td>1.0</td>
<td>120-240</td>
<td>20-30</td>
</tr>
<tr>
<td>(5 µm tolerance)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectrically Isolated I$^2$L</td>
<td>0.1</td>
<td>200-300</td>
<td>5-10</td>
</tr>
<tr>
<td>(5 µm tolerance)</td>
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</tr>
</tbody>
</table>
### TABLE II

**MEASURED PARAMETERS OF THE OXIDE ISOLATED SUBSTRATE FED I^2L CELL**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNITS</th>
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<tbody>
<tr>
<td><strong>NPN:</strong></td>
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<td></td>
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<tr>
<td>$\alpha_F$</td>
<td>0.994</td>
<td></td>
</tr>
<tr>
<td>$\alpha_R$</td>
<td>0.993</td>
<td></td>
</tr>
<tr>
<td>$I_{es}$</td>
<td>3.085E-16</td>
<td>AMPS</td>
</tr>
<tr>
<td>$I_{cs}$</td>
<td>3.090E-16</td>
<td>AMPS</td>
</tr>
<tr>
<td>$\tau_F$</td>
<td>0.521E-9</td>
<td>SECONDS</td>
</tr>
<tr>
<td>$\tau_R$</td>
<td>1.25E-9</td>
<td>SECONDS</td>
</tr>
<tr>
<td>$C_{TC}$</td>
<td>0.020E-12</td>
<td>FARADS</td>
</tr>
<tr>
<td>$C_{TE}$</td>
<td>0.393E-12</td>
<td>FARADS</td>
</tr>
<tr>
<td><strong>PNP:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\alpha_F$</td>
<td>0.085</td>
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</tr>
<tr>
<td>$\alpha_R$</td>
<td>0.602</td>
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<tr>
<td>$I_{es}$</td>
<td>10.3E-17</td>
<td>AMPS</td>
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<tr>
<td>$I_{cs}$</td>
<td>1.46E-17</td>
<td>AMPS</td>
</tr>
<tr>
<td>$\tau_F$</td>
<td>18.2E-9</td>
<td>SECONDS</td>
</tr>
<tr>
<td>$\tau_R$</td>
<td>18.2E-9</td>
<td>SECONDS</td>
</tr>
<tr>
<td>$C_{TE}$</td>
<td>1.64E-12</td>
<td>FARADS</td>
</tr>
</tbody>
</table>
LOGIC CIRCUIT EQUIVALENT
OF AN I²L CELL

FIGURE 1
TOPOLOGY AND CROSS SECTION OF A CONVENTIONAL $I^2$L CELL

FIGURE 2
MULTIPLE OUTPUT I\textsuperscript{2}L CELL
CONNECTED AS NAND LOGIC

FIGURE 3
LAYOUT OF A D-TYPE FLIP FLOP USING CONVENTIONAL I^2L CELLS

FIGURE 5
TOPOLOGY AND CROSS SECTION OF AN OXIDE ISOLATED SUBSTRATE FED I$^2$L CELL

FIGURE 6
DOPING PROFILES OF THE NPN TRANSISTOR AND THE PNP TRANSISTOR OF THE OXIDE ISOLATED SUBSTRATE FED I²L CELL

FIGURE 7
LAYOUT OF A D-TYPE FLIP FLOP USING SUBSTRATE FED OXIDE ISOLATED $I^2L$ CELLS

FIGURE 8
COMPONENTS OF EXCESS MINORITY-CARRIER CHARGES SET UP IN THE BASE REGION OF AN NPN TRANSISTOR FOR FORWARD AND REVERSE INJECTION

**FIGURE 9**
IMPURITY DISTRIBUTION FOR A LINEARLY GRADED JUNCTION IN THERMAL EQUILIBRIUM

FIGURE 10
CURRENT FLOW IN AN NPN TRANSISTOR

FIGURE 11
NPN CHARGE - CONTROL MODEL

FIGURE 12
PNP CHARGE - CONTROL MODEL

FIGURE 13
I^2L COMPOSITE MODEL

FIGURE 14
TOPOLOGY OF CELL USED FOR CHARACTERIZATION

FIGURE 15
TEST CIRCUIT
USED FOR MEASURING GAIN

FIGURE 16
FORWARD AND REVERSE GAIN VS COLLECTOR CURRENT
FOR THE NPN TRANSISTOR OF THE I^2L CELL

FIGURE 17
COLLECTOR CURRENT VS BASE-EMITTER VOLTAGE FOR THE NPN TRANSISTOR OF THE I₂L CELL

FIGURE 18
$\frac{1}{2\pi f_t}$ VS $\frac{1}{I_E}$ MEASURED AT 40 MHz

FOR THE NPN TRANSISTOR OF THE I$^2$L CELL

FIGURE 19
MEASUREMENT TECHNIQUE FOR FINDING $|\beta|$  

FIGURE 20
CIRCUIT FOR MEASURING $|\beta|$  

FIGURE 21

FIGURE 22
PROPAGATION DELAY AS A FUNCTION OF POWER DISSIPATION FOR THE OXIDE-ISOLATED SUBSTRATE FED I2L CELL

O = MEASURED
Δ = SIMULATION

POWER/CELL (WATTS)
5 x 10^-9 2 x 10^-8 5 x 10^-8 10^-7 2 x 10^-7

PROPAGATION DELAY (SEC)
10^-7 5 x 10^-8 2 x 10^-8 10^-7 5 x 10^-9
MODEL USED TO MEASURE THE SIMULATED PROPAGATION DELAY OF THE OXIDE ISOLATED SUBSTRATE FED I^2L CELL
CURRENT FLOW AT THE BASE–COLLECTOR JUNCTION OF THE PNP TRANSISTOR

FIGURE 25
SIMULATION OF PROPAGATION DELAY AS A FUNCTION OF POWER DISSIPATION WITH $I_{CS} = 1/5.18$ A FOR THE OXIDE ISOLATED SUBSTRATE FET I$^2$L CELL
REFERENCES


11. D. Leenov, Professor at Lehigh University, private communication.
REFERENCES (CONT'D.)


18. R. L. Pritchett, Member of Technical Staff, Bell Telephone Laboratories, private communication.

Mr. Clarence E. Williams, Jr. was born in Troy, New York on June 9, 1946, the son of Mr. and Mrs. Clarence E. Williams. He graduated from Berlin High School, Berlin, New York in June, 1964. He received an Associate Degree in Electronic Technology from Hudson Valley Community College, Troy, New York, in June, 1966. He graduated Magna Cum Laude with a Bachelor of Science Degree in Electrical Engineering from Lafayette College in June, 1975. He is a member of Eta Kappa Nu and Tau Beta Pi. He joined Bell Laboratories, Allentown, Pennsylvania in 1966 where he was engaged in the layout and testing of linear integrated circuits. He is currently a Member of Technical Staff involved in the design of digital integrated circuits employing $I^2L$ devices. He and his wife, the former Linda J. Wittman, and their children, Lisa and Michael, reside in Whitehall, Pennsylvania.