Enhancing the models for gallium arsenide metal-semiconductor field-effect transisitors

Fadi Ahmad Abbas

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Enhancing the Models for Gallium Arsenide Metal-Semiconductor Field-Effect Transistors

by

Fadi Ahmad Abbas

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Abstract

Enhancing the Model for the GaAs MESFET

For the purpose of circuit simulation, empirical models are usually used for the GaAs MESFET. The model equations used are approximations, based on experiments, and they don't reflect the device physics. However they are used in simulation programs such as SPICE because of their simplicity and acceptable accuracy.

In this thesis, an analytical model is derived, based on a two-region description of the channel in which velocity saturation occurs in a region near the drain. The current-voltage relations are derived starting with an analysis of the Schottky junction in the MESFET, followed by derivations of the drain and the gate currents. The capacitive currents, due to the charge on the gate electrodes are then derived. Finally, an empirical model is described.

Experimental data show the extraction of the device parameters and the I-V characteristics, and a set of the I-V characteristics is computed from the analytical formulas. Measured data of the I-V characteristics are then compared to both an empirical SPICE model and the derived analytical expressions, with very good agreement between them. The derivations for capacitive currents unfortunately result in very complex analytical expressions. Hence, no comparisons between data and derived expressions for the capacitive currents was attempted.
Introduction

For the purpose of circuit simulation, several empirical models are usually used for the Gallium Arsenide MESFET. In them, the current-voltage relation is approximated by an explicit function of the terminal voltages. This relation, however, is strictly mathematical and has little to do with the physics of the device and is therefore unsuitable for use in device characterization. This paper is an attempt to develop a theoretical model that is more reliable and useful in predicting how the device performance will change when the device parameters are changed.

Because of its energy band structure, GaAs is an ideal medium for achieving remarkable speed in electronic devices and circuits. Electrons in GaAs are exceedingly light and highly mobile. The effective mass of electrons is only 7 percent that of electrons in silicon, and electron mobility in the channels of GaAs MESFETs is about an order of magnitude higher than in silicon MOSFETs. Electron velocities measured in GaAs transistor structures range up to $5 \times 10^7$ cm/s, about five times those achieved in silicon devices. Furthermore, GaAs is readily available in a semi-insulating substrate form that substantially reduces parasitic capacitances, so its potential device speeds can be fully realized in integrated circuits. This high speed, plus power dissipation that tends to be substantially lower than that of high speed silicon devices, accounts for the growing interest in GaAs.

An idealized MESFET structure is shown in Fig. 1. An active layer of n-type GaAs is grown on top of a semi-insulating GaAs substrate. Each of the drain and source electrodes makes contact with the active layer through an n+ region. A third electrode, which is the gate, is placed directly on the active layer. From consideration of the energy band diagram at the metal-semiconductor interface, we find that there is a depletion region under the gate whose height is controlled by a transverse electric field created by an
applied gate voltage $V_G$. The undepleted region is called the channel. When a positive voltage $V_D$ is applied to the drain with respect to the source, a longitudinal electric field is created that accelerates electrons in the channel from the source toward the drain. The resulting current in the channel, called the drain current, will depend on the gate voltage and the drain to source voltage.

Fig. 1 An idealized MESFET structure

Since no simple analytical models of MESFETs exist, a variety of empirical models have been implemented in different versions of SPICE. The Curtice model [1] is one of the earliest ones. It describes the I-V characteristics by taking into account transit-time effects, gate capacitance, and circuit parasitics. In the past, the JFET model was used to simulate GaAs MESFETs in SPICE and this led to inaccurate results. Later, a GaAs MESFET model was implemented in SPICE 2G.5 [2]. The Statz model [3] improved on the one implemented in SPICE 2G.5 by differentiating between gate-to-source and gate-to-drain charges. The Statz model is discussed in chapter 2. A more recent model [4] has been developed by modifying the Statz model equations so that $I_{DS}$ is more accurately represented as a function of the applied voltage.

Fig. 2 presents a schematic diagram of the circuit commonly used to represent the GaAs MESFET. The controlled current source, $I_D(V_{GS,i}, V_{DS,i})$, at the center is the key
element for the dc model. It produces a drain current that depends on the internal gate-to-source and gate-to-drain voltages, $V_{GS,i} = V_{GS} - I_D R_S$ and $V_{DS,i} = V_{DS} - I_D (R_S + R_D)$. $R_S$ and $R_D$ are source and drain parasitic resistances. The diodes represent the gate junction; the forward-bias current flow is modeled with individual Schottky barrier diodes. Time dependent effects are simulated through charge storage elements, $C_{GS}$ and $C_{GD}$.

Only one set of model equations is generally used for both depletion and enhancement type devices. The depletion mode device is normally on, allowing flow of substantial drain current. As the gate-to-source voltage is made more negative, for n-channel devices, the width of the depletion region under the metal gate increases, reducing the width of the channel through which current can flow. When the gate-to-source voltage is increased beyond pinch off, the current flow essentially stops. GaAs MESFET integrated circuits give excellent performance, but they typically require two power supplies for proper operation and they also must contain some voltage level shifting built into the logic gates to generate the negative gate voltages required for switching from positive drain voltages.

---

**Fig. 2** A simplified MESFET equivalent circuit used in SPICE [5]
Use of the enhancement mode device avoids the requirement for dual power supplies and level shifting circuitry by having slightly positive pinch off voltages. Its structure is similar to the depletion mode device, except that the implanted channel depth and the doping concentration are designed so that the built-in potential of the metal Schottky barrier gate normally cuts off the channel conduction. Thus, a small positive gate voltage (about 0.1V) must be applied for source-drain conduction to begin. Enhancement type MESFETs are restricted to very limited logic voltage swings (typically about 0.5V) because they begin to draw excessive gate currents for larger gate voltages due to forward biased gate-source and gate-drain diodes. Because the difference between voltages representing logical 0 and 1 states must be roughly 20 times the standard deviation of pinch-off (threshold) voltages to allow adequate margins for building integrated circuits, the pinch-off voltage must be uniform within 25mV. It is difficult to achieve this degree of control. An additional complication in the manufacture of enhancement type MESFETs is their need for more complex device processing than depletion type MESFETs. The problem is that the substantial depletion region at the surface between the gate and the source contact region tends to pinch off the lightly doped channel. This leads to high source resistance that degrades the transconductance. This can be avoided by modifying the fabrication process.

In the following chapter, we will describe an analytical model of the MESFET. First, we derive current-voltage relations from first principles. In addition to the drain current there is current flowing from the gate into the semiconductor when the gate voltage is sufficiently positive with respect to the voltage along the channel. A distributed model of the gate current is given, which is then simplified to one that is represented by two diodes. Then the capacitive currents, due to the charge on the gate electrode, are derived. Finally, an empirical model is described, and experiments conducted on GaAs MESFETs will be used to derive device parameters. I-V characteristics obtained from both analytical and empirical models will be compared to those obtained from measured data.
Chapter 1

Analytical Model

In this chapter, we describe a theoretical model of GaAs MESFETs. First, we derive an expression relating the height of the depletion region under the Schottky junction to the gate voltage. Then, this expression will be used in deriving the drain current. Next, we derive the gate current and the charge-voltage relations.

I) Schottky Junction Characteristics

The metal-semiconductor interface in a MESFET is a Schottky junction. The current flowing across a cross-sectional area A of a MESFET, is proportional to the doping concentration, N, and to the average velocity of the charge carriers crossing the area: \( I = N A v \); v is the electron velocity in GaAs, which is a function of the longitudinal electric field. A is the height of the channel times the width of the gate. The height of the channel is related to the height of the depletion region under the metal-semiconductor interface.

Fig. 3 shows the energy band diagram of a Schottky junction. An n-type semiconductor is assumed. At thermal equilibrium and in the absence of an applied voltage across the junction, the Fermi levels of the metal and semiconductor must line up. Since there are many unfilled energy states in the metal, electrons in the semiconductor with sufficient energy will go over to the metal and leave an equal amount of positive charge in the semiconductor side. In addition, there will be a large number of "surface states" at the surface. Additional electrons from the semiconductor bulk will fill these surface states, further increasing the amount of positive charge near the junction. A depletion region is thus formed. The height h of the region is such that the potential built up by the positive
charge is just enough to prevent further movement of electrons into the metal of surface states.

\[ qV_B \]

\[ qV_{bi} \]

**Fig. 3 Band Diagram.**

For GaAs, the number of surface states at the junction is large so that the barrier height on the metal side is approximately independent of the number of electrons absorbed in the surface state, and the barrier height \( V_B \) is said to be "pinned" to a constant. From the band diagram, we see the barrier height is related to the built-in potential \( V_{bi} \) by:

\[ -qV_B = -qV_{bi} + E_C - E_F \quad (1.1) \]

where \( E_C \) is the conduction band edge in the bulk semiconductor and \( E_F \) is the Fermi level.

### 1.1 Depletion Height and Capacitance [6]

First, for \( V_G = 0 \), in thermal equilibrium the electron and hole concentrations are given by:

\[ n = N_C e^{-(E_C - E_F)/kT} \quad (1.2) \]

\[ p = N_V e^{-(E_F - E_V)/kT} \quad (1.3) \]

where \( N_C \) and \( N_V \) are the effective densities of states for the conduction and valence bands respectively. Inside the semiconductor, \( E_C \) and \( E_V \) are governed by Poisson's equation:
\[
\frac{d^2 E_C}{dx^2} = \frac{d^2 E_V}{dx^2} = -q \frac{d^2 V}{dx^2} = \frac{\rho(x)}{\varepsilon}
\]  
(1.4)

where \( V(x) \) is the electrostatic potential, \( \rho(x) \) the space charge density, and \( \varepsilon \) the permittivity of the semiconductor.

Assume all donors and acceptors are ionized. Then the space charge density is given by:
\[
\rho(x) = q\left[N_D(x) - N_A(x) - n(x) + p(x)\right]
\]
(1.5)

where \( N_D \) and \( N_A \) are the donor and acceptor densities respectively.

For an n-type semiconductor, we assume \( N_A = 0 \) and \( p(x) = 0 \). Far away from the junction, the semiconductor is electrically neutral so that:
\[
\rho(\infty) = q(N_D - n(\infty)) = 0
\]
(1.6)

\[
n(\infty) = N_D = N_c e^{-(E_c(\infty) - E_F)/kT}
\]
(1.7)

The space charge density at any \( x \) can now be written as:
\[
\rho(x) = qN_D\left[1 - e^{-(E_c(x) - E_F)/kT}\right]
\]
(1.8)

Noting that:
\[
E_c(x) - E_c(\infty) = -qV(x)
\]
(1.9)

we find Poisson's equation to be:
\[
\frac{d^2 V}{dx^2} = -qN_D\frac{1 - e^{qV/kT}}{\varepsilon}
\]
(1.10)

with boundary conditions: \( V(\infty) = 0 \) and \( dV/dx(\infty) = 0 \)

Integrating 1.10 and imposing the boundary conditions that at \( x = \infty \), \( V = 0 \) and \( E = -dV/dx = 0 \), we get:
\[
E(x) = -\frac{2qN_D}{\varepsilon}\left[-V(x) - \frac{kT}{q}\frac{kT}{q}\exp\left(\frac{qV(x)}{kT}\right)\right]^{1/2}
\]
(1.11)

Since \( V(0) = -V_{bi} \), under zero gate bias, we get
\[
E(0) = -\frac{2qN_D}{\varepsilon}\left[V_{bi} - \frac{kT}{q}\frac{kT}{q}\exp\left(-\frac{qV_{bi}}{kT}\right)\right]^{1/2}
\]
(1.12)

If a gate bias \( V_G \) is applied across the junction with the bulk semiconductor maintained at 0V, then:
In practice, \( V_{bi} - V_G \approx kT/q \) and the exponential term can be neglected. The surface charge density \( Q_s \) is given by: \( Q_s = eE(0) \) and is negative to balance the positive charge in the depletion region.

The "differential" gate capacitance is given by:

\[
C = \frac{dQ_s}{dV_G}
\]  

(1.14)

Taking the derivative, we get:

\[
C = \left[ \frac{eqN_D}{2} \left( \frac{1}{V_{bi} - V_G - kT/q} \right) \right]^{1/2}
\]  

(1.15)

This capacitance can be regarded as the capacitance of a parallel plate capacitor with a separation \( h = e/C \). So we have:

\[
h = \left[ 2e \left( V_{bi} - V_G + kT/q \right) \right]^{1/2}
\]  

(1.16)

This equation shows that as we increase the gate bias positively, the depletion height shrinks and therefore the current will increase.

The depletion height along the channel is:

\[
h = \left[ \frac{2e}{qN_D} \left( V_{bi} - V_G + V \right) \right]^{1/2}
\]  

(1.17)

where \( V_G - V \) is the voltage across the Schottky junction, \((kT/q)\) was neglected.

Eq. (1.17) shows that as we increase the gate bias positively, the depletion height shrinks and the channel height increases, therefore, the current will increase. This expression will be used in the process of drain current derivation.

II) Drain Current Derivation

An important part of a MESFET model is the drain current for which we will now derive an expression as a function of the terminal voltages. The derivation is based on the work of [7,8,9].
Fig. 4 shows a MESFET structure. The resistivity of the semi-insulating substrate is too high compared to that of the active layer. It follows that the substrate can be regarded as a perfect insulator so that the surface charge density on the n-GaAs/GaAs interface is zero. The n+ regions will be considered as perfect conductors (very low resistivity), and the n+/n junction built-in potential is assumed to be zero. Let the voltage along the channel be V. It is a function of both x and y. However, if V varies slowly along x, we can simplify the analysis by assuming that the voltage is a function of y only so that it satisfies a one-dimensional Poisson's equation along y.

![MESFET structure diagram]

**Fig. 4 MESFET structure**

Using the expression derived in the previous chapter for h, the depletion heights at the source (hₜ) and at the drain (hₜ) are given by:

\[
h_s = \left[ \frac{2\varepsilon}{qN_D} (V_{bi} - V_{gs}) \right]^{1/2} \quad (1.18)
\]

\[
h_D = \left[ \frac{2\varepsilon}{qN_D} (V_{bi} - V_{gd}) \right]^{1/2} \quad (1.19)
\]

If the drain voltage with respect to the gate is sufficiently high (the Schottky junction is highly reverse biased near the drain) the depletion height hₜ can reach the bottom of the channel.
active layer ($h_{D_{\text{max}}} = a$). The region under the gate is totally depleted at this point. The channel is pinched-off. The pinch-off voltage is:

$$V_p = \frac{qN_D a^2}{2\varepsilon} \quad (1.20)$$

At cut-off, the threshold voltage is given by:

$$V_T = V_{b_i} - V_p = V_{b_i} - \frac{qN_D a^2}{2\varepsilon} \quad (1.21)$$

2.1 Velocity field Relation

The longitudinal electric field along the channel created by the drain-to-source voltage will accelerate the electrons towards the drain. If $n(x)$ is the electron density and $v(x)$ the average electron velocity, then the steady-state drain current is given by:

$$I_{DS} = qn(x)[a - h(x)]Wv(x) \quad (1.22)$$

where $[a-h(x)]$ is the height of the channel and $W$ is its width. We assume that the donor density is uniform and equal to $N_D$ and that the donors are completely ionized so that:

$$n(x) = N_D^+ = N_D$$

The electron velocity $v(x)$ is a function of the longitudinal electric field $E_x$. For GaAs, the steady state velocity has a peak value of about $2 \times 10^7$ cm/s and occurs at $E_x \approx 3$ kV/cm.

The velocity-field relation is shown in the figure below:

![Velocity-field relation diagram](image)

Fig. 5 Assumed velocity-field relation for the derivation of drain current
2.2 Two-Region Model

In region I, the longitudinal electric field is small compared to the transverse field. The depletion height $h(x)$ is determined by a one-dimensional Poisson's equation. In region II, the longitudinal field is no longer small and a two-dimension description of the potential is required.

The electron velocity is given by:

$$v(E) = \frac{\mu E}{1 + \frac{E}{E_p}} \quad (1.23)$$

and the drain current is:

$$I_{DS} = qN_D W \mu \frac{dV}{dx} \left[ a - \left[ \frac{2\epsilon}{qN_D} (V_{bi} - V_G + V) \right]^{1/2} \right] \quad (1.24)$$

Let $V_C$ be the channel voltage at $x=L_C$. Separating variables in the equation above, and integrating from $x=0$ to $x=L_C$ on one side and from $V=V_S$ to $V=V_C$ on the other, we get:

$$I_{DS} = \frac{I_p}{1 + \frac{V_{CS}}{E_p L_C}} \left[ \frac{V_{CS}}{V_p} + \frac{2}{3} \left[ \left( \frac{V_{bi} - V_{GS}}{V_p} \right)^{3/2} - \left( \frac{V_{bi} - V_{GC}}{V_p} \right)^{3/2} \right] \right] \quad (1.25)$$

where,

$$I_p = (qN_D)^2 a^2 \mu \frac{W L_c}{2\epsilon}$$

$$V_{CS} = V_C - V_S$$

$$V_{GC} = V_G - V_C$$

$L_C$ and $V_C$ are unknown.

Special case:

Long-channel, low-field approximation:

If the channel is long (gate length is large compared to the thickness of the active layer) and the drain voltage is low, the electric field along the channel never reaches the value $E_C$. 
In fact, if $E \ll E_p$, so that the velocity is given by $V = \mu E$, we obtain a long-channel, low-field approximation of the drain current:

$$I_{DS} = I_p \left\{ \frac{V_{GS}}{V_p} + \frac{2}{3} \left( \frac{V_{bi} - V_{GS}}{V_p} \right)^{3/2} \right\} - \left( \frac{V_{GD}}{V_p} + \frac{2}{3} \left( \frac{V_{bi} - V_{GD}}{V_p} \right)^{3/2} \right)$$

$$= f(V_{GS}) - f(V_{GD})$$

(1.26)

![Assumed field and velocity as functions of x](image)

**Fig 6** Assumed field and velocity as functions of $x$

**Region II**

Here, the electron velocity is constant at the saturation value $V_s$. At the boundary of the two regions, $V = V_C$ and the depletion height is:

$$h_c = \left[ \frac{2\varepsilon}{qN_D} (V_{bi} - V_C + V_C) \right]^{1/2}$$

(1.27)
which is assumed to be the same across the region.

The drain current is: \( I_{DS} = qN_D W V_s (a - h_c) \). It must be continuous across the boundary, so setting \( I_{DS} \) as given by eq. 1.25 to that given by the above, we get one of the two necessary expressions relating the two unknowns \( V_C \) and \( L_e \).

\[
1 - \left( \frac{V_{bi} - V_{GC}}{V_p} \right)^{1/2} = \frac{V_p}{E_C L_C} + \frac{E_p}{V_{CS}} \left\{ \frac{V_{CS}}{V_p} + \frac{2}{3} \left[ \left( \frac{V_{bi} - V_{GS}}{V_p} \right)^{3/2} - \left( \frac{V_{bi} - V_{GC}}{V_p} \right)^{3/2} \right] \right\} \quad (1.28)
\]

The second expression is obtained from solving for the potential in region II and setting its value at the drain end to the applied drain voltage. In this region, the longitudinal electric field is large and the potential \( V(x,y) \) satisfies Poisson's equation:

\[
\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = -\frac{qN_D}{\varepsilon}
\]

and the boundary conditions:

1) \( V(x,0) = V_G - V_{bi} \)

2) \( \left. \frac{\partial V}{\partial y} \right|_{y=a} = 0 \)

3) \( \left. \frac{\partial V}{\partial x} \right|_{x=L_c,y=a} = -E_x(L_c,a) = E_c \)

4) \( V(L_c^+,y) = V(L_c^-,y) \)

The first condition says that the potential along the interface of the gate and the active layer in region II is equal to the built-in potential reduced by the applied gate voltage.

The second condition says the surface charge on the boundary of the semiconductor-semi-insulating interface is zero.

The third condition requires the longitudinal field at \( x=L_c \) be continuous.

The fourth condition states that the potential across the two regions must be continuous.

To solve Poisson's equation, we decompose \( V(x,y) \) into: \( V(x,y) = V_0(x,y) + V_1(x,y) \), in which \( V_0(x,y) \) satisfies the homogeneous equation (Laplace equation) and \( V_1(x,y) \) is a particular solution of Poisson's equation. That is:

\[
\frac{\partial^2 V_0}{\partial x^2} + \frac{\partial^2 V_0}{\partial y^2} = 0 \quad (1.29)
\]
with boundary conditions:

1) \( V_0(x,0) = 0 \)

2) \( V_0(L_c,y) = 0 \)

3) \( \frac{\partial V_0}{\partial y} \bigg|_{y=a} = 0 \)

4) \( \frac{\partial V_0}{\partial x} \bigg|_{x=L_c, y=a} = E_c \)

The most general solution that satisfies eq. 1.29 and the boundary conditions 1, 2, and 3 is:

\[
V_0(x,y) = \sum_{n=1}^{\infty} A_n \sin \left( \frac{(2n-1)\pi}{2a} \right) y \sinh \left( \frac{(2n-1)\pi}{2a} \right) (x - L_c) \quad (1.30)
\]

To satisfy condition 4, we must have:

\[
\sum_{n=1}^{\infty} A_n \frac{(2n-1)\pi}{2a} = E_c \quad (1.31)
\]

But, this condition alone is not sufficient to determine the coefficients \( A_n \).

If the normal electric field along \( x=L \) is known, then \( A_n \) can be determined from the Fourier series expansion of the field there. Since this field is not known, we must look for an approximation that is self-consistent.

As explained in [7], \( A_n \) must diminish rapidly with \( n \), for otherwise, \( V_0 \) and \( E_x \) would grow exponentially along \( x \) via the sinh function. Accordingly, we assume that \( A_n=0 \) for all \( n \neq 1 \), so we get:

\[
V_0(x,y) = \frac{2a}{\pi} E_c \sin \left( \frac{\pi}{2a} \right) y \sinh \left( \frac{\pi}{2a} \right) (x - L_c) \quad (1.32)
\]

The expression found for the drain current (eq. 1.25) is not explicit in the terminal voltages and iterations need be used to compute the current value for a given set of gate, drain, and source voltages.

### III) Gate Current Derivation

In the derivation of the drain current, we have assumed that the gate voltage is sufficiently low so that the thermionic emission current across the Schottky junction is
negligible. When the gate is driven to a large positive voltage, gate current will flow. The derivation of the gate current is based on the work of [7].

To derive an expression for the gate current, consider the region under the gate in a transistor as shown in Fig. 7

\[ I_D = I_{DS} + I_{GD} \quad (1.33a) \]
\[ I_G = I_{GD} + I_{GS} \quad (1.33b) \]
\[ I_S = I_{DS} + I_{GS} \quad (1.33c) \]

Let \( V(x) \) be the channel voltage at point \( x \) taken with respect to the source.
Let \( I(x) \) be the longitudinal channel current (in the \(-x\) direction).
We assume the gate current consists of only thermionic emission current.
Let the gate current density at \( x \) be \( J_G(x) \). Then the gate current in the interval \( \Delta x \) is:
\[ \Delta I_G(x) = J_0 W A \Delta x \left[ e^{(V_{GS} - V(x))/kT} - 1 \right] \quad (1.34) \]
where \( I_0 = A R T^2 e^{-qV_0/kT} \), and \( W \) is the width of the gate.

Over the interval \([x, x+\Delta x]\), we have:

\[
I(x) = I(x+\Delta x) + \Delta I_G(x)
\]  
(1.35)

then,

\[
\frac{dI(x)}{dx} = -J_0 W \left[ e^{q(V_{os} - V(x))/kT} - 1 \right]
\]  
(1.36)

This equation says, the longitudinal current decreases along \( x \) as we move from the source to the drain. The extra current as we go from the drain to the source comes from the distributed gate current along \( x \). The longitudinal current \( I(x) \) is the drift current that depends on the electron velocity.

Using a 2-region model, we have for region I:

\[
I(x) = qN_D W \frac{\mu}{1 + \frac{1}{E_p}} \left( \frac{2e}{qN_D} \left( V_{bi} - V_{GS} + V(x) \right) \right)^{1/2}
\]  
(1.37)

\[
\frac{dV(x)}{dx} = \frac{qN_D W \mu}{\left( \frac{2e}{qN_D} \left( V_{bi} - V_{GS} + V(x) \right) \right)^{1/2}} \cdot \frac{I(x)}{E_p}
\]  
(1.38)

The two equations above form a system of differential equations in the unknowns \( I(x) \) and \( V(x) \). These equations can be solved once the boundary conditions are specified, which are: \( V(L_C) = V_C \) and \( V(0) = V_S = 0 \). \( L_C \) is the point along the channel where the electron velocity equals the saturation velocity and the longitudinal electric field reaches \( E_C \).

Let \( I_C = I(L_C) \). We assume it is given by the total longitudinal current in region II plus the total gate current in this region. That is:

\[
I_C = I_D + \int_{L_C}^{L_2} J_0 W \left[ e^{q(V_{os} - V(x))/kT} - 1 \right]
\]  
(1.39)

\[
= I_D + I_{GD}
\]
It should be noted that the drain voltage is so low that the field never reaches the value $E_C$, then there is only one region and $I_C=I_D$

\[ I(x) = I_C + \int_x^{L_C} J_0 W \left[ e^{q(V_{oa} - V(x))/kT} - 1 \right] dx \]  
(1.40)

also we have:

\[ I(x) \left( dx + \frac{1}{E_p} dV \right) = qN_D W \mu \left\{ a - \left[ \frac{2e}{qN_D} (V_{bi} - V_{GS} + V) \right] \right\} dV \]  
(1.41)

Substituting this last equation in the one before it and integrating from $x=0$ to $x=L_C$ on $dx$ and from $V=0$ to $V=V_C$ on $dV$, we get:

\[ I_C \left( L_C + \frac{V_{CS}}{E_p} \right) + \int_0^{L_C} \left[ 1 + \frac{1}{E_p} \frac{dV}{dx} \right] \int_x^{L_C} J_0 W \left[ e^{q(V_{oa} - V(x))/kT} - 1 \right] dx' dx \]

\[ = qN_D W \mu \left\{ aV_{cs} - \frac{2}{3} \left( \frac{2e}{qN_D} \right)^{1/2} \left[ \left( V_{bi} - V_{GS} + V_{cs} \right)^{3/2} - \left( V_{bi} - V_{GS} \right)^{3/2} \right] \right\} \]  
(1.42)

The right hand side of the equation was previously found to be: $(L_C+V_{CS}/E_p)I_{DS}$, where $I_{DS}$ is the drain-to-source current in the absence of gate current.

The double integral on the left side of the equation can be defined as: $(L_C+V_{CS}/E_p)I_{GC}$

Therefore, the equation is reduced to: $I_{DS}=I_C+I_{GC}$

These suggest an equivalent circuit (not shown here) in which:

\[ -I_S = I_{DS} + I_{GC} - I_{GD} \]  
(1.43)

Using the definition of $I_{GC}$, we can integrate by parts to obtain:

\[ I_{GC} = \int_0^{L_C} W \left[ \frac{V(x)}{x + \frac{E_p}{V_{CS}/E_p}} \right] \left[ e^{q(V_{oa} - V(x))/kT} - 1 \right] dx \]  
(1.44)

and the total gate current is:

\[ I_G = \int_0^{L_C} \left[ e^{q(V_{oa} - V(x))/kT} - 1 \right] dx + I_{GD} \]  
(1.45)

Assume that the channel voltage $V(x)$ is a linear function of $x$:

\[ V(x) = \frac{dV}{dx} \left. x = E_1 x \right|_{x=0} \quad 0 \leq x \leq L_C \]  
(1.46a)
\[ V(x) = \frac{V_{DS} - E_1 L_C}{L - L_C} (x - L_C) + E_1 L_C \quad L_C \leq x \leq L \quad (1.46b) \]

So \( V(x) \) satisfies the boundary conditions that \( V(0) = 0 \) and \( V(L) = V_{DS} \).

Substituting the value of \( V(x) \) into the \( I_{GC} \) equation we get:

\[ I_{GC} = J_0 W L_C \frac{1 + \frac{E_1}{E_p}}{1 + \frac{V_{GS}}{E_p L_C}} \left\{ \frac{e^{qV_{GS}/kT}}{(qE_1L_C/kT)^2} \left[ 1 - \left( 1 + \frac{qE_1L_C}{kT} \right) e^{-qE_1L_C/kT} \right]^{-\frac{1}{2}} \right\} \quad (1.47) \]

and the total gate current becomes:

\[ I_G = J_0 W L_C \left\{ \frac{kT}{qE_1L_C} e^{qV_{GS}/kT} \left[ 1 - e^{-qE_1L_C/kT} \right] - 1 \right\} + I_{GD} \quad (1.48) \]

where,

\[ I_{GD} = J_0 W (L - L_C) \left\{ \frac{kT}{q(V_{DS} - E_1 L_C)} e^{q(V_{GS} - E_1 L_C)/kT} \left[ 1 - e^{-q(V_{GS} - E_1 L_C)/kT} \right] - 1 \right\} \quad (1.49) \]

\( I_{GC}, I_G \) and \( I_{GD} \) are all functions of \( E_1 \).

\( E_1 \) must satisfy the requirements that at \( x=0, I(0) = I_S \) and \( dV/dx = E_1 \).

Thus, from the \( I(x) \) equation we obtain:

\[ E_1 = \frac{I_S}{qN_D W \mu \left[ a - \left( \frac{2e}{qN_D} (V_{bi} - V_{GS}) \right) \right]^{1/2} - \frac{I_S}{E_p}} \quad (1.50) \]

It is seen that the gate current is approximately an exponential function of the gate voltage. This suggests a simplification of the gate current model. In fact, the gate currents at the source and the drain can be approximated by the currents of two diodes.

IV) Capacitive Currents

So far we have derived the expressions for the DC currents at the terminals of a MESFET in terms of the terminal voltages. If the voltages vary slowly with time, the
terminal currents will follow these changes. The values of the currents can be computed from the values of voltages at each particular instant of time, using the DC formulas for the current. However, when the rate of change of the voltages is large, we expect there will be capacitive currents at the terminals due to the presence of surface charge on the gate and to the charge in the depletion region along the channel. In this chapter we shall derive expressions for these capacitive currents based on the work of [10].

For the purpose of circuit analysis and simulation, it is convenient to assume a terminal description as follows:

\[
\begin{align*}
  i_D(t) &= I_D + \frac{dQ_D}{dt} \\
  i_G(t) &= I_G + \frac{dQ_G}{dt} \\
  i_S(t) &= -I_S + \frac{dQ_S}{dt}
\end{align*}
\]  

(1.51a) (1.51b) (1.51c)

where \( I_D, I_G, \) and \( I_S \) are the DC or slowly varying part of the respective terminal currents. \( Q_D, Q_G, \) and \( Q_S \) are the terminal charges whose rate of change is due to the capacitive currents at the terminals. The terminal charge is conserved at all times, thus:

\[
Q_D + Q_G + Q_S = 0
\]

(1.52)

Fig. 8 shows the two depletion regions under the gate. As the terminal voltages change with time, the depletion height \( h(x) \) and hence the amount of charge on the gate will change. The rate of change of the charge gives rise to a displacement current at the
gate, which adds to the total channel current and emerges at the drain and source terminals. Let $q_s(x,t)$ be the surface charge density on the gate. Then the current continuity equation becomes:

$$\frac{\partial i}{\partial x} = -W \frac{\partial q_s}{\partial t} \quad (1.53)$$

In integral form, we have, noting that $i(0,t) = -i_s(t)$,

$$i_s(t) = -i(x,t) - W \int_0^x \frac{\partial q_s}{\partial t} dx \quad (1.54)$$

Integrating over the channel and using integration by parts on the double integral, we get

$$i_s(t) = -\frac{1}{L} \int_0^L i(x,t)dx - \frac{d}{dt} \left[ W \int_0^L \left(1 - \frac{x}{L}\right) q_s(x,t)dx \right] \quad (1.55)$$

We define the quantity inside the brackets as the terminal charge at the source:

$$Q_s = -W \int_0^L \left(1 - \frac{x}{L}\right) q_s(x,t)dx \quad (1.56)$$

In a similar manner, we find the terminal charge at the drain to be:

$$Q_D = -W \int_0^L \frac{x}{L} q_s(x,t)dx \quad (1.57)$$

The total charge on the gate is

$$Q_G = -W \int_0^L q_s(x,t)dx \quad (1.58)$$

and it is equal to $-Q_D - Q_s$ as required.

In a two-region model, the surface charge density at any point $x$ is given by, for Region I:

$$q_s = -qN_D h(x) = -\sqrt{2\varepsilon q N_D (V_{bi} - V_{gs} + V(x))} \quad (1.59)$$

and for Region II:

$$q_s = -\varepsilon E_c \sinh \left[ \frac{\pi}{2a} (x - L_c) \right] - qN_D h_c \quad (1.60)$$

$$q_s = -qN_D \left[ \frac{h_c - h_s}{L_c} x + h_s \right] \quad (1.61)$$

with
\[
    h_c = \left[ \frac{2\varepsilon}{qN} \left( V_{bi} - V_{GS} + V_{CS} \right) \right]^{1/2}
\]

and
\[
    h_s = \left[ \frac{2\varepsilon}{qN} \left( V_{bi} - V_{GS} \right) \right]^{1/2}
\]

\[
    Q_D = WqN_D L_c \left[ \frac{1}{3} h_c \frac{L_c}{L} + \frac{1}{6} h_s \frac{L_c}{L} \right] + WqN_D h_c (L - L_c) \left( \frac{L + L_c}{2L} \right)
    + \frac{W\varepsilon E_c}{\pi} \left[ \frac{2a}{\pi} \cosh \frac{\pi}{2a} (L - L_c) - \frac{2a}{\pi} \sinh \frac{\pi}{2a} (L - L_c) - \frac{L_c}{L} \right]
\]

\[
    Q_G = -WqN_D L_c \left( \frac{h_c}{2} + \frac{h_s}{2} \right) - WqN_D h_c (L - L_c) - \frac{W\varepsilon E_c}{\pi} \left[ \frac{2a}{\pi} \cosh \frac{\pi}{2a} (L - L_c) - 1 \right]
\]

\[
    Q_s = WqN_D L_c \left[ \frac{h_c}{2} \left( 1 - \frac{2L_c}{3L} \right) + \frac{h_s}{2} \left( 1 - \frac{L_c}{3L} \right) \right] + WqN_D h_c (L - L_c) \left[ 1 - \frac{L + L_c}{2L} \right]
    + \frac{W\varepsilon E_c}{\pi} \left[ \frac{2a}{\pi} \sinh \frac{\pi}{2a} (L - L_c) - \frac{L - L_c}{L} \right]
\]

4.1 Charge-Based Model for Circuit Simulation

In any circuit simulation program, the transient response of a circuit is computed by solving numerically at discrete time points, \( t_1, t_2, t_3, \), etc., a system of nonlinear differential
equations which are in fact the node equations of the circuit. The solution is usually based on an implicit integration method. We can substitute each derivative term as follows:

\[
\frac{dx}{dt} \approx \frac{x(t_{k+1}) - x(t_k)}{h}
\]  

(1.70)

where \( h \) is the step size.

The set of terminal equations describing the transient behavior is shown at \( t = t_{k+1} \) in (1.71). Each term in the equation is a current term and therefore this suggests that the MESFET can be replaced by a circuit for the purpose of simulation, valid for \( t = t_{k+1} \), as shown in Fig. 9.

\[
i_D(t_{k+1}) = I_{DS}(t_{k+1}) - I_{GD}(t_{k+1}) + \frac{1}{h}(Q_D(t_{k+1}) - Q_D(t_k))
\]

\[
i_G(t_{k+1}) = I_G(t_{k+1}) + \frac{1}{h}(Q_G(t_{k+1}) - Q_G(t_k))
\]

(1.71)

\[
i_S(t_{k+1}) = -I_{DS}(t_{k+1}) - I_{GS}(t_{k+1}) + \frac{1}{h}(Q_S(t_{k+1}) - Q_S(t_k))
\]

Each current term, including those from the terminal charges, is a function of the terminal voltages. When these expressions are substituted, each terminal current of the device becomes a function of the node voltages at \( t_{k+1} \), which are the variables of the node equations of the circuit. When the node equations are assembled for the circuit, we have a system of non-linear algebraic equations in the unknowns of the node voltages. The equations are solved by iteration to obtain the node voltages at \( t_{k+1} \). We then proceed to the next time point and repeat the solution process after each current and charge term has been updated by the node voltages just computed, until the solution has been computed for the desired number of time points.

It should be emphasized that at any time point, charge is conserved in each device. Secondly, though the currents associated with the terminal charges are capacitive, no capacitance is computed. The derived charge-based model is most suitable for the purpose of numerical circuit simulation.
Fig. 9  Circuit Model of a MESFET
Chapter 2

Empirical Model

The models used in circuit simulation programs today are still based on empirical formulas. The reason is the simplicity of the equations which speeds up computer simulation. A variety of different models have been implemented in different versions of SPICE and other circuit simulation programs [1,2,3,4]. This chapter emphasizes the Statz model [3], because it's one of the more popular models.

1 Current-Voltage Characteristics

Figure 10 shows a typical set of current-voltage characteristics of a depletion type GaAs MESFET. Those of an enhancement type are shown in Figure 11. For a given gate-to-source voltage \( V_{GS} \), the drain current \( I_{DS} \) is an increasing function of the drain voltage \( V_{DS} \) that exhibits saturation at large values of \( V_{DS} \). This suggests a \( \tanh x \) type function.

Fig. 12 shows the drain current as a function of gate voltage for a set of fixed drain voltages. The current increases approximately quadratically as \( V_{GS} \) increases. The rate of increases is reduced as \( V_{GS} \) increases further. This suggests a function that is quadratic at low values of its argument and is less than quadratic for larger values.

When the gate voltage exceeds the Schottky barrier voltage, the gate becomes conducting and part of the gate current goes to the drain to reduce the net drain current, to the extent that for low values of \( V_{DS} \), the drain current becomes negative, as shown in Fig 11. The gate current can be accounted for by two diodes connecting the gate to the source and drain, respectively. The circuit model is shown in Fig. 13 in which a series resistance has also been added to each of the device terminals to account for the resistance of the gate, of the source-to-channel and drain-to-channel voltage drops.
As shown in Fig. 12, the device also has a cut-off characteristic, namely, when $V_{GS}$ is less than the threshold voltage $V_T$, the drain current is essentially zero, and the device can be regarded as a voltage-controlled switch. It is the cut-off and saturation characteristics that are utilized in the design of digital circuits.

Fig. 10 I-V Characteristics of a Depletion MESFET

Fig. 11 I-V Characteristics of an Enhancement MESFET
Many simplified models have been proposed. All are based on fitting the measured current characteristics to a functional description of the current. One of the most popular models is that of Statz [3] which has been installed in SPICE.

In the Statz model, the drain current is given by:

\[ I_{DS} = \beta \frac{(V_{GS} - V_T)^2}{1 + b(V_{GS} - V_T)} (1 + \lambda V_{DS}) \tanh \alpha V_{DS} \]  

(2.1)

where \( \beta \) is, according to [11]:

\[ \beta = \frac{2\varepsilon \mu v_s W}{a(\mu V_p + 3v_s L)} \]  

(2.2)

in which \( \varepsilon \) is the permittivity, \( \mu \) the low field mobility, \( v_s \) the electron saturation velocity, \( W \) the gate width, \( a \) the thickness of the active layer, \( L \) the gate length, and:

\[ V_p = \frac{qN_d a^2}{2\varepsilon} \]  

(2.3)

is the pinch-off voltage. \( N_d \) is the doping concentration of the active layer.

In Eq. 2.1, the second term accounts for the dependence on the gate voltage. The expression in the denominator, with \( b \) as a parameter, describes the compression of the drain current when the gate voltage is large. The third term accounts for the finite slope of the drain current when the drain voltage is large and the slope is controlled by the parameter \( \lambda \). The last term describes the drain current in both the linear and saturation regions with \( \alpha \) as a parameter. Sometimes, the \( \tanh x \) term is approximated by a polynomial and the drain current is given by:

\[ I_{DS} = I_{DSAT} \left(1 + \lambda V_{DS}\right) \left[1 - (1 - \alpha V_{DS} / 3)^3\right] \]  

(2.4)

for \( V_{DS} \leq 3/\alpha \) and

\[ I_{DS} = I_{DSAT} (1 + \lambda V_{DS}) \]  

(2.5)

for \( V_{DS} > 3/\alpha \).
Fig. 12 $I_D$ vs $V_{gs}$

Fig. 13 Simplified Equivalent Circuit of a MESFET
\[ I_{\text{DSAT}} \text{ is the "saturation current" given by:} \]
\[ I_{\text{DSAT}} = \beta \frac{(V_{GS} - V_T)^2}{1 + b(V_{GS} - V_T)} \quad (2.6) \]

Thus \( \alpha \) determines the onset of the "knee" of the current characteristics.

As shown in [3], the parameters of the Statz model can be adjusted to match the measured data almost exactly.

2 Charge and Capacitance

To complete the circuit model, we need to account for the capacitances at the terminals. For circuit simulation, it is the change of the charge as we go from time point \( t_k \) to \( t_{k+1} \) that describes the displacement current. It is argued that in a MESFET, there is only one physical charge that is the total charge on the gate. The displacement currents at the drain and source will have to be derived from this charge alone.

The gate charge \( Q_G \) is a function of the gate-to-source and gate-to-drain voltages. We assume that the gate-to-source and gate-to-drain displacement currents can be included in the terminal description as:

\[ i_D = I_{DS} - I_{GD} - \frac{dQ_{GD}}{dt} \]
\[ i_G = I_G + \frac{dQ_G}{dt} \quad (2.7) \]
\[ i_{GS} = -I_{DS} - I_{GS} - \frac{dQ_{GS}}{dt} \]

where the displacement currents are computed from:

\[ \frac{dQ_{GD}}{dt} \approx \frac{\Delta Q_{GD}}{h} \]
\[ \frac{dQ_{GS}}{dt} \approx \frac{\Delta Q_{GS}}{h} \quad (2.8) \]
\[ \frac{dQ_G}{dt} \approx \frac{\Delta Q_G}{h} \]

and the incremental changes will be approximated as:
\[ \Delta Q_{GD} = \frac{1}{2} \left[ Q_G \left( V_{DS}(t_{k+1}), V_{GS}(t_{k+1}) \right) - Q_G \left( V_{DS}(t_k), V_{GS}(t_{k}) \right) \right] + Q_G \left( V_{DS}(t_{k+1}), V_{GS}(t_k) \right) - Q_G \left( V_{DS}(t_{k}), V_{GS}(t_{k}) \right) \]

\[ \Delta Q_{GD} = \frac{1}{2} \left[ Q_G \left( V_{DS}(t_{k+1}), V_{GS}(t_{k+1}) \right) - Q_G \left( V_{DS}(t_{k}), V_{GS}(t_{k}) \right) \right] + Q_G \left( V_{DS}(t_{k}), V_{GS}(t_{k+1}) \right) - Q_G \left( V_{DS}(t_{k}), V_{GS}(t_{k}) \right) \]

\[ \Delta Q_G = Q_G \left( V_{DS}(t_{k+1}), V_{GS}(t_{k+1}) \right) - Q_G \left( V_{DS}(t_{k}), V_{GS}(t_{k}) \right) = \Delta Q_{GD} + \Delta Q_{GS} \]

It is seen that the sum of the displacement currents is zero.

It remains to find an expression for \( Q_G \). In order to keep the model simple and explicit, the gate charge is approximated by the following function:

\[ Q_G = 2 C_{gs0} V_{bi} \left[ 1 + \left( 1 - \frac{V_{eff1}}{V_{bi}} \right)^{1/2} \right] + C_{gs0} V_{eff2} \quad (2.12) \]

\[ V_{eff1} = \frac{1}{2} \left\{ V_{GS} + V_{GD} + \sqrt{\left( V_{GS} - V_{GD} \right)^2 + \Delta^2} \right\} \quad (2.13) \]

\[ V_{eff2} = \frac{1}{2} \left\{ V_{GS} + V_{GD} - \sqrt{\left( V_{GS} - V_{GD} \right)^2 + \Delta^2} \right\} \quad (2.14) \]

where \( C_{gs0} \) and \( C_{gd0} \) are the gate-to-source and gate-to-drain capacitances, respectively, under zero gate bias, i.e. \( V_{GS} = 0 \). The capacitances under a general bias condition are:

\[ C_{GD} = \frac{\partial Q_G}{\partial V_{GD}} \quad (2.15) \]

\[ C_{GS} = \frac{\partial Q_G}{\partial V_{GS}} \quad (2.16) \]

The parameter \( \Delta \) is chosen to smooth the transition of the capacitances as one becomes the other at \( V_{DS} = 0 \) when the drain becomes the source and vice versa. A value of \( 1/\alpha \) seems to work well.

In eq. 2.12, when \( V_{eff1} \) exceeds \( V_{bi} \), the expression breaks down, and it is suggested that it be replaced by:

\[ Q_G = C_{gs0} \left\{ 2 V_{bi} \left[ 1 - \left( 1 - \frac{V_{max}}{V_{bi}} \right)^{1/2} \right] + \frac{V_{eff1} - V_{max}}{\left( 1 - \frac{V_{max}}{V_{bi}} \right)^{1/2}} \right\} \quad (2.17) \]
for $V_{eff} \geq V_{max}$, with $V_{max}$ a parameter. A suitable value is 0.5V.

Finally, when the gate-to-source voltage goes beyond cutoff, i.e., $V_{GS} < V_T$, as often happens in circuit simulation, $V_{max}$ is replaced by $V_{new}$ where

$$V_{new} = \frac{1}{2} \left[ V_{eff} + V_T + \sqrt{(V_{eff} - V_T)^2 + \delta^2} \right]$$

(2.18)

Again, the parameter $\delta$ is used to smooth the transition of the capacitance $C_{GS}$ from a finite value to a small value beyond cutoff. A value of $\delta = 0.2$ is used.
Chapter 3

Experimental Data

In this chapter, we will describe experiments that have been conducted on a wafer containing GaAs MESFETs, to obtain measured current-voltage characteristics. SPICE is then used to generate I-V curves for the same devices. And finally, I-V characteristics obtained from the derived analytical model will be presented for comparison.

Measurements were taken on four transistors of different sizes. FET#1 (L=15μm, W=100μm), FET#2, or "FAT FET", (L=150μm, W=165μm), FET#3 (L=1μm, W=15μm) and FET#4, an RF transistor (L=1μm, W=50μm x 4).

The figure below shows how the probes were arranged on each MESFET for taking I-V measurements. A software was used on a computer interfaced to the probes and set for collecting data. In this case it gives the current value for each voltage setting.

![Fig. 14 Probes arrangement for I-V measurements](image-url)
Experiment 1

In the first experiment, the gate of a metal semiconductor field effect transistor has been characterized by the current-voltage (I-V) measurement technique and the capacitance-voltage (C-V) technique. As will be shown later, gate contacts were found to have a barrier of 0.84V and a forward voltage ideality factor of 1.04 using the I-V technique. The C-V technique produced a slightly higher barrier height value of 0.846V. Figures 15 and 16 show representative I-V curves for the gate contact (FET#2) in both forward and reverse bias conditions. A reverse breakdown voltage of \( V_b = -19V \) can be seen, as well as a forward turn on voltage of 0.6V.

![Fig. 15 MESFET Gate Characteristics for FET #2](image-url)
1.1 Current-Voltage Measurements

Using the Thermionic Emission-Diffusion Theory, the forward current density in a metal-semiconductor junction for $V > 3kT/q$ is:

$$J_F = A^* T^2 \exp\left(\frac{-q\phi_{bn}}{kT}\right) \exp\left(\frac{qV}{nkT}\right)$$

where $A^*$ is the effective Richardson constant, $\phi_{bn}$ is the junction barrier height, and $n$ is the ideality factor. Figure 17 shows the measured current density versus forward gate voltage for several discrete MESFETs. The intersection at zero voltage gives the saturation current density $J_S$, which is used in the following equation to determine the barrier height.

Fig. 16 Forward Biased Gate Schottky Contact (FET #2)
The ideality factor, $n$, is a measure of the quality of the diode junction. For a near perfect junction $n=1$, and all current transport is due to thermionic emission. Any interface damage will cause recombinations centers which act as intermediate states for tunnel currents. This raises $n$ typically between 1 and 2. $n$ can be determined from the following equation:

$$n = \left( \frac{kT}{q} \right) \left( \frac{\Delta V}{\Delta \ln(J)} \right)$$
Using the slope of the current density in Figure 17, 
\[ n = (38.6)(0.31/11.5) = 1.04. \]
n is very close to one indicating that the gate contact is very clean and free of damage.

At larger values of forward bias, Figure 17 shows there is a definite deviation from the straight line ideal diode characteristic. This effect is due to the series resistance of the ohmic source and drain contacts, and the channel. Essentially, the voltage seen by the intrinsic diode is reduced by this resistance, therefore reducing the current generated. The effect can be modeled as an ideal diode in series with a resistance, all with forward current:

\[
I_p = J_F A = A \left[ A^{\alpha T^2} \exp\left(-\frac{q\phi_B}{kT}\right) \right] \exp\left[ \frac{q(V_F - I_F R)}{nkT} \right]
\]

Where \( R \) is the lumped series resistance and \( A \) is the gate Area.

Figure 18 shows \( J_S \) solved numerically at various values of \( R \). This matches the measured data to the first order. Figure 19 shows the results of solving this equation for \( R \), given measured values of \( J_F \). \( R \) is only of importance at high currents, because of the \( I_S R \) term, and at high currents, the resistance approaches approximately 28 ohms. Figure 20 shows a plot of measured versus modeled current densities using \( R=28 \) ohms for transistors of two different areas. The measured current density shows a softer curvature, possibly due to the distributed nature of the real resistance.

Also from Figure 17 of the measured current density, at low values of applied voltage, the current level seems to oscillate. This effect is very small for the FAT FET, and becomes increasingly more noticeable for the smaller area devices.
Fig. 18 Modeled Diode Curves

Fig. 19 Effective FET Series Resistance
1.2 Capacitance-Voltage Measurements.

Another method, the Capacitance-Voltage technique, was used to characterize the gate diode. Capacitance measurements at different biases were taken on three devices with different gate areas: 2.5e-4, 1.5e-5, and 1.5e-7 cm². Figure 21 shows capacitance versus voltage for the three devices. Between -1 and -1.5V, the capacitance drops drastically, indicating that the full channel has been depleted, thus we expect a pinch-off voltage for the MESFET to be in this range.

A plot of capacitance versus area at zero volt bias, for nine different transistors is shown in Figure 22. It can be seen that capacitance increases linearly with area indicating that the area calculation is quite accurate for the larger area gates.
The doping density, $N_D$, can be found from:

$$N_D = \frac{2}{qK_0e_0A^2 \left[ \frac{dC^-}{dV} \right]}$$

where $A$ is the gate area and $C$ is the capacitance. Plots of $(A/C)^2$ versus $V$ for the three different devices were made (Figure 23).

From these plots the slope, $d(A/C)^2/dV$, can be determined at a particular bias, and therefore the doping density calculated. For example, the doping density for zero bias is:

$$N_D = \frac{2}{1.6e-19 \cdot 12.9 \cdot 8.85e-14 \cdot 9.5e13} = 1.15e17 \text{ cm}^{-3}$$

Fig. 21 Capacitance vs Voltage

![Fig. 21 Capacitance vs Voltage](image-url)
at 0 volt bias

**Fig. 22** Capacitance vs Area

**Fig. 23** \((A/C)^2\) vs Voltage
Also from the $(A/C)^2$ data, the barrier height can be determined using:

$$\phi_{Bn} = V_i + \frac{kT}{q}$$

where $V_i$ is the intercept with the voltage axis in Figure 23. From the graph, $V_i=0.82\text{V}$ therefore, $\phi_{Bn}=0.82+0.026=0.846\text{V}$.

The barrier heights found by the I-V and C-V techniques are very comparable, 0.84V and 0.846V respectively. Theoretically the barrier height found by the C-V technique is expected to be less affected by the interface defects, and therefore may be
slightly higher than the one from the I-V technique. The quality of the gate junction can be concluded to be very good from the ideality factor of 1.04.

2 Experiment 2

In the second experiment, detailed measurements were taken on four MESFETs of different sizes, in order to obtain their DC characteristics. The parameters found were the forward knee voltage $V_{KF}$, and the zero gate-bias knee voltage $V_{K0}$, their respective total drain currents $I_F$ and $I_{d0}$, and leakage current components $I_{PF}$ and $I_{P0}$. The pinch-off voltage $V_p$ and the transconductance $g_m$ are also determined. A DC model was developed, shown in Figure 25, which includes a current source, series gate, source, and drain resistances $R_g$, $R_s$, $R_d$ and a channel resistance $R_{ch}$. Values for all parameters are determined for the four transistors which include a FAT FET and a RF FET.

![DC MESFET Model](image)

**Fig. 25** DC MESFET Model
The test reticle contains a series of nine test transistors, from which we used the following FET's:

<table>
<thead>
<tr>
<th></th>
<th>Gate Length (μm)</th>
<th>Gate Width (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#2 (FAT FET)</td>
<td>150</td>
<td>165</td>
</tr>
<tr>
<td>#1</td>
<td>15</td>
<td>100</td>
</tr>
<tr>
<td>#3</td>
<td>1</td>
<td>15</td>
</tr>
<tr>
<td>RF</td>
<td>1</td>
<td>50 x 4 fingers</td>
</tr>
</tbody>
</table>

The I-V characteristics are shown in Figure 26 (for FET #3), showing the typical drain current vs voltage for different gate biases.

![Figure 26 I_d vs V_d (FET #3)](image)
2.1 Currents and Knee Voltages.

Figure 27 shows the values for $I_F$, $I_{d0}$, $V_{KF}$, and $V_{K0}$ which were extrapolated from the I-V characteristics of each transistor.

Figure 28 shows the extrapolation of $I_{PF}$ and $I_{P0}$ from the I-V curve at pinch-off. The results for all four FETs are shown in Table 1 and can be used as defined limits on the useful amplifying region of the transistors.

2.2 Pinch-off Voltage $V_F$:

Tests were made to determine the pinch-off voltage of the transistors. Nine devices were tested in order to determine the uniformity of $V_F$ for various geometries and sizes.

Fig. 27 $I_d$ vs $V_d$ (FET #1)
Fig. 28  $I_d$ vs $V_d$ (FET #1) at pinch-off

<table>
<thead>
<tr>
<th>FET (Gate LxW)</th>
<th>$V_{ko}$ (V)</th>
<th>$V_{kf}$ (V)</th>
<th>$I_{do}$ (mA)</th>
<th>$I_{f}$ (mA)</th>
<th>$I_{po}$ (mA)</th>
<th>$I_{pf}$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#2 (150x165um)</td>
<td>0.85</td>
<td>1.05</td>
<td>0.45</td>
<td>0.85</td>
<td>0.0080</td>
<td>0.0081</td>
</tr>
<tr>
<td>#1 (15x100um)</td>
<td>0.70</td>
<td>0.90</td>
<td>2.40</td>
<td>4.60</td>
<td>0.0320</td>
<td>0.0330</td>
</tr>
<tr>
<td>#3 (1x15um)</td>
<td>0.60</td>
<td>0.65</td>
<td>1.80</td>
<td>2.80</td>
<td>0.0460</td>
<td>0.0500</td>
</tr>
<tr>
<td>#4 (1x50x4um)</td>
<td>0.62</td>
<td>0.72</td>
<td>26.00</td>
<td>40.00</td>
<td>0.2300</td>
<td>0.2500</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FET (Gate LxW)</th>
<th>$R_{g/w}$ (Ω/mm)</th>
<th>$R_{ch}$ (Ω)</th>
<th>$\text{Ave} R_{s-Rd}$ Ω</th>
<th>$g_m$ (mS)</th>
<th>$g_m/W$ (S/mm)</th>
<th>$V_p$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#2 (150x165um)</td>
<td>44.91</td>
<td>1491.00</td>
<td>18.90</td>
<td>7.03</td>
<td>4.3</td>
<td>1.5</td>
</tr>
<tr>
<td>#1 (15x100um)</td>
<td>42.28</td>
<td>230.73</td>
<td>19.06</td>
<td>3.95</td>
<td>42.7</td>
<td>1.4</td>
</tr>
<tr>
<td>#3 (1x15um)</td>
<td>138.45</td>
<td>89.30</td>
<td>97.17</td>
<td>1.68</td>
<td>133.9</td>
<td>1.4</td>
</tr>
<tr>
<td>#4 (1x50x4um)</td>
<td>15.19</td>
<td>10.86</td>
<td>6.97</td>
<td>25.5</td>
<td>155.0</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Table 1  Table of Results
Using a plot of drain current vs gate voltage at $V_{ds}=0.05V$ (Figure 29), the pinch-off voltage is extrapolated as shown for each transistor. $V_p$ is found to be very uniform between FETs at a value of -1.4V as seen in Figure 30. Fukui's method for refining $V_p$ was also applied to the data. This method is described in [12]. The resulting pinch-off voltages averaged -1.5 and had less consistency among FETs, therefore the extrapolated values are believed to be more useful.

2.3 Parasitic Series Resistances.

In order to determine the resistances associated with the MESFET, several types of measurements were taken. The resistances to be determined are the gate, source, and drain series resistances $R_g$, $R_s$, $R_d$ and the channel resistance $R_{ch}$. The first measurement involved grounding the source and drain, and applying a forward bias to the gate. The slope of the I-V characteristic at high voltages, about 0.8V, will yield the resistance $R_{G-SD}$.

![Figure 29 Determination of the Pinch-off Voltage ($V_{ds}=0.05V$)](image)
The second and third measurements involved grounding only the source or the drain and applying a forward gate bias. The slopes of these I-V characteristics will yield $R_{G-S}$, and $R_{G-D}$, respectively. In the final measurement, the gate was left floating, drain grounded, and a small voltage was applied to the source. The slope of the resulting linear I-V characteristic is then $R_{S-D}$. A model was postulated in Figure 25, where current crowding is assumed along the edges of the gate (especially for long gate devices). Series source and drain resistances, $R_s$ and $R_d$, include contact resistance and some bulk channel resistance, gate resistance $R_g$ is simply the resistance of the gold metalization, and the channel resistance $R_{ch}$ is that of the channel GaAs. The measured resistances will have the following components of model parameters:

1. $R_{S-D} = R_s + R_d + R_{ch}$
2. $R_{G-S} = R_g + R_s$
3. $R_{G-D} = R_g + R_D$
4. \( R_{G-SD} = R_g + (R_S \parallel R_D) \)

Solving these equations for the model parameters we obtain:

1. \( R_s = R_{G-SD} - \sqrt{R_{G-SD}^2 - (R_{G-S}R_{G-SD} + R_{G-D}R_{G-SD} - R_{G-S}R_{G-D})} \)
2. \( R_s = R_{G-S} - R_g \)
3. \( R_d = R_{G-D} - R_g \)
4. \( R_{ch} = R_{D-S} - R_S - R_d \)

The source and drain resistances of individual FETs were found to be identical within 5\%, and the average of the two is plotted in Figure 31. \( R_S \) is proportional to \( \left( \frac{\text{source-gate spacing}}{\text{gate width}} \right) \) as expected. Theoretical calculations of \( R_S \) were made using channel parameters obtained in previous experiments:

Channel Doping: \( N_D = 10^{17} \text{ cm}^{-3} \)

Channel Thickness using \( V_p = -1.4V \): \( a = 0.18 \mu\text{m} \)

![Fig. 31 Source and Drain Series Resistance](image)

The theoretical values are also plotted in Figure 31. The FAT FET has a longer source-gate spacing, and therefore has a resistance above the line of theoretical values.
The channel resistance is expected to be proportional to \( \frac{\text{gate length}}{\text{gate width}} \), and is plotted in Figure 32 along with theoretical calculations of \( R_{ch} \) for a totally open channel and for a channel partially depleted by the gate built-in voltage of \( \phi_b = 0.84 \text{V} \). The measured parameter is found to be smaller than the theoretical calculation probably due to an error in the value of channel depth. A channel depth of 0.25\( \mu \text{m} \) would result in an excellent correlation to the theory. In order to maintain \( V_p = -1.4 \text{V} \), the doping for this channel depth would be \( 5 \times 10^{16} \) which is only 1/2 the peak calculated value.

**Fig. 32 Channel Resistance**

The gate resistance is shown in Figure 33 and can be seen to depend on the gate width. The different interconnects to the actual gate will increase \( R_g \) by a constant for the DC FETs. For the RF FET, with four fingers, the gate resistance is approximately 1/3 of
that expected for a single gate FET. The ratio is theoretically 1/4 because the fingers are
four resistances in parallel. Using a conductance for gold of $\sigma = 4.1\times10^4$ per $\Omega$cm, and a
gold thickness of $t = 0.5\mu m$, theoretical values of gate resistance were calculated by
counting 'squares' of gate length.

$$R_g = (\text{squares of gate length}) \times (\sigma t)^{-1}$$

The theoretical values are also plotted in Figure 33. The values are on the right order of
magnitude, but vary from the measurements due to the different multi-thickness sections
of the gate interconnect which was not modeled.

Table 1 contains values for all model resistances for each transistor. Since $R_g$ is
proportional to gate width, it is normalized to $1mm$ of gate width.

![Fig. 33 Gate Resistance](image)

2.4 DC Transconductance $g_m$

In order to determine $g_m$, we first find the average transconductance $g_m'$ from Figure
34 (drain current vs gate voltage at $V_d=1.6V$) as the slope of the curve.
However, this value is a result of degradation due to $R_S$.

The intrinsic value of the small-signal transconductance at the bias point $V_{ds}=1.6\text{V}$ can be derived as:

$$g_m = \frac{g_m'}{1-g_m'R_S}$$

The results obtained for $g_m'$ and $g_m$ are shown in Table 1, normalized to unit gate width.

![Graph](image-url)

**Fig. 34** $I_d$ vs $V_g$ (at $V_d=1.6\text{V}$) for FET #1

A summary of all results is shown in Table 1. The extracted parameters will define ranges of operation for the transistor. For example, to use a FET in an amplifying configuration the DC+small-signal voltage must be $>V_{K0}$, also a DC bias point of $I=I_0/2$ will allow uniform negative and positive small-signal inputs. Values of $R_g$, $R_S$, (and $R_d$),...
and \( R_{\text{eh}} \) can be used in the circuit in Figure 25 to estimate the effect of the parasitic resistances.

The transconductance is directly proportional to the amplifying power of a transistor. It can be seen in Table 1 that the RF transistor has, by far, the best design of the four. The unit transconductance has been increased by using a short gate length, and the total transconductance is over 15 times any other due to the long total gate width of 200\( \mu \)m. Because of the four gate fingers in parallel, the increase in \( g_m \) has been accomplished along with a reduction in parasitic resistances. The dramatic advantages of the multi-finger MESFET compensate for the increase in difficulty due to the air bridge interconnects.

3 Experiment 3

In order to characterize the metal-semiconductor field effect transistor (MESFET) many different measurements and modeling efforts were performed. Previously, the gate contact of a MESFET was characterized by: 1) the current-voltage (I-V) technique using the Thermionic Emission-Diffusion Theory with the forward current density given by:

\[
J_F = A^* T^2 \exp \left( -\frac{q\phi_{\text{Bn}}}{kT} \right) \exp \left( \frac{qV}{nkT} \right)
\]

and 2) the capacitance-voltage (C-V) technique where the barrier height can be obtained from \( 1/C^2 \) versus voltage data. Both methods gave the same value for the barrier height \( \phi_{\text{Bn}} = 0.84 \)V. Also obtained from these measurements was the saturation current density \( J_S = 1e-7 \) A/cm\(^2\); and the ideality factor \( n = 1.04 \).

The complete DC characteristics of four MESFETs of different sizes were also performed. Common source characteristics were measured and parasitic resistances were determined. Of most interest from the circuit design standpoint are characteristics of the RF transistor that has four gate fingers (1x50\( \mu \)m). This transistor was determined to have a pinch-off voltage \( V_P = -1.4 \)V, a saturation current of \( I_{\text{ds}} = 26 \)mA, and a transconductance \( g_m = 155 \) mS/mm.
In this experiment, the characteristics of this RF transistor are simulated. A SPICE model is used to simulate the DC behavior. Many of the model parameters are used from the analysis mentioned above, while others are further derived from DC data.

### 3.1 DC Characteristics Using PSPICE.

A simulation of the DC characteristics of the RF MESFET is performed on PSPICE, and then compared to measured results obtained previously. The model used is the SPICE GaAsFET model shown in Figure 35. Parameters for the SPICE model are calculated from measured data in the following manner.

![PSPICE n-Channel GaAsFET Model](image)

**Circuit Parameters:**
- Threshold voltage $V_{TO} = -1.7 \text{V}$
- Built-in potential $V_{BI} = 0.84 \text{V}$
- Ideality factor $N = 1.04$
- Saturation current $I_S = 2 \times 10^{-13} \text{A}$
- Tanh constant $\alpha = 1.61/\text{V}$
- Transconductance coefficient $\beta = 8.89 \times 10^{-3} \text{A/V}^2$
- Channel length modulation $\lambda = 1.95 \times 10^{-5} \text{m/V}$

*Fig. 35 PSPICE n-Channel GaAsFET Model*
Determination of VTO and BETA:

Figure 36 shows a plot of $\sqrt{I_{D, sat}}$ vs $V_{GS}$. The values for $I_{D, sat}$ were obtained by extrapolation to the $I_D$-axis of the saturated drain current on the $I_D$ vs $V_{DS}$ characteristics curves.

The plot in Figure 36 obeys the following equation:

$$\sqrt{I_{D, sat}} = \sqrt{\beta (V_{GS} - I_D R_s - VTO)}$$

The slope of this curve squared gives the transconductance coefficient parameter BETA, and the extrapolation of that curve intercepts the $V_{GS}$-axis with the threshold voltage parameter VTO. The values found were: $BETA=8.89 \times 10^{-3}$ A/V$^2$ $VTO=1.7$ V.

![Fig. 36 $\sqrt{I_{D, sat}}$ vs $V_{GS}$ (saturation mode)]
ii. Determination of LAMBDA: (channel length modulation)

For the common source characteristics of Figure 38 the curves of constant $V_{GS}$ can be extrapolated to intersect at some large negative voltage. The parameter $\lambda$ is the inverse of this voltage, and can be determined from the slope of the constant $V_{GS}$ curve by using two drain currents $I_{D1}$ and $I_{D2}$ and their corresponding $V_{DS1}$ and $V_{DS2}$:

\[
\frac{I_{D2}}{I_{D1}} = \frac{1 + \lambda \cdot V_{DS2}}{1 + \lambda \cdot V_{DS1}}
\]

The value obtained is:

$LAMBDA=19.95mV^{-1}$

Fig. 37  I-V Characteristics, RF-FET#4- Measured (solid)/SPICE (dashed)
iii. Determination of ALPHA: (tanh constant)

For short gate length MESFETs, the saturation current is determined by an additional term: \( \tanh(\alpha V_{DS}) \). The parameter \( \alpha \) affects the slope in the linear region. This can be seen by taking the first derivative of the following equation:

\[
    I_D = \beta(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tanh(\alpha V_{DS}) \quad \text{for } V_{GS} > V_T
\]

and evaluating the result at \( V_{DS} = 0 \):

\[
    \frac{\partial I_D(0)}{\partial V_{DS}} = \alpha \beta (V_{GS} - V_T)^2 = \alpha I_{D0}
\]

\( I_{D0} \) has been found previously to be equal to 26mA.

Hence \( \alpha \) is calculated to be: \( \text{ALPHA} = 1.61 \text{V}^{-1} \)

iv. Other Parameters.

Other parameters, whose values were previously measured, were also included in the model:

- The built-in potential: \( V_{BI} = 0.84 \text{V} \)
- The ideality factor: \( n = 1.04 \)
- The saturation current: \( I_S = 2 \times 10^{-13} \text{A} \)

Resistances used in the model are ohmic contact resistances and are negligible, therefore they have been left at their default value of zero.

Using the parameters cited above, the final results were obtained from the PSPICE model and plotted along with the previously measured data as shown in Figure 37. The modeled results matched well with the measured ones. Similarly, for FET #1, #2 and #3, we show the PSPICE and measured I-V characteristics in figures 38, 39 and 40 respectively. Again, the PSPICE curves were fairly close to the measured ones.
Fig. 38 I-V Characteristics, FET#1 Measured (solid)/SPICE (dashed)

Fig. 39 I-V Characteristics, FET#2 Measured (solid)/SPICE (dashed)
4 Analytical Model Characteristics

Using the results from chapter 1, for the drain current, we can get the I-V characteristics for the MESFETs used in the previous experiments.

Equation 1.25, \( \begin{align*}
I_{DS} &= \frac{I_p}{1 + \frac{V_{CS}}{V_p}} \left[ \frac{V_{CS}}{V_p} + \frac{2}{3} \left( \frac{V_{bi} - V_{GS}}{V_p} \right)^{3/2} - \left( \frac{V_{bi} - V_{GC}}{V_p} \right)^{3/2} \right] \\
I_p &= (qN_D)^2 a^3 \mu \frac{W}{L_c} \frac{1}{2\varepsilon}
\end{align*} \)

where, \( V_{GC} = V_{GS} - V_{CS} \)

\( L_c \) and \( V_{CS} \) are unknown.

From eq. 1.32, and after considering the boundary conditions at the drain we get:

\( V_{DS} = \frac{2a}{\pi} E_c \sinh \frac{\pi}{2a} (L - L_c) + V_{CS} \)

Thus we can find \( L_c \), knowing that \( \sinh^{-1} x = \ln \left( x + \sqrt{x^2 + 1} \right) \),
We can substitute the value of $L_c$ in eq. 1.28. Then, we have an equation with $V_{cs}$ unknown. Using the Mathcad computer program we enter all the equations mentioned above, and solve for $V_{cs}$ by Newton iteration method. Once we find $V_{cs}$, we substitute its value in the equation above to find $L_c$.

The following parameters were obtained previously in the experimental section:

Critical field, $E_c = 3$ kV/cm, saturation velocity, $v_s = 2 \times 10^7$ cm/s,

mobility, $\mu = 8600$ cm$^2$/V-s, channel doping concentration, $N_D = 1.15 \times 10^{17}$ cm$^{-3}$, built-in potential, $V_{bi} = 0.84$ V, threshold voltage, $V_T = -1$ V, channel thickness, $a = 0.18$ $\mu$m

For each of the four MESFETs we use the appropriate $L$ and $W$.

$V_{GS}$ and $V_{DS}$ are variables to which we can assign appropriate values to obtain $I_{DS}$.

Figures 41 to 44 show the I-V characteristics of the MESFETs (measured and analytical).

The results obtained come close to the measured data. The differences are due to precision errors in both measurements and calculations.

The charge/capacitance equations were derived in chapter 1 for the analytical model, and some C-V measurements were taken in the experimental section. The resulting analytical expressions for capacitive currents are extremely complex, and unfortunately there does not appear to be a way to obtain meaningful simplifications. Therefore, no attempt was made to correlate the analytical analysis with the data.
Fig. 41  I-V Characteristics, FET #1- Measured(solid)/analytical(dashed)

Fig. 42  I-V Characteristics, FET #2- Measured(solid)/analytical(dashed)
Fig. 43  I-V Characteristics, FET #3- Measured(solid)/analytical(dashed)

Fig. 44  I-V Characteristics, FET #4- Measured(solid)/analytical(dashed)
Conclusion

An Analytical model for the GaAs MESFET has been derived, based on a two-region description of the channel in which velocity saturation occurs in a region near the drain. The model expresses the terminal currents in terms of the terminal voltages and their rate of change, the former accounting for the DC characteristics and the latter the capacitive effects of the device. Both the drain current and the gate current must be computed from solution of nonlinear equations.

The MESFET analytical model derived previously is too complicated for use in circuit design or simulation. Each time the terminal voltages are changed, the drain current, gate current, and terminal charges must be re-evaluated and the evaluation requires that we solve a number of nonlinear algebraic equations by iteration. As the transient solution of a circuit is computed by numerical method, time point by time point, these currents and charges must be computed for each transistor over a number of terminal voltage values at each time point. This clearly requires a great deal of computer time and circuit simulation becomes inefficient.

On the other hand, the analytical model is based on physical principles and it shows how the current-voltage characteristics of the transistor depend on the device parameters. The model provides means to compute the sensitivity of circuit performance to changes in device dimensions, doping concentration, barrier height, or layer thickness. Such a model is needed to understand the properties of the device and to determine the theoretical limits of its capabilities.
Nevertheless, it is highly desirable to have a description of the current-voltage characteristics in an explicit functional form. The model should capture the essence of the device characteristics and be simple enough to make it possible to derive analytical expressions of the circuit performance for use in analysis and optimization of circuit design.

For efficient circuit simulation and hand analysis, a simple, empirical model, such as the Statz model, is preferred.

A variety of other empirical models exist (see References for further study). Other analytical models include a complete description of the conduction process [7], an analysis based on a three-section depletion region [13].


5. T.W. Thorpe, Computerized Circuit Analysis with SPICE: a complete guide to SPICE, with applications, John Wiley and Sons, 1992

6. S. Sze, Physics of semiconductor devices, John Wiley and Sons, 1981, Chap.5,6


Vita

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END OF TITLE