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A COMPARISON OF THRESHOLD VOLTAGE MODELS FOR NMOS TRANSISTORS INCLUDING SHORT-CHANNEL AND NARROW-WIDTH EFFECTS

by

Janet Cassard Montgomery

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

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April 14, 1981
(date)

Professor in Charge

Chairman of Department

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ABSTRACT

A practical and accurate model for determining the threshold voltage of NMOS transistors which takes into account short-channel and narrow-width effects is needed as large scale integrated circuits become more dense. Four models are compared on the basis of how well they predict threshold voltage with varying biases for various channel lengths and widths. The four models are: (1) Hiroo Masuda, Masaaki Nakai, and Masaharu Kubo's model, (2) A variation of a curve-fitting model (CFSIM) presently implemented in SPICE, (3) A simplification of Toru Toyabe and Shojiro Asai's model, and (4) R. R. Troutman and A. G. Fortino's model.

Forty different devices located on the same chip were probed. Their coded channel lengths were 2.0, 2.25, 2.5, 2.75, 3.0, 4.0, 5.0, 6.0, 7.0, and 8.0 microns in combination with coded widths of 2.0, 5.0, 10.0, and 30.0 microns. These coded dimensions yielded electrical channel lengths of 1.27, 1.50, 1.77, 2.00, 2.11, 3.34, 4.33, 5.33, 6.53, and 7.53 microns and electrical channel widths of 1.97, 4.85, 9.37, and 29.46 microns. For each device 25 threshold voltages were measured for 25 different combinations of biases. The values of backgate bias used were -2.0, -3.75, -5.5, -7.25, and -9.0 volts in combination with drain-to-source voltages of 0.2, 1.0,

3.0, 5.0, and 7.0 volts. This range of biases is sufficient to describe the possible biases a transistor could undergo in the normal operation of 5V dynamic RAMs.

For each device an n-parameter least squares fit is performed to determine the coefficients and RMS deviation of each model. The accuracy of the prediction is dependent upon device geometry for the four models. The Curve-Fitting Short-channel IGFET Model (the CFSIM model) shows the smallest RMS deviations for the forty devices and it does not suffer a loss of accuracy for the narrow long-channel devices as do the other models. Therefore, this model will be used in SPICE.

This work is not supported by government funds.

LIST OF SYMBOLS

β	Gain of a device (A/V^2).
$\beta_{\square}$	Gain of a large square device (A/V^2).
C_o	Gate capacitance per unit area.
ε_{ox}	Oxide dielectric constant = $3.9 \times 8.85 \times 10^{-14}$ F/cm.
ε_s	Dielectric constant of silicon = $11.4 \times 8.85 \times 10^{-14}$ F/cm.
I_{DS}	Drain-to-source current.
k	Boltzmann's constant.
L	Coded channel length.
L´	Electrical channel length.
N_B	Substrate doping.
ϕ_F	Fermi potential.
ψ_s	Surface potential.
q	Electronic charge.
T	Temperature.
t_{ox}	Gate oxide thickness.
V_{bi}	Built-in voltage.
V_{BS}	Backgate-to-source voltage.
V_{DS}	Drain-to-source voltage.
V_{FB}	Flatband voltage.
V_{GS}	Gate-to-source voltage.
V_T	Threshold Voltage.
W	Coded channel width.
W´	Electrical channel width.

I. INTRODUCTION

In order to design large scale integrated circuits there must exist an IV model which characterizes a transistor under all possible biases. For example when operating in the triode region, the classical equation is:

$$I_{DS} = \beta[(V_{GS} - V_T)\ V_{DS} - 1/2\ V_{DS}^2] \qquad (1)$$

and in the saturation region

$$I_{DS} = \frac{\beta}{2}\ (V_{GS} - V_T)^2 \qquad (2)$$

Then when the transistors are interconnected, the current and/or voltage level at any point in the circuit can be predicted through computer simulations. Even though more complex expressions than are contained in equations (1) and (2) are required to describe the IV characteristics of a real MOS transistor, threshold voltage plays a key role in these formulations. The accuracy with which the threshold voltage is modeled determines, especially near turn-on, the accuracy of the IV model. Good accuracy of the threshold model also tends to minimize the complexity of the IV formulations. This paper deals with the evaluation of various threshold models in order to find the most accurate one.

Knowledge of the threshold voltage is an aid when designing circuits. In simple terms, it lets the designer know the "on-off" gate voltage of a transistor (i.e. the point below which the drain current is negligible). This "on-off" point is a function of the process parameters, the device dimensions, and the bias conditions.

There are many definitions of threshold voltage. Three commonly used are: (A) In a plot of I_{DS} versus V_{GS} for $V_{DS} \leq V_G - V_T$, extrapolating the point of maximum slope to zero current and then subtracting 1/2 V_{DS} will yield a triode region threshold according to equation (1). This threshold for enhancement mode devices corresponds to the gate voltage necessary to produce a surface potential equal to twice the Fermi potential. (B) When operating in the saturation region (i.e. $V_{DS} > V_G - V_T$), a plot of $\sqrt{I_{DS}}$ versus V_{GS} supposedly yields a straight line according to equation (2). Extrapolating this line to zero current yields the saturation region threshold. This line is actually not straight, and, therefore, the determination of the threshold voltage is not very accurate or reproducible in this region. The reason for the deviation from a straight line fit is that equation (2) is the classical equation which does not take into account bulk charge and short-channel effects and,

hence, a two dimensional model should be used. (C) Another alternative is to define the threshold voltage to be the gate voltage which produces a predetermined current level regardless of the back-gate bias and drain-to-source voltage. This eliminates the need for distinguishing between triode region and saturation region thresholds and eliminates the ambiguity in determining the latter.

The computerized test set time needed to obtain the threshold voltage for a particular set of biases for a constant current level is approximately two seconds as opposed to about thirty seconds when the IV points have to be generated in order to extrapolate the threshold. This time difference is significant if many V_T points have to be taken. Hence, the gate voltage which produces a predetermined current level will be the definition of threshold voltage used in this paper. The current level used is $(.15 \times 10^{-6}) \frac{W}{L}$ amps. The method to obtain the threshold voltage is described in the Investigational Procedure section.

Several restrictions were placed upon the models to be considered. They are as follows:

(1) The threshold voltage must be a function of back-gate bias and drain-to-source voltage thereby taking into consideration short-channel effects.

(2) The model should not use too much computer time. H. S. Lee's model was discarded for this reason.

(3) It is desirable but not mandatory that the model have physical significance.

Four models were chosen which met these specifications:

(1) Hiroo Masuda, Masaaki Nakai, and Masaharu Kubo's model.

(2) A variation of a curve-fitting model (CFSIM) presently implemented in SPICE.

(3) A simplification of Toru Toyabe and Shojiro Asai's model.

(4) R. R. Troutman and A. G. Fortino's model.

A brief description of each model will now be given.

II. Masuda, Nakai, and Kubo's Model

Masuda, Nakai, and Kubo studied the effect of threshold lowering due to an increase in drain-to-source voltage. Using two-dimensional numerical analysis, they saw that the drain-to-source voltage has the effect of shortening the effective channel length.

> "In a short-channel MOSFET, the channel current is affected not only the the gate field but by the drain field . . . The results of this analysis clearly indicate that electrons are swept out into the bulk near the drain edge, which results in a shortening of the effective channel. The computed quasi-Fermi potential distrubution (Figure 1), furthermore, reveals that the drain field affects the channel as far as 1 μm from the drain junction. Such a drain field leads to poor cutoff characteristics of the device that are observed as the threshold voltage[1] (V_{TH}) changes with the drain voltage (V_D)."

Using experimental results, they proposed a model for the threshold voltage which is an extension of the classical gradual channel approximation. The expression is

$$V_T = V_{FB} + 2\phi_F + \frac{1}{C_o}\sqrt{2\varepsilon_S q N_B(|V_{BS}| + 2\phi_F)} - \frac{\eta}{C_o}[V_D + 2(|V_{BS}| + V_{bi})] \quad (3)$$

---

[1] H. Masuda et al, "Characteristics and Limitations of Scaled-Down MOSFET's Due to Two-Dimensional Field Effect," IEEE Transactions on Electron Devices (June 1979): 981.

where the variation of the drain coefficient, η, with channel length is given by

$$\eta = \eta_o (x_j, N_B) L'^{-n}$$

A two-parameter least squares fit will be performed on this equation determining the values of V_{FB} and η. A plot will be made of η versus L'^{-n} to check the accuracy of the prediction of threshold voltage dependence on channel length.

III. The CFSIM Model

The CFSIM model is a curve-fitting model and hence the name (Curve-Fitting Short-channel IGFET model).[2] The originator, W. Rosenzweig, calls it a "know-nothing" model. It attempts to describe experimentally observed characteristics with the simplest formulations possible, while maintaining accuracy. The formulas are extensions of the classical gradual channel approximation formulas. Thus, correspondence is maintained and the coefficients allow physical interpretation.

He originally modeled the threshold voltage variation with bias as

$$V_T = V_{T0} + K_1 \left(\sqrt{|V_{BS}| + 2\phi_F} - \sqrt{2\phi_F}\right) + K_2 V_{DS} \qquad (4)$$

where V_{T0} is the extrapolated threshold voltage at zero backgate bias and zero drain-to-source voltage. A plot of V_T versus $\sqrt{|V_{BS}| + 2\phi_F} - \sqrt{2\phi_F}$ with constant V_{DS} yields a straight line once sufficient backgate bias is applied. K_1 is the slope of this line. The decrease of threshold voltage with increasing drain-to-source voltage is described by K_2.

This equation does not take into account the interaction between backgate bias and drain voltage which is

[2] W. Rosenzweig, private communication.

not negligible for shorter channel length devices. For these devices, this interaction can lower the threshold as much as 200 mV. Hence, another term has been added. A new equation for threshold voltage is proposed:

$$V_T = V_{T0} + K_1 \left(\sqrt{|V_{BS}| + 2\phi_F} - \sqrt{2\phi_F}\right) + K_2 V_{DS}$$

$$+ K_{12} V_{DS} \left(\sqrt{|V_{BS}| + 2\phi_F} - \sqrt{2\phi_F}\right) \qquad (5)$$

where the K_{12} term simultaneously describes the decrease of K_1 with increasing V_{DS} and the increase of $|K_2|$ with increasing $|V_{BS}|$. A four-parameter least squares fit will be performed on this equation determining the values of V_{T0}, K_1, K_2, and K_{12}.

IV. Toyabe and Asai's Model

A model involving two-dimensional analysis is not appropriate when designing large scale integrated circuits since it takes too much computer time to simulate a circuit. Hence, Toyabe and Asai proposed an analytically closed form expression for the threshold voltage. They utilized their calculations of surface potential based on two-dimensional analysis to help derive the model.

Results from the two-dimensional analysis showed that a minimum surface potential, ψ_{min}, is obtained near the middle of the channel at the threshold voltage. A plot of $\psi_S-\psi_{min}$ versus distance along the channel (Figure 2b) reveals that there is an exponential behavior of the surface potential. Thus, their expression for threshold voltage shows an exponential decrease of V_T with decreasing channel length.

They also calculated the potential behavior from the surface to the substrate at different locations along the channel (Figure 2c).

> "The potential distribution is a concave curve similar to the depletion layer potential distribution in the middle of the

channel [curve (1)], while it is convex near the drain [curve (2)] when the drain voltage V_D is larger than the gate voltage V_G."[3]

Using these observations, Toyabe and Asai derived a closed form expression for V_T which they altered slightly with the aid of a two-dimensional analysis to improve the accuracy. Their equation is

$$V_T = V_{FB} + B\phi_F + \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_s q N_B (B\phi_F + |V_{BS}|)}$$

$$x[1 - \eta_o e^{-L'/l_o}] \qquad (6)$$

where

$$B = c_1 + \frac{kT}{2q\phi_F} \ln\left(\frac{2\phi_F + |V_{BS}|}{2\phi_F}\right) - c_2 e^{-L'/c_3}$$

$$l_o = W_o \left[c_4 + c_5 \frac{\varepsilon_{ox}}{\varepsilon_S} \frac{W_o}{t_{ox}}\right]^{-1/2}$$

$$\eta_o = \frac{\varepsilon_{ox}}{\varepsilon_S} \frac{\sqrt{(V + V_{bi} - B\phi_F)(V_{bi} - B\phi_F)}}{B\phi_F + |V_{BS}|}$$

$$x[c_6 \sqrt{B\phi_F + |V_{BS}|} + c_7]$$

$$W_o = \sqrt{\frac{2\varepsilon_S (B\phi_F + |V_{BS}|)}{qN_B}}$$

---

[3] T. Toyabe and S. Asai, "Analytical Models of Threshold Voltage and Breakdown Voltage of Short-Channel MOSFET's Derived from Two-Dimensional Analysis," IEEE Transactions on Electron Devices (April 1979): 434.

The constants c_1 through c_7 are determined for the range of processing parameters and bias conditions that are of interest.

Two simplifications will be made both of which enable a linear least squares fit to be performed on the equation. First, B will be set equal to 2.0. The Brown factor, B, designates the strength of inversion. For B=1 the silicon surface is intrinsic indicating the onset of inversion. When the concentration of minority carriers at the surface is equal to the concentration of majority carriers in the bulk, the surface is strongly inverted and B=2. Therefore, setting B=2 in equation (6) is a justifiable approximation. The second simplification will be letting l_o be independent of backgate bias. The end result is that we should expect larger RMS deviations for shorter channel length devices. With these assumptions, the equation may be written as

$$V_T = V_{FB} + 2\phi_F + \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_S q N_B (2\phi_F + |V_{BS}|)}\ [\ 1 - \eta_o] \quad (7)$$

where

$$\eta_o = \frac{\varepsilon_{ox}}{\varepsilon_S} \frac{\sqrt{(V_D + V_{bi} - 2\phi_F)(V_{bi} - 2\phi_F)}}{2\phi_F + |V_{BS}|}$$

$$\times [c_8 e^{-L'/l_o} \sqrt{2\phi_F + |V_{BS}|} + c_9 e^{-L'/l_o}]$$

Using these simplifications, a three-parameter least squares fit can be made, as opposed to an eight-parameter fit which can be cumbersome. The parameters $C_{c8} = C_8 e^{-L'/l_o}$, $C_{c9} = C_9 e^{-L'/l_o}$, and V_{FB} will be determined. A plot of ln $[C_{c8} \sqrt{2\phi_F + |V_{BS}|} + C_{c9}]$ versus L' for different widths when V_{BS} equals -3.0 volts will be made along with a plot of ln $[C_{c8} \sqrt{2\phi_F + |V_{BS}|} + C_{c9}]$ versus L' for varying backgate biases when W = 30.0 microns. These plots will help determine if the channel length dependence is predicted accurately.

V. Troutman and Fortino's Model

Troutman and Fortino's model utilizes the concept of charge injection over a potential barrier. With the aid of two-dimensional numerical simulations they came up with a simplified formula for threshold voltage which adequately describes the behavior of the potential barrier. Their expression is

$$V_T = V_{TLC} - \alpha - \beta V_{DS} \quad (8)$$

where V_{TLC} is the long-channel threshold voltage. They then express α and β in terms of the proximity factor, Pr, and the penetration coefficient, Pe, to be discussed later. By solving the one-dimensional Poisson equation they were able to write their equation as

$$V_T = V_{TLC} - (\frac{kT}{q} \; Pr + PeV_{DS})[1 + \frac{t_{ox}(q\varepsilon_S N_B)^{1/2}}{\varepsilon_{ox}[2(|V_{BS}| + 2\phi_F)]^{1/2}}] \quad (9)$$

where Pe is directly proportional to $\frac{1}{L}$..

In order to appreciate this expression, it is necessary to understand the behavior of the potential barrier.

For long-channel devices when the drain-to-source voltage is zero (Figure 3a), the excess band-bending is constant along the channel except near the source and

drain where it increases due to the built-in voltage of the junctions. If there is an increase in V_{DS} (Figure 3b) the potential near the middle of the channel remains the same and hence the current flow is not altered.

For short-channel devices, Troutman and Fortino considered two separate effects. In the first case, when V_{DS} equals zero the potential has a minimum value at one point in the middle of the channel (Figure 3c). This minimum value corresponds to the minimum value in the long-channel case. As V_{DS} increases (Figure 3d) this potential minimum increases and moves closer to the source. This is due to the merging of the source and drain depletion regions (the penetration effect). Due to the increase of the potential minimum, an application of a drain-to-source voltage increases the current flow in the channel.

In the second case, due to the proximity of the junctions, the source and drain depletion regions have already merged for V_{DS} equal to zero (Figure 3e). Hence, the potential minimum located in the middle of the channel is larger than for the long-channel case (the proximity effect). In order to correct for this the substrate bias has to be made more negative. An application of a drain-to-source voltage (Figure 3f) again increases the potential minimum and moves it closer to the source.

Referring to Equation (9), the penetration and proximity effects are described by the terms involving Pe and Pr, respectively. The multiplicative term describes the amount of band-bending defined to be the threshold voltage.

The classical expression for V_{TLC} is

$$V_{TLC} = V_{FB} + 2\phi_F + \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_s q N_B}\ [\sqrt{|V_{BS}| + 2\phi_F}] \tag{10}$$

Hence the equation for the threshold voltage becomes

$$V_T = V_{FB} + 2\phi_F + \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_S q N_B}\ [\sqrt{|V_{BS}| + 2\phi_F}] - (\frac{kT}{q} Pr + PeV_{DS})[1 + \frac{t_{ox}\ (q\varepsilon_S N_B)^{1/2}}{\varepsilon_{ox}[2(|V_{BS}| + 2\phi_F)]^{1/2}}] \tag{11}$$

A three-parameter least squares fit will be performed on this equation. V_{FB}, Pr, and Pe will be determined and an RMS deviation returned. Choosing the flatband voltage as a parameter will improve the fit and will also be a check to see if it lies within a reasonable range. Pe will then be plotted versus $\frac{1}{L}$ to see if the channel length dependence is predicted accurately.

VI. Investigational Procedure

A. Equipment Used

For this investigation a computer program was written for the Keithley System 2/LPT System. On this system a computer program can make and break circuit connections, force currents and voltages, take measurements, perform calculations on the measurements, provide operator interaction if desired, and print out the results on a line printer.

The system includes a PDP-11/03TM microcomputer made by DEC, three voltage sources, a current source, a voltmeter, a picoammeter, and a capacitance meter which can be connected to a device via a full Kelvin relay matrix. The programs are entered from a terminal and stored on floppy discs. The program written for this investigation enabled the Keithley to take all the measurements on one device and determine the model parameters for all four models in less than five minutes.

B. The Circuit Wiring

The circuit wiring used to obtain the gate voltage for a predetermined current level in shown in Figure 4. With a specified drain voltage and backgate bias, the threshold current is forced and the gate voltage adjusted until the voltmeter reads a negligible value. The threshold voltage is, by definition, the final gate voltage.

C. Determination of the Gate Oxide Thickness

To determine the active gate oxide thickness a large capacitor (325 x 355 microns) located near the chip of interest was probed and connected to a Boonton capacitance meter. The meter can be accessed through the matrix of the Keithley system. Minus ten volts is applied to the polysilicon electrode to assure that the capacitor is biased into accumulation. Under this condition a capacitance measurement corresponds to the oxide capacitance. The measured capacitance was used to determine the oxide thickness:

$$t_{ox} = \frac{\varepsilon_o k_{ox} AREA}{C_{meas}} \qquad (12)$$

A gate oxide thickness of 556Å was thus determined.

D. Determination of the Substrate Doping

To determine the substrate doping a large square transistor (200 x 200 microns) located near the chip of interest was probed. Using 0.2 volts on the drain, the threshold voltage was measured for three different values of backgate bias (-3.0, -6.0, and -9.0 volts). A plot of V_T versus $\sqrt{|V_{BS}| + 2\phi_F} - \sqrt{2\phi_F}$ yields a straight line, according to equation (10), once sufficient backgate bias is applied. The slope of this line is related to the substrate doping by the classical long-channel equation:

$$N_B = [\frac{(SLOPE)\ \varepsilon_{ox}}{t_{ox}}]^2 \frac{1}{2\varepsilon_S q} \qquad (13)$$

A linear least squares fit on the three points gave a slope of .423 $V^{1/2}$ with an RMS deviation of 1.4 mV. The substrate doping was calculated to be 2.14 x $10^{15}/cm^3$ using the oxide thickness of 556Å found previously.

E. Determination of the Electrical Channel Length

In order to determine the electrical channel length, L´, the gain of a large square device (50 x 50 microns) was found. To determine the gain of a device the following procedure was used. With 0.1 volts applied to the drain and -3.0 volts backgate bias, the I_{DS} versus V_{GS} curve was generated. The maximum slope of this curve divided by the drain-to-source voltage is the gain of the device, β, according to equation (1). After the gain of the large square device was found the gain of a wide device (30 microns) with the channel length of interest was found using the same procedure. Since $\beta = \beta_{\square} \frac{W'}{L'}$, L´ can be determined assuming the coded channel width is equal to the electrical channel width which is a good approximation for wide devices.

F. Method of Measurement and Analysis

The purpose of this investigation is to determine which of the four models is most accurate over a realistic range of biases and device dimensions. Therefore,

forty different devices located on the same chip were probed. Their coded channel lengths were 2.0, 2.25, 2.5, 2.75, 3.0, 4.0, 5.0, 6.0, 7.0 and 8.0 microns in combination with coded widths of 2.0, 5.0, 10.0, and 30.0 microns. These coded dimensions yielded electrical channel lengths of 1.27, 1.50, 1.77, 2.00, 2.11, 3.34, 4.33, 5.33, 6.53, and 7.53 microns and electrical channel widths of 1.97, 4.85, 9.37, and 29.46 microns. The junction depth was 0.3 microns. For each device 25 threshold voltages were measured for 25 different combinations of biases. The values of backgate bias used were -2.0, -3.75, -5.5, -7.25, and -9.0 volts in combination with drain-to-source voltages of 0.2, 1.0, 3.0, 5.0, and 7.0 volts. This range of biases is sufficient to describe the possible biases a transistor could undergo in the normal operation of 5V dynamic RAMs.

For each device an n-parameter least squares fit was performed to determine the coefficients and RMS (root means square) deviation of each model. The RMS deviation is defined as

$$\text{RMS} = \sqrt{\frac{\Sigma\ (\text{measured values} - \text{calculated values})^2}{\text{number of points}}}$$

It is a measure of how well the calculated values correspond to the experimental points. The same set of data

points was used for the four models. The results are analyzed as follows. To determine the ability of each model to predict threshold with bias, the four "corner" transistors (L = 2,8 and W = 2,30 combinations) are examined in detail. This is done in Section VII. The length and width variation of the model coefficients are then examined in Section VIII. The overall accuracy based on the RMS deviations between calculated and measured values for all 40 transistors and the four models are discussed in the concluding Section IX.

VII. Variation with Bias

To determine which of the four models predicts most accurately the threshold variation with bias and device dimensions let's first consider how the models predict the threshold variation with bias. To do this let's consider the following four devices:

(1) A wide long-channel device (W = 30, L = 8),

(2) A narrow long-channel device (W = 2, L = 8),

(3) A wide short-channel device (W = 30, L = 2), and

(4) A narrow short-channel device (W = 2, L = 2).

For the wide long-channel device, Figure 5 is a plot of V_T versus $\sqrt{2\phi_F + |V_{BS}|} - \sqrt{2\phi_F}$ for a drain-to-source voltage of 3 volts. The plots are similar for different values of drain-to-source voltage. For this device, each model predicts accurately the threshold voltage with less than a 5 mV RMS deviation. This is to be expected. For long-channel devices, the effect of drain-to-source voltage is negligible and, hence, in each model the terms involving V_{DS} tend toward zero. In other words, η in Masuda's model, K_2 and K_{12} in the CFSIM model, $[C_{c8}\sqrt{2\phi_F + |V_{BS}|} + C_{c9}]$ in Toyabe's model, and Pe in Troutman's model all go to zero.

Figure 6 is a similar plot for the narrow long-channel deivce where V_{DS} is equal to 0.2 volts. The CFSIM model fits well with an RMS deviation of 7 mV. This is due to the fact that the parameters which govern

the drain-to-source dependence are width independent as they should be. In other words, K_2 and K_{12} tend toward zero for long-channel devices independent of the width. Eta in Masuda's model and $[C_{c8} \sqrt{2\phi_F + |V_{BS}|} + C_{c9}]$ in Toyabe's model are both width dependent resulting in RMS deviations of 76 and 75 mV, respectively. In Troutman's model Pe is width independent, however, Pr is width dependent resulting in a deviation from the long-channel case of 37 mV.

For the wide short-channel case (i.e. W = 30, L = 2) Figures 7 through 10 are the plots of V_T versus $\sqrt{2\phi_F + |V_{BS}|} - \sqrt{2\phi_F}$ at different values of V_{DS} for Masuda's model, the CFSIM model, Toyabe's model, and Troutman's model, respectively. From these plots as well as those for the narrow short-channel device (i.e. W = 2, L = 2) in Figures 11 through 14 we can closely examine the behavior of the models as a function of bias. For all of the models the threshold voltage increases with backgate bias and decreases with drain-to-source voltage as it should.

The data shows an interdependence of V_{BS} and V_{DS}. The threshold voltage is more sensitive to V_{DS} at higher values of $|V_{BS}|$ and is less sensitive to V_{BS} at higher values of V_{DS}. The CFSIM model predicts this and so does Toyabe's model; however, Toyabe's model overemphasizes this interdependence. Troutman's model predicts

the interdependence in the wrong direction and Masuda's model shows no interdependence at all as can be seen from the equations. Therefore, data patterning results especially for short-channel devices where the interdependence predominates. This can lead to large RMS deviations. For the wide short-channel case the RMS deviations were 128, 15, 41, and 27 mV for Masuda's model, the CFSIM model, Toyabe's model, and Troutman's model, respectively while for the narrow short-channel case the deviations were 134, 17, 16, and 25 mV, respectively.

VIII. Variations with L´ and W

A. Masuda's Model

For Masuda's model Figure 15 is a plot of V_{FB} versus L´ for various widths. The values of the flatband voltage fall within a reasonable range; however, it was expected that it would be independent of device dimensions. The plot shows that the flatband voltage decreases for short-channel devices and increases for narrow-width devices. Understanding these variations is beyond the scope of this investigation.

Masuda's model indicates that η is channel length dependent and varies as L^{-n}. Figure 16 is a plot of η versus L^{-n} where n equals 1.5. It is apparent that the model accurately describes the channel length dependence.

B. The CFSIM Model

Figures 17 through 20 are plots of K_1, K_2, K_{12}, and V_{T0}, respectively, versus L´ for various widths for the CFSIM model. All of the parameters are channel length dependent and only K_1 exhibits significant width dependence. For the wide devices in the long-channel limit K_1 should approach $\frac{\sqrt{2q\varepsilon_S N_B}}{C_{ox}}$ which equals .424 $V^{1/2}$. It does approach this limit.

For the CFSIM model the flatband voltage can be expressed as

$$V_{FB} = V_{T0} - 2\phi_F - \sqrt{2\phi_F}\,(K_1 + K_{12}V_{DS}) \qquad (14)$$

At zero drain-to-source voltage it becomes

$$V_{FB0} = V_{T0} - 2\phi_F - K_1\sqrt{2\phi_F} \qquad (15)$$

A plot of V_{FB0} versus L´ for the various widths is shown in Figure 21. The flatband voltages take on reasonable values. However, its dependence on device dimensions is again a subject for further study beyond the present scope. For this model it appears that the flatband voltage decreases with decreasing channel width.

C. Toyabe's Model

For Toyabe's model, Figure 22 is a plot of V_{FB} versus L´ for the different channel widths. The values fall within a reasonable range; however, for the narrow devices the values are significantly higher. It is apparent that the flatband voltage varies with channel length and width as it does in Masuda's model.

The simplified model predicts an exponential channel length dependence for $[C_{c8}\sqrt{2\phi_F + |V_{BS}|} + C_{c9}]$. Therefore, ln $[C_{c8}\sqrt{2\phi_f + 3.0} + C_{c9}]$ is plotted against L´ in Figure 23 for various widths. This plot shows that deviations from a straight line fit occur for narrow devices. Had the model without simplification been used it would not significantly correct the deviations shown for the narrow long-channel devices.

Figure 24 is a plot of ln $[C_{c8} \sqrt{2\phi_F + |V_{BS}|} + C_{c9}]$ versus L' for three different values of backgate bias for the 30 micron wide devices. This shows that the effect of backgate bias is to shift and slightly displace the "straight lines".

D. <u>Troutman's Model</u>

Figure 25 is a plot of V_{FB} versus L' for different widths for Troutman's model. As for Masuda's and Toyabe's model the flatband voltage decreases for short-channel devices and increases for narrow-width devices. The flatband voltage is much too positive for the narrow long-channel devices and loses its physical significance.

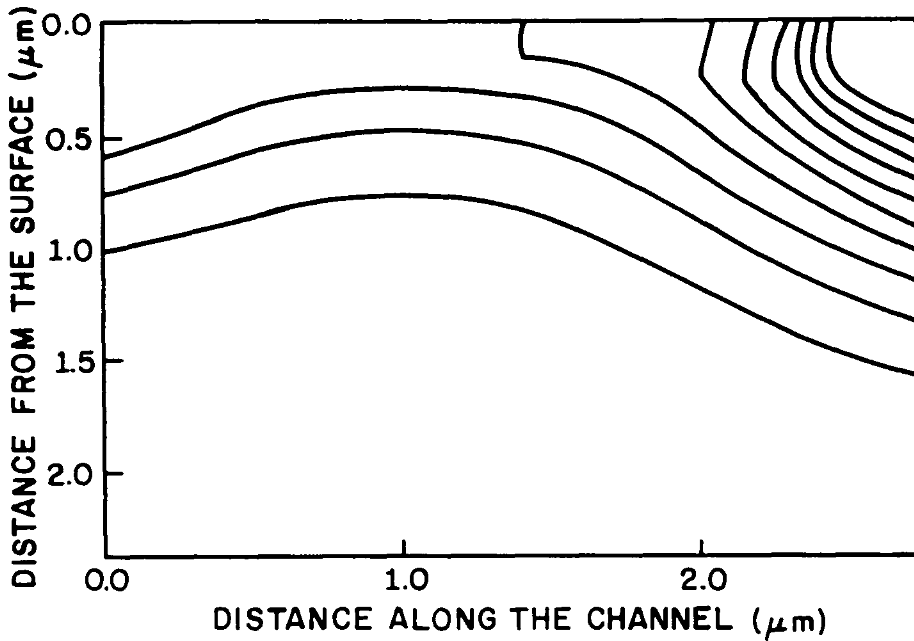
Figure 26 is a plot of Pr versus L' and Figure 27 is a plot of Pe versus $\frac{1}{L'}$. The channel length dependence of Pe is accurately described. Allowing the flatband voltage to vary causes Pr to be channel length dependent.

IX. Summary - The Best Model

Figures 28 through 31 are the RMS deviations versus L for the different channel widths for Masuda's model, the CFSIM model, Toyabe's model, and Troutman's model, respectively. It is apparent from these plots that the CFSIM model is the best model as well as the simplest formulation and should be used to model NMOS transistors. In addition to having low RMS deviations this model also fits well for narrow long-channel devices unlike the other models. Although it is not an altogether physical model, reasonable interpretation of the coefficients lead to reasonable flatband voltages and substrate doping. Curve-fitting models are attractive because messy equations do not have to be solved and it's relatively easy to describe or improve the models.

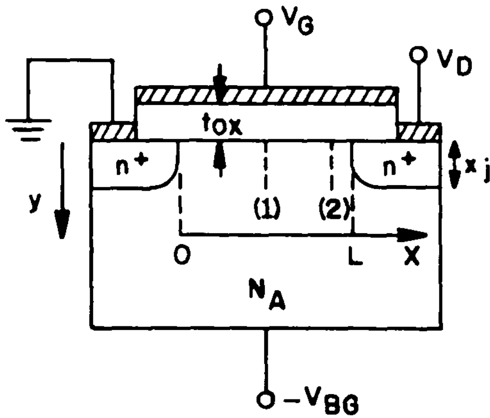
It might be argued that the CFSIM model describes the threshold voltage most accurately since a four-parameter least squares fit was used for this model, a three-parameter fit for Toyabe's and Troutman's models, and a two-parameter fit for Masuda's model. This is a result of how "physical" each model is represented to be. A totally physical model would have no adjustable parameters. Let it be noted, however, if in each of the models V_{FB} were to have been constrained to a reasonable "physical" value, the CFSIM model would still have provided the best fit.

If the flatband voltage is indeed independent of device dimensions, then the parameter V_{FB} in each of the models should be redefined. However, it is conceivable that the flatband voltage can depend on device dimensions especially for the short-channel or narrow-width devices.

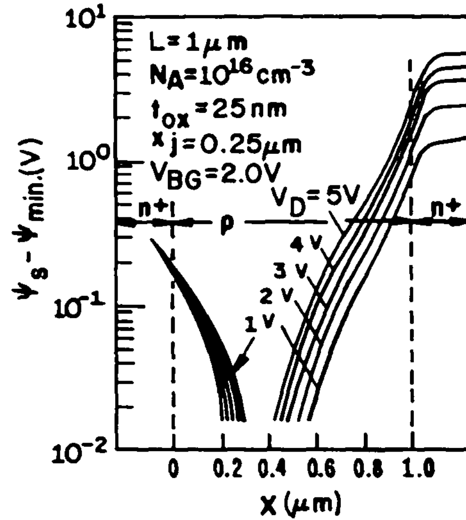


MASUDA'S TWO DIMENSIONAL NUMERICAL ANALYSIS
WHEN $L = 2.8\,\mu m$ AND $V_{BS} = -2.0$ V.
QUASI-FERMI POTENTIAL LINES: 0.62–6.02 (V)

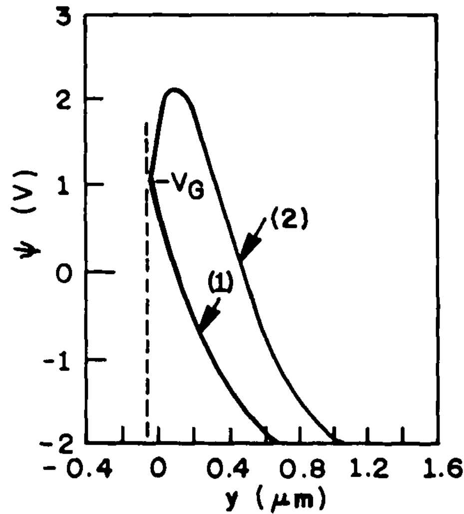
FIGURE 1



(a) CROSS SECTION OF A MOSFET

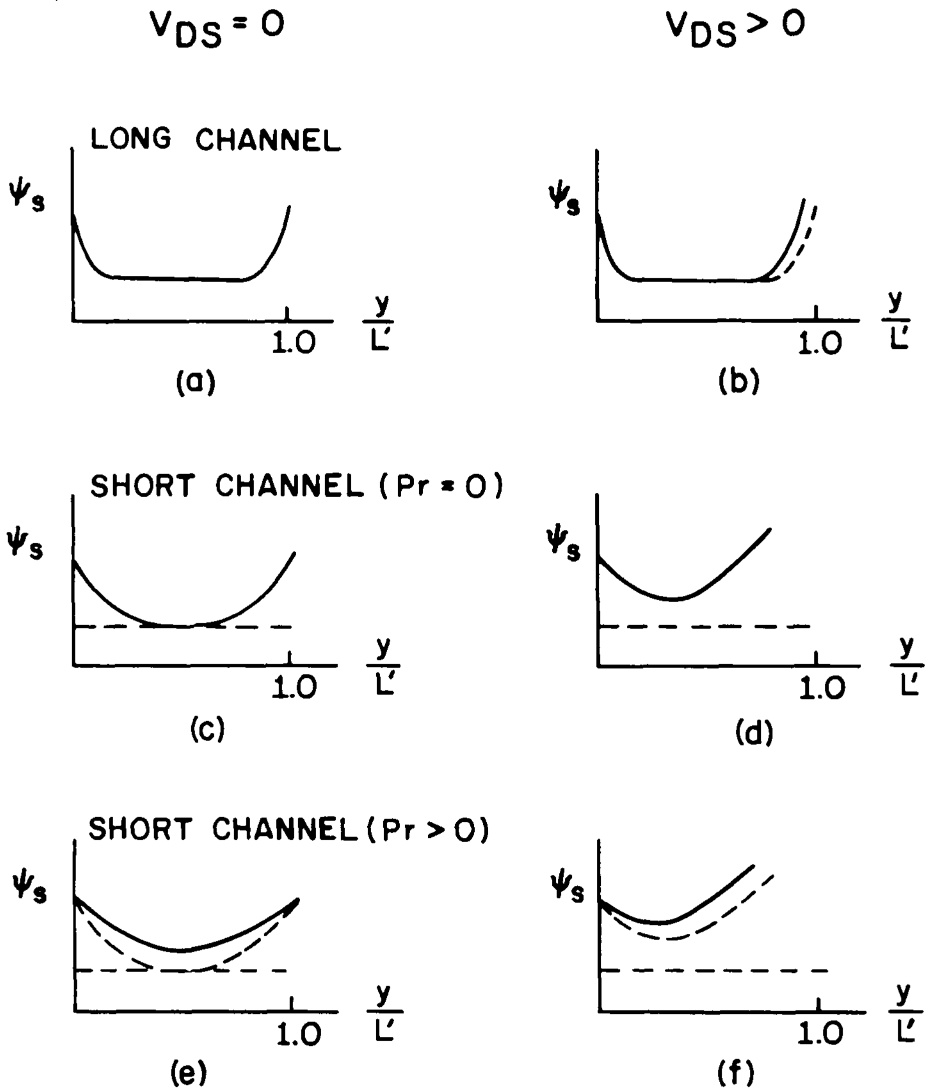


(b) TOYABE'S SURFACE POTENTIAL DISTRIBUTION FOR VARIED DRAIN VOLTAGE



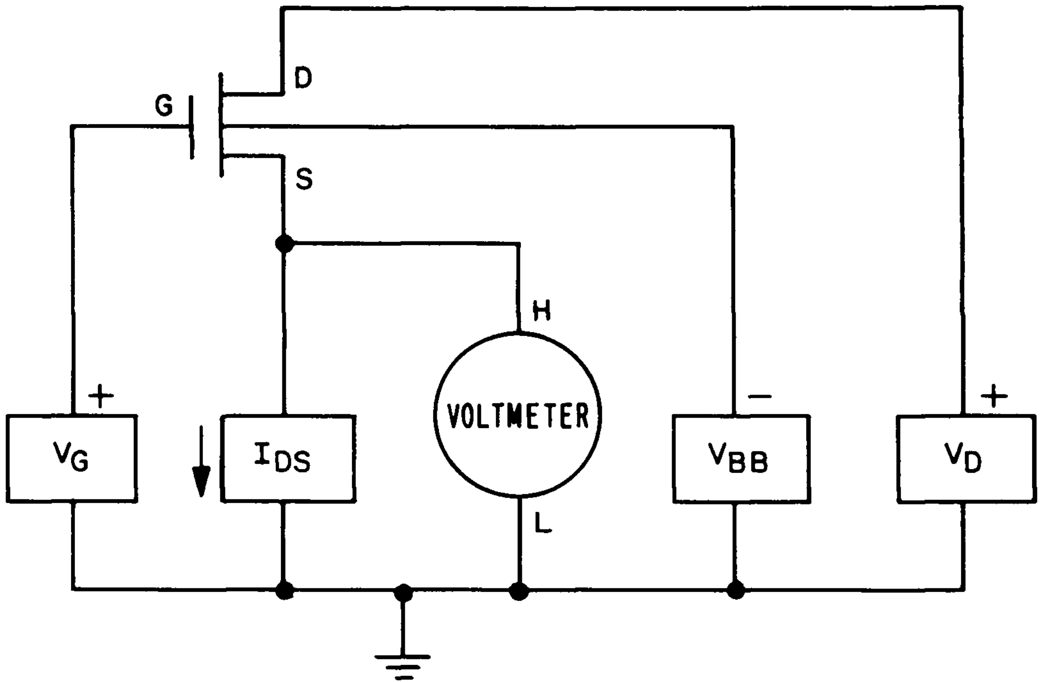
(c) TOYABE'S POTENTIAL DISTRIBUTION IN THE DIRECTION FROM SURFACE TO SUBSTRATE. CURVES (1) AND (2) ARE POTENTIAL DISTRIBUTIONS ON THE LINES (1) AND (2), RESPECTIVELY, IN FIGURE (a).

FIGURE 2

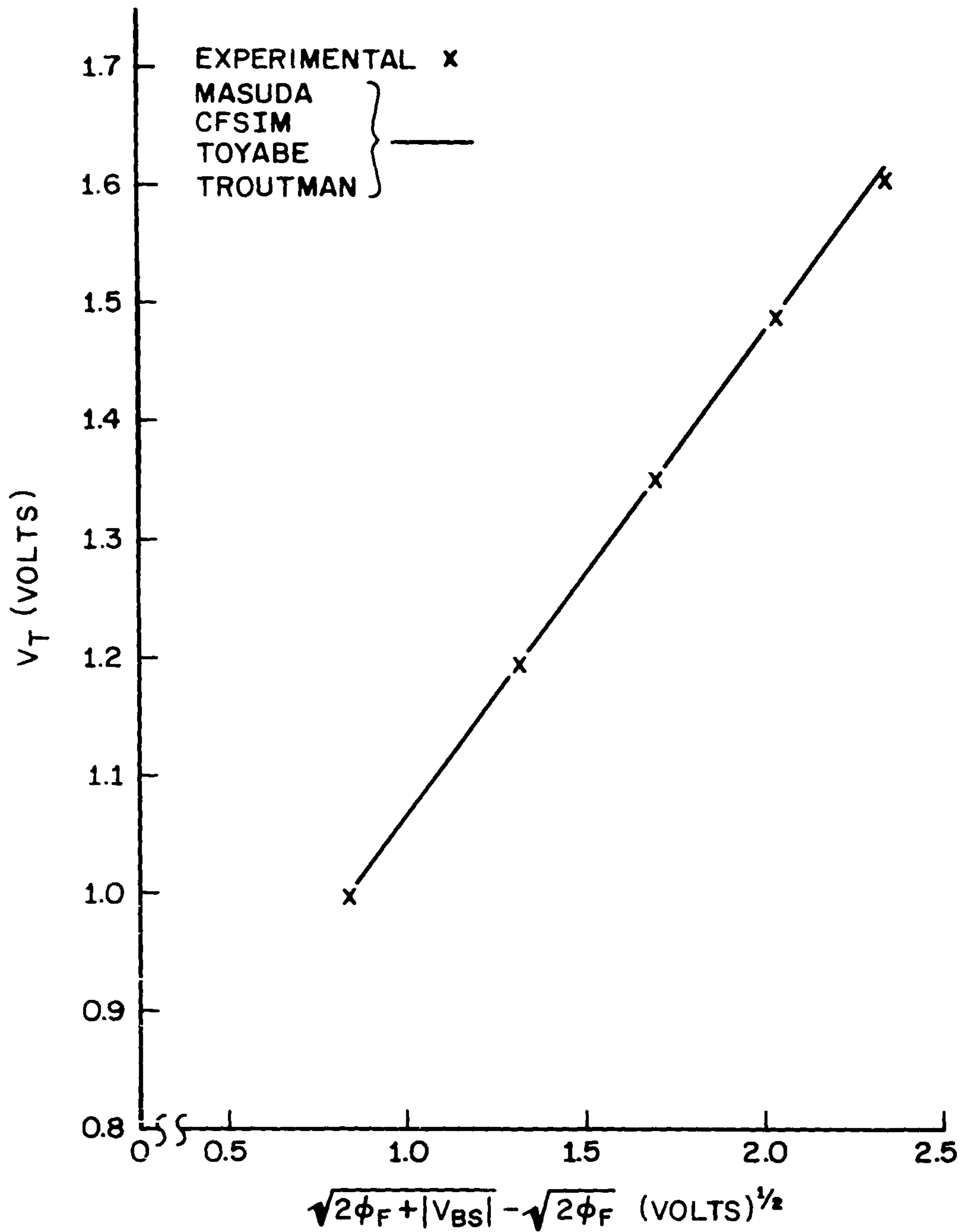


TROUTMAN'S SCHEMATIC ILLUSTRATIONS OF THE SURFACE POTENTIAL FROM THE SOURCE TO THE DRAIN

FIGURE 3

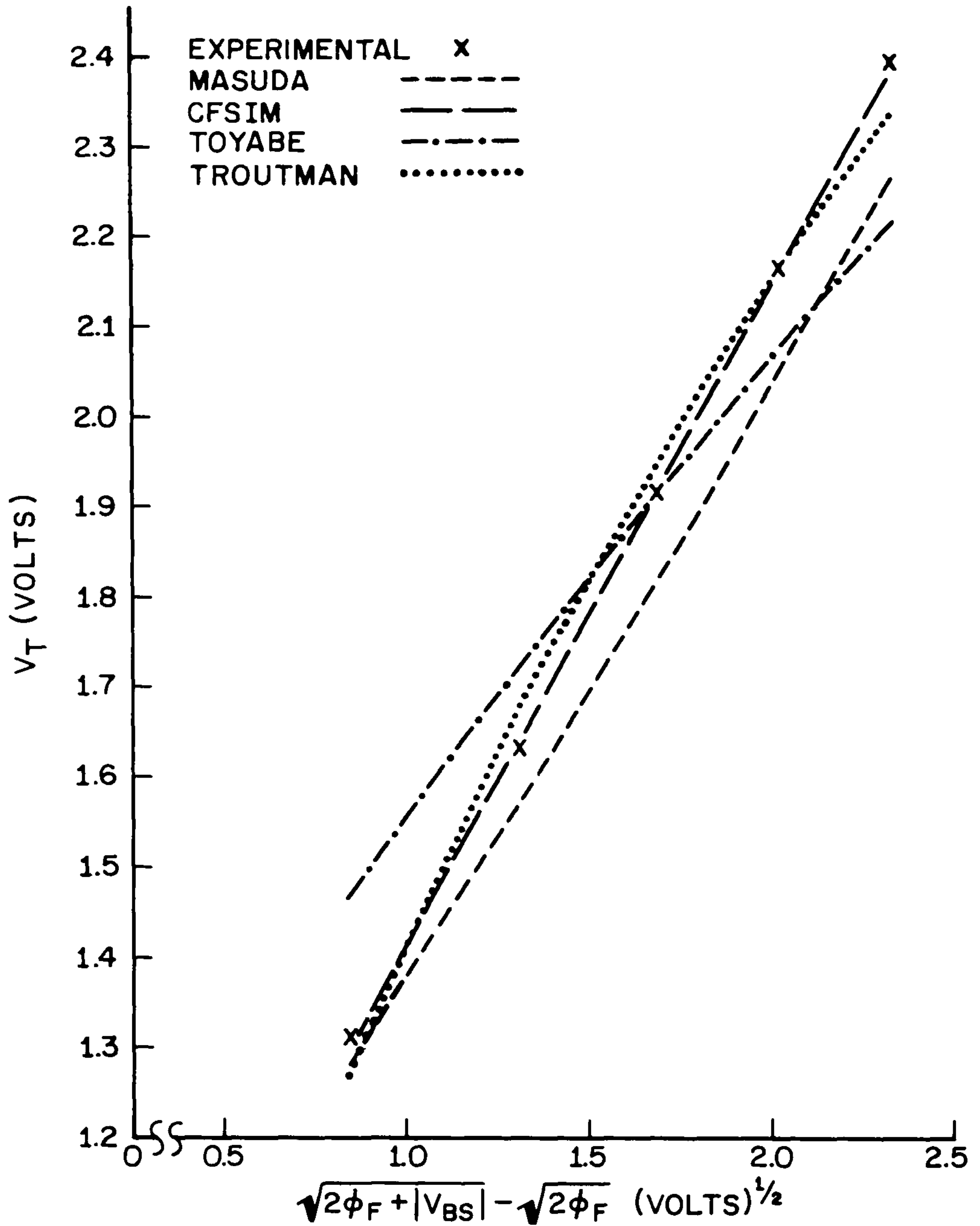


CIRCUIT WIRING
USED TO GET THE THRESHOLD VOLTAGE
FIGURE 4



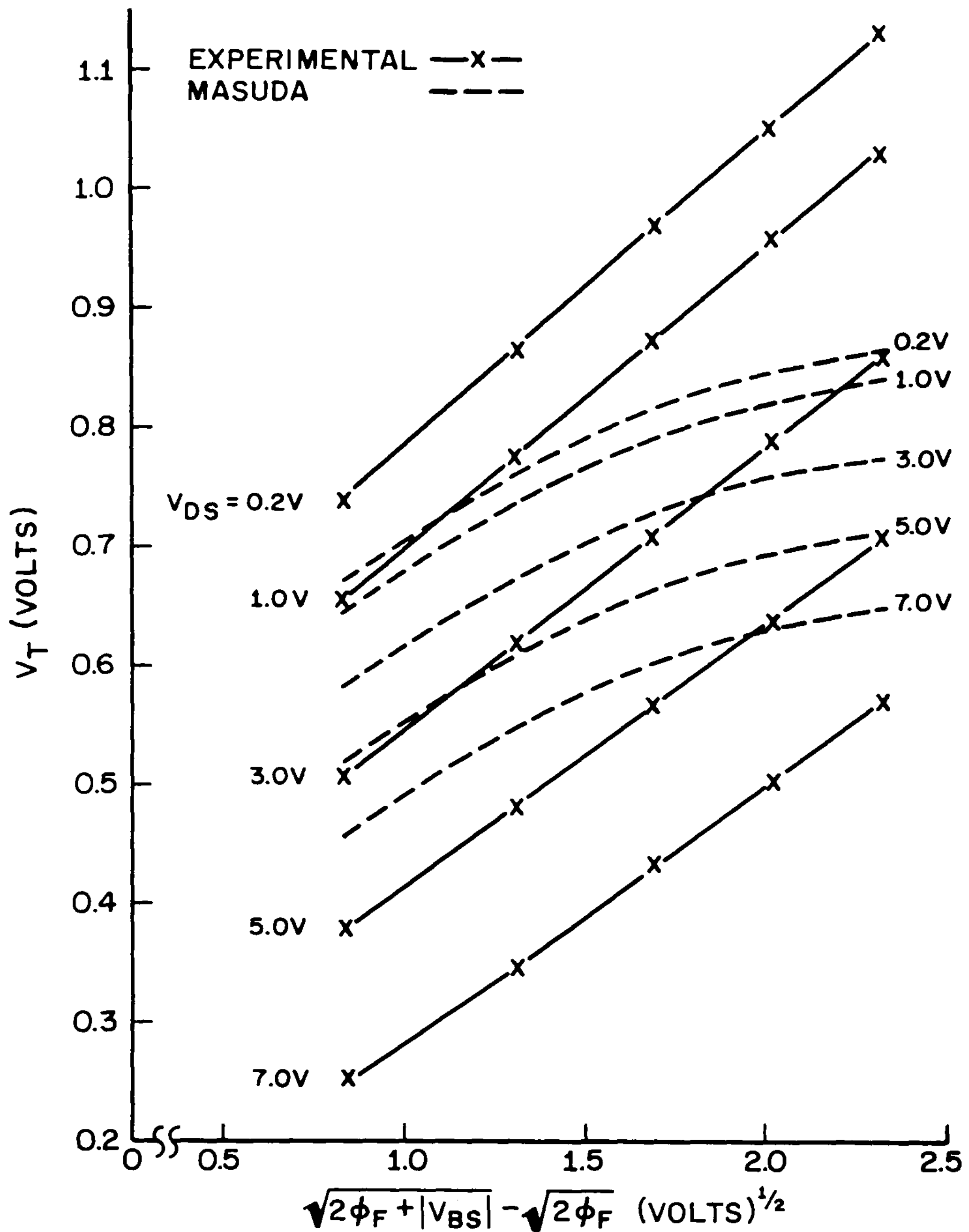
EXPERIMENTAL POINTS AND THE GENERAL CALCULATED CURVE FOR THE FOUR MODELS OF V_T VERSUS $\sqrt{2\phi_F + |V_{BS}|} - \sqrt{2\phi_F}$ AT ANY V_{DS} FOR A WIDE LONG-CHANNEL DEVICE

FIGURE 5

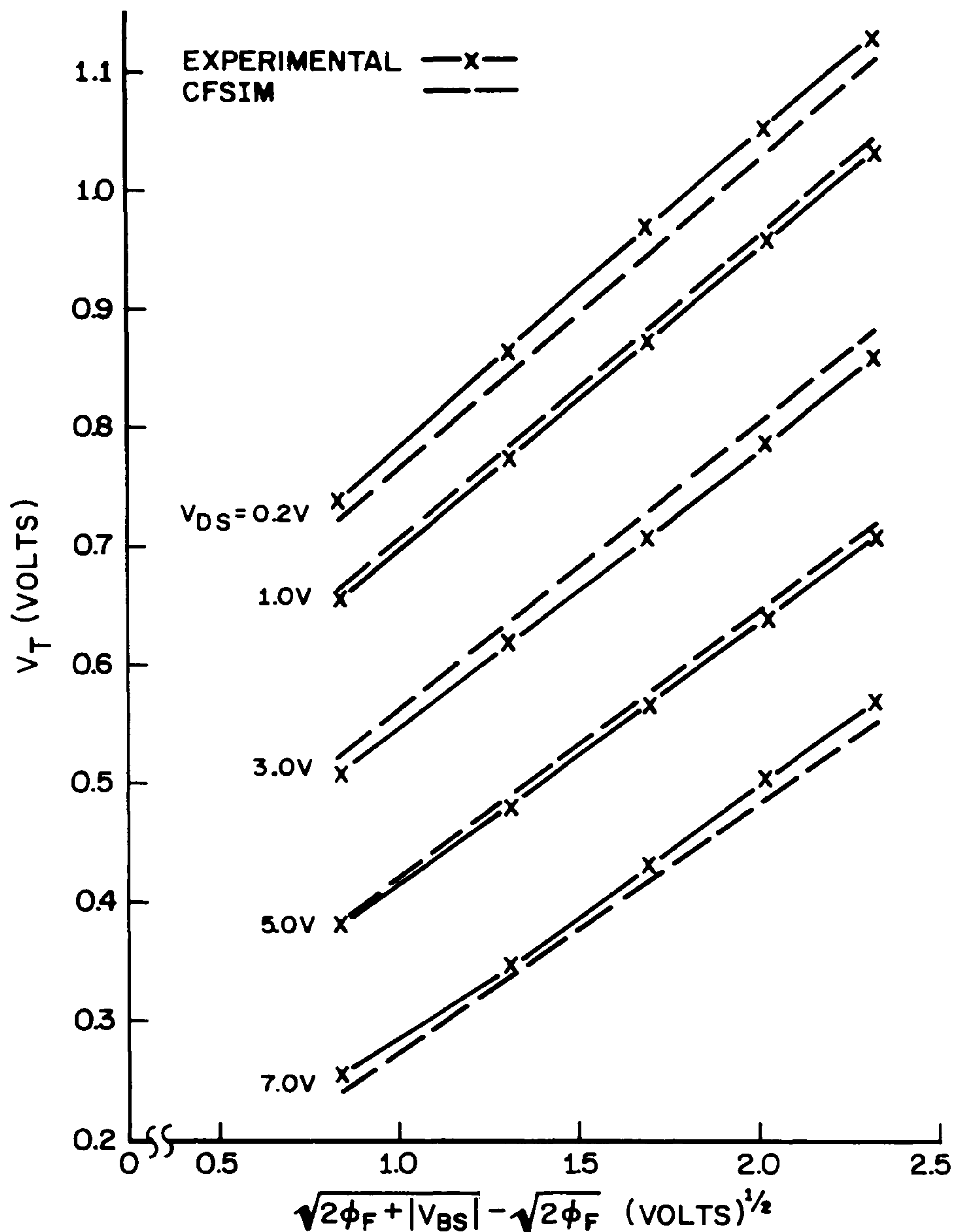


EXPERIMENTAL POINTS AND CALCULATED CURVES FOR THE FOUR MODELS OF V_T VERSUS $\sqrt{2\phi_F + |V_{BS}|} - \sqrt{2\phi_F}$ AT V_{DS} EQUAL TO 0.2 VOLTS FOR A NARROW LONG-CHANNEL DEVICE

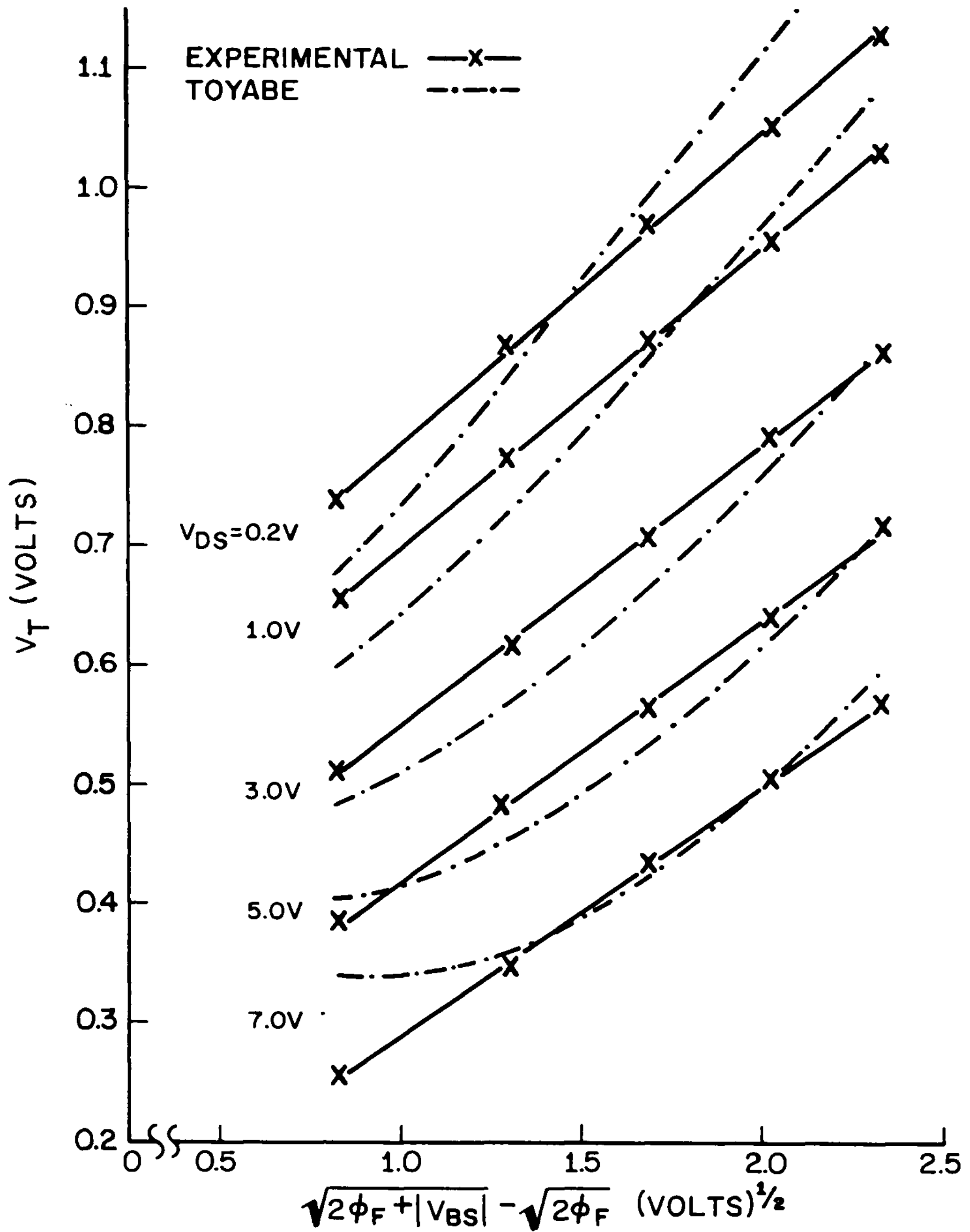
FIGURE 6



EXPERIMENTAL POINTS AND MASUDA'S CALCULATED CURVES
OF V_T VERSUS $\sqrt{2\phi_F + |V_{BS}|} - \sqrt{2\phi_F}$
AT VARIOUS DRAIN-TO-SOURCE VOLTAGES FOR A WIDE SHORT-CHANNEL DEVICE
FIGURE 7

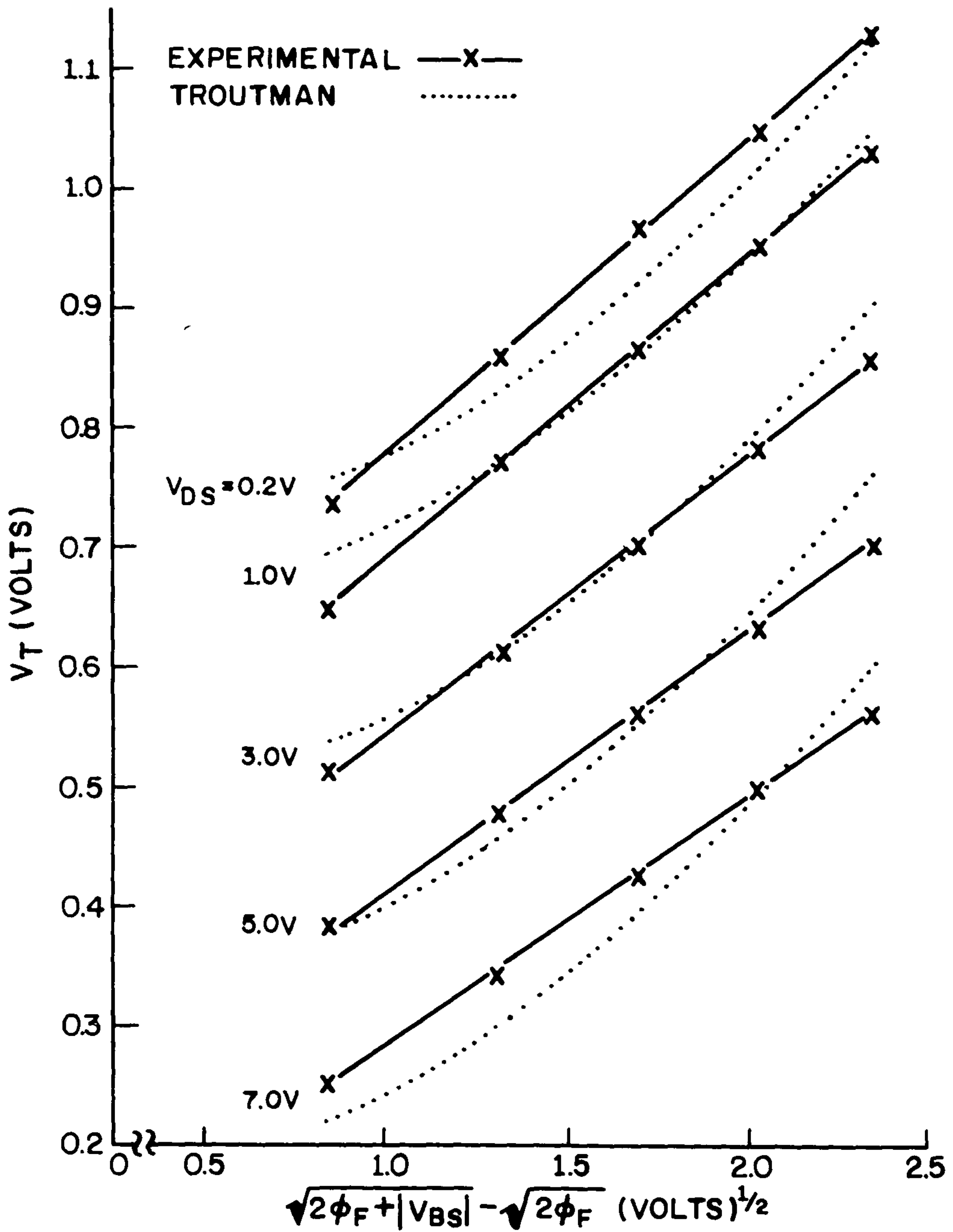


EXPERIMENTAL POINTS AND THE CFSIM CALCULATED CURVES
OF V_T VERSUS $\sqrt{2\phi_F+|V_{BS}|}-\sqrt{2\phi_F}$
AT VARIOUS DRAIN-TO-SOURCE VOLTAGES FOR A WIDE SHORT-CHANNEL DEVICE
FIGURE 8



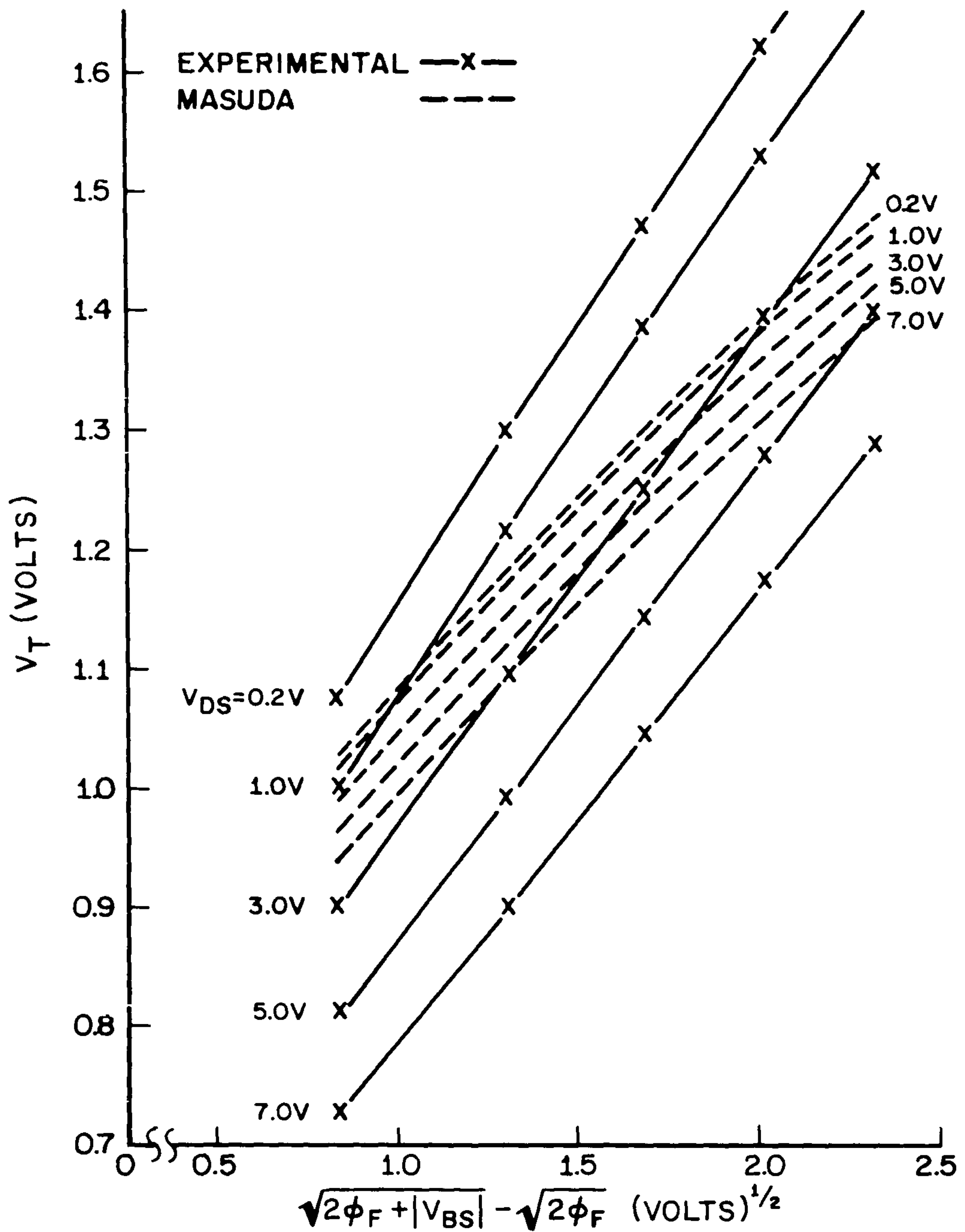
EXPERIMENTAL POINTS AND TOYABE'S CALCULATED CURVES OF V_T VERSUS $\sqrt{2\phi_F+|V_{BS}|}-\sqrt{2\phi_F}$ AT VARIOUS DRAIN-TO-SOURCE VOLTAGES FOR A WIDE SHORT-CHANNEL DEVICE

FIGURE 9



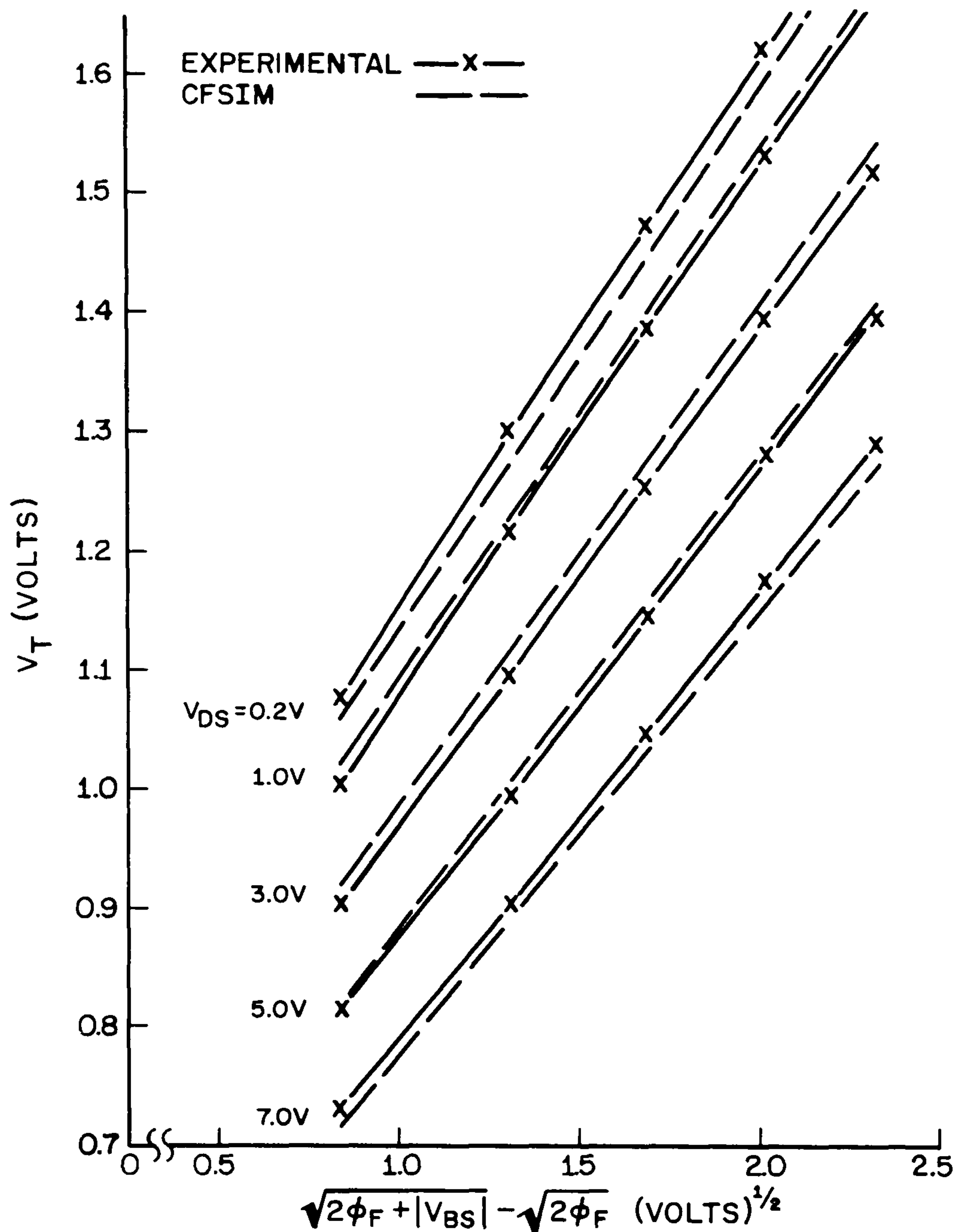
EXPERIMENTAL POINTS AND TROUTMAN'S CALCULATED CURVES OF V_T VERSUS $\sqrt{2\phi_F+|V_{BS}|}-\sqrt{2\phi_F}$ AT VARIOUS DRAIN-TO-SOURCE VOLTAGES FOR A WIDE SHORT-CHANNEL DEVICE

FIGURE 10



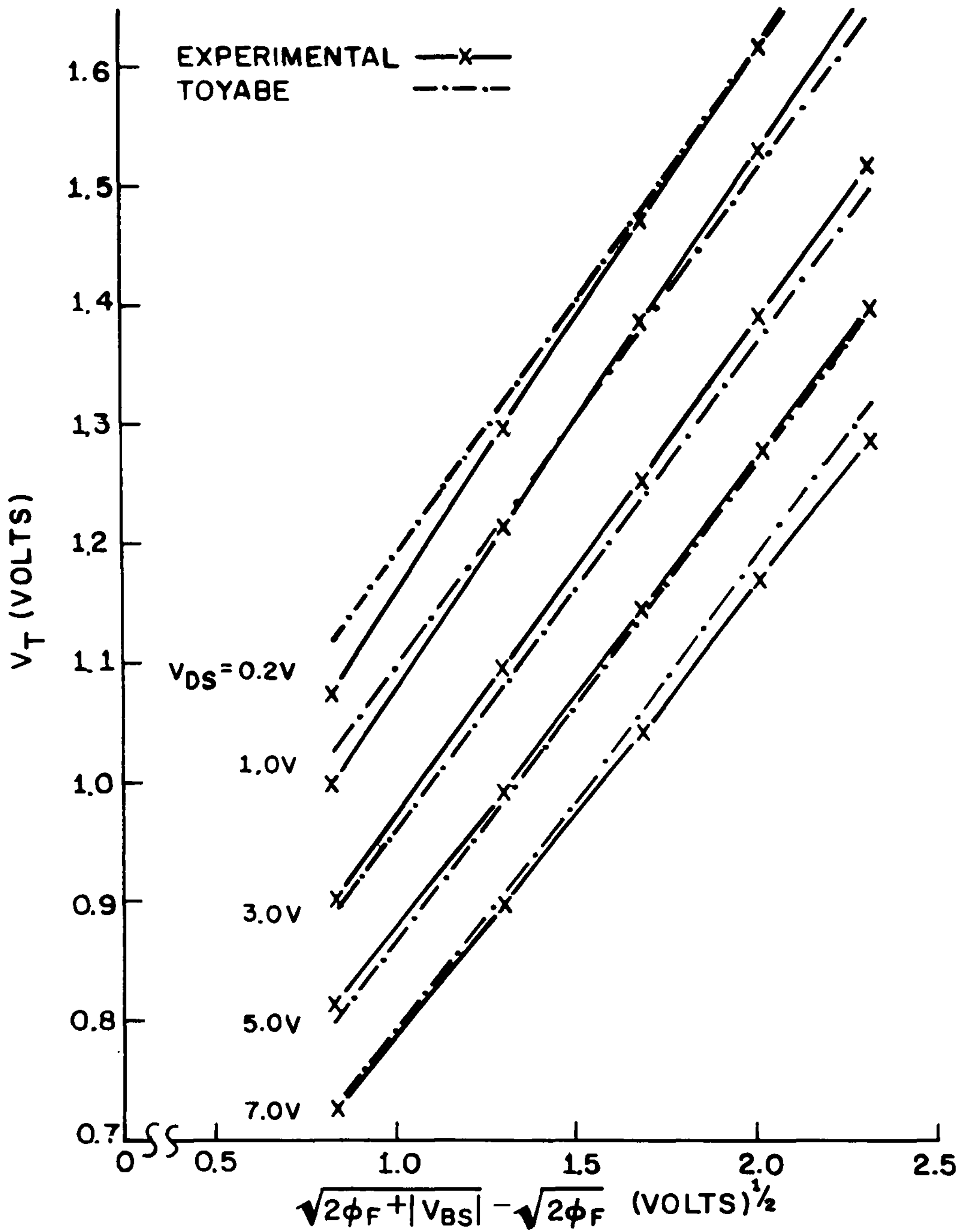
EXPERIMENTAL POINTS AND MASUDA'S CALCULATED CURVES OF V_T VERSUS $\sqrt{2\phi_F+|V_{BS}|}-\sqrt{2\phi_F}$ AT VARIOUS DRAIN-TO-SOURCE VOLTAGES FOR A NARROW SHORT-CHANNEL DEVICE

FIGURE 11



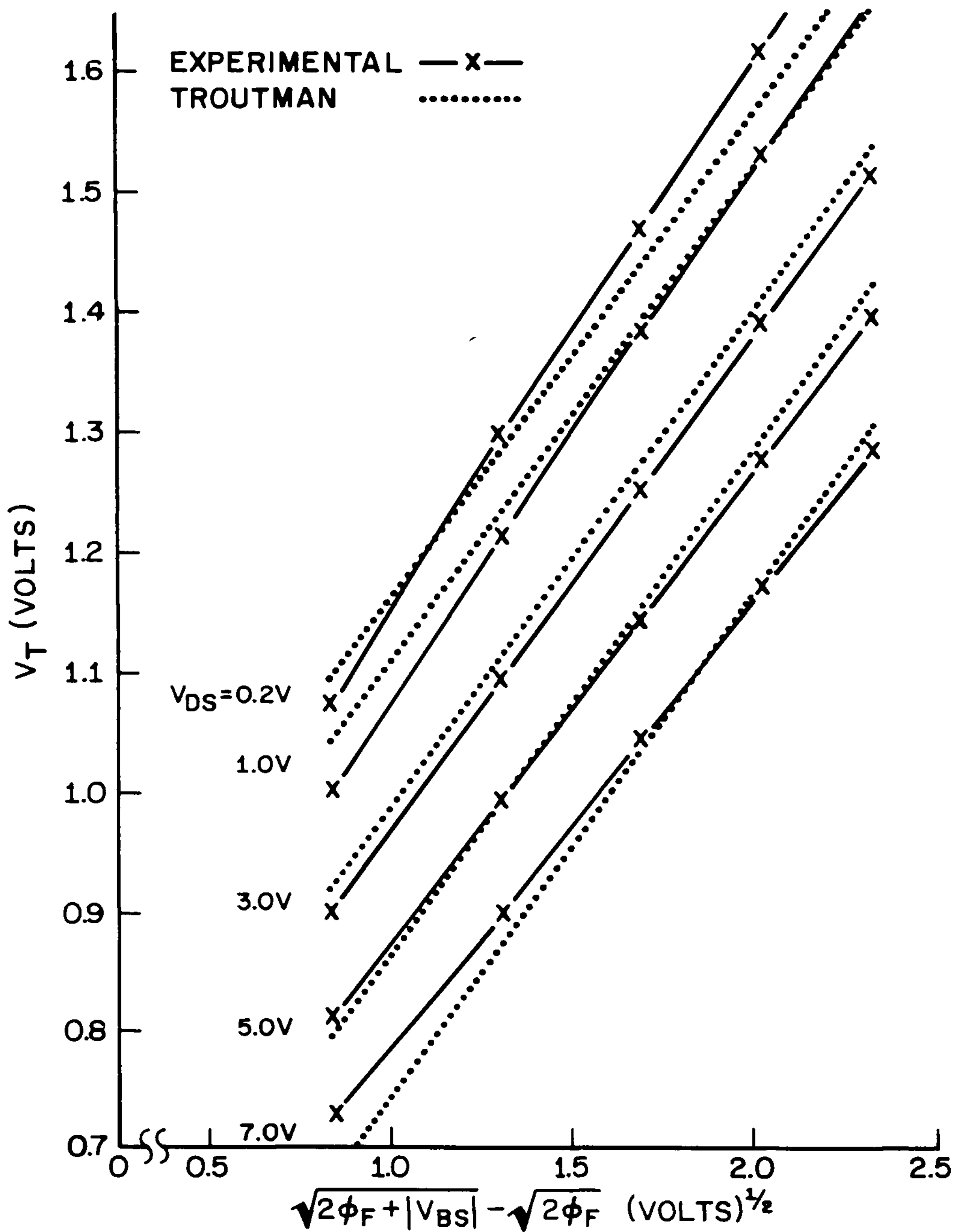
EXPERIMENTAL POINTS AND THE CFSIM CALCULATED CURVES OF V_T VERSUS $\sqrt{2\phi_F+|V_{BS}|}-\sqrt{2\phi_F}$ AT VARIOUS DRAIN-TO-SOURCE VOLTAGES FOR A NARROW SHORT-CHANNEL DEVICE

FIGURE 12

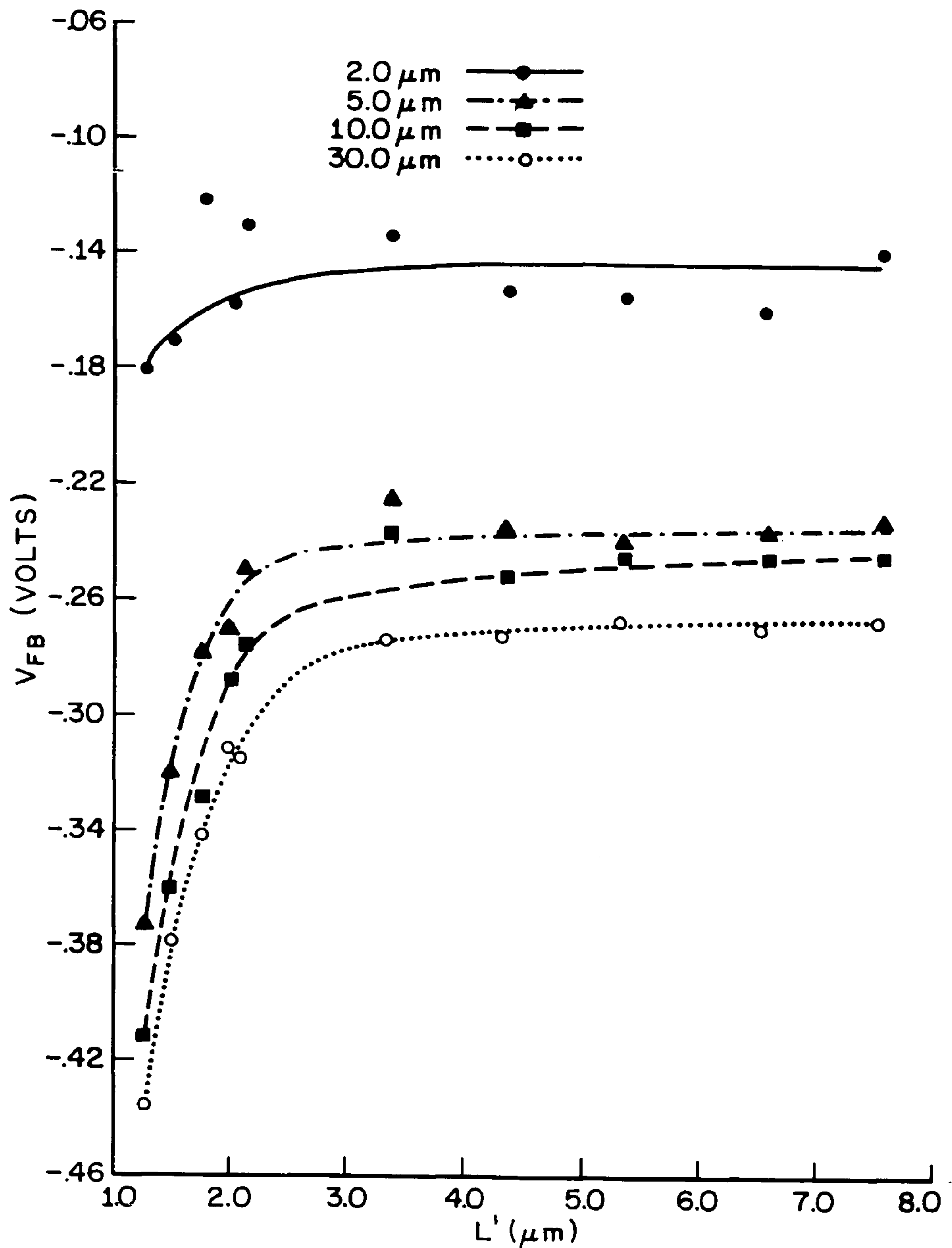


EXPERIMENTAL POINTS AND TOYABE'S CALCULATED CURVES
OF V_T VERSUS $\sqrt{2\phi_F+|V_{BS}|}-\sqrt{2\phi_F}$
AT VARIOUS DRAIN-TO-SOURCE VOLTAGES FOR A NARROW SHORT-CHANNEL DEVICE

FIGURE 13

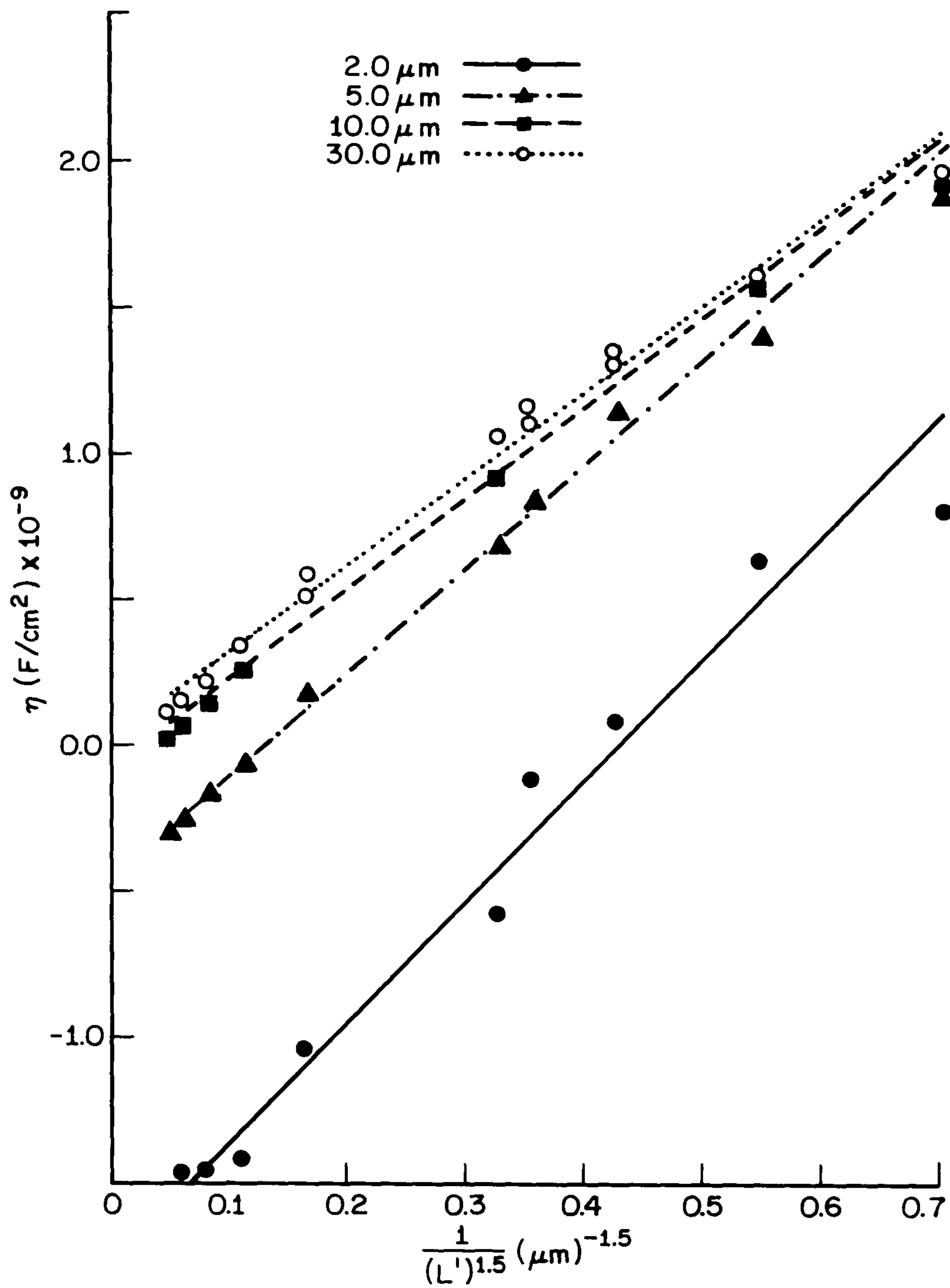


EXPERIMENTAL POINTS AND TROUTMAN'S CALCULATED CURVES
OF V_T VERSUS $\sqrt{2\phi_F+|V_{BS}|}-\sqrt{2\phi_F}$
AT VARIOUS DRAIN-TO-SOURCE VOLTAGES FOR A NARROW SHORT-CHANNEL DEVICE
FIGURE 14



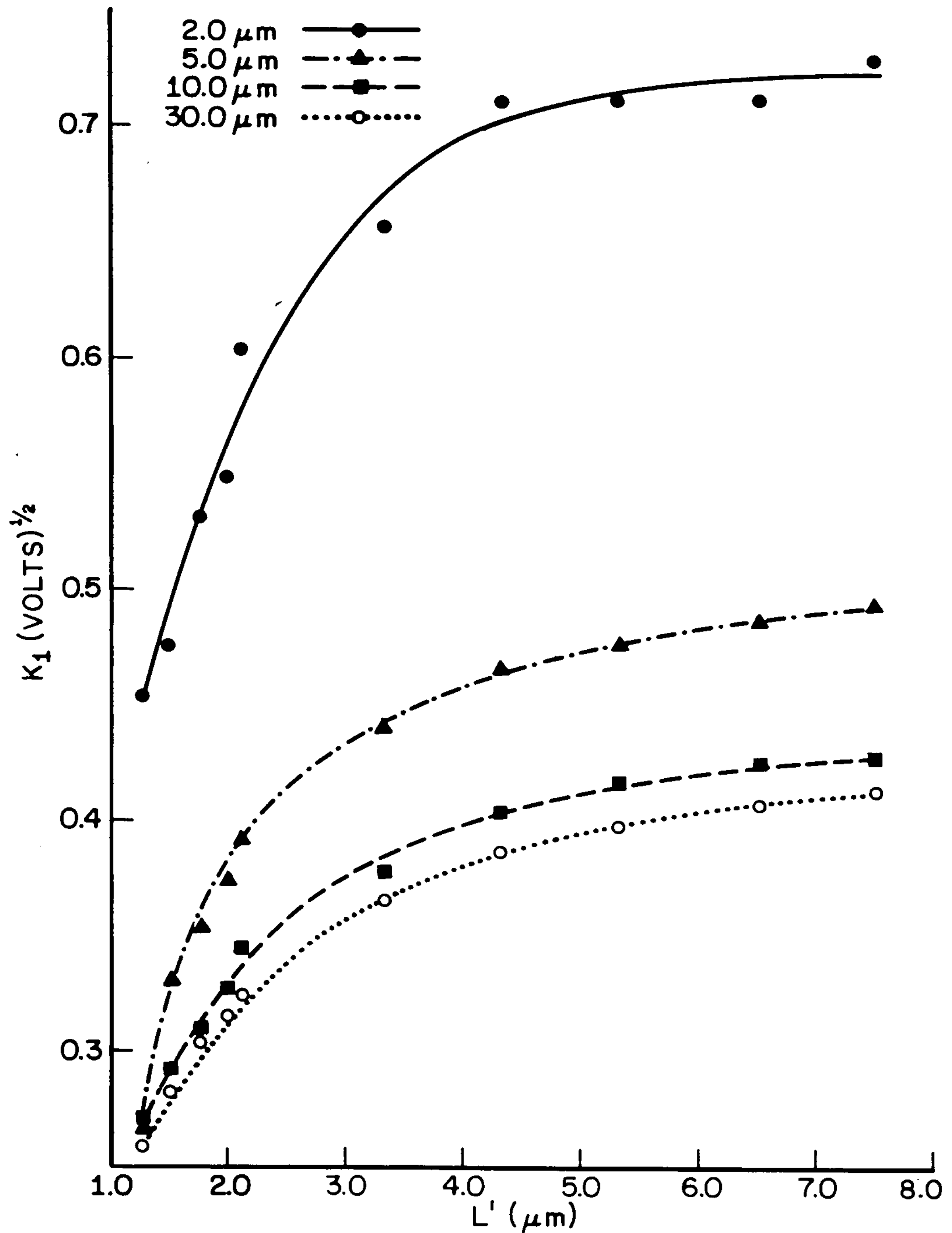
V_{FB} VERSUS L' FOR VARIOUS WIDTHS FOR MASUDA'S MODEL

FIGURE 15



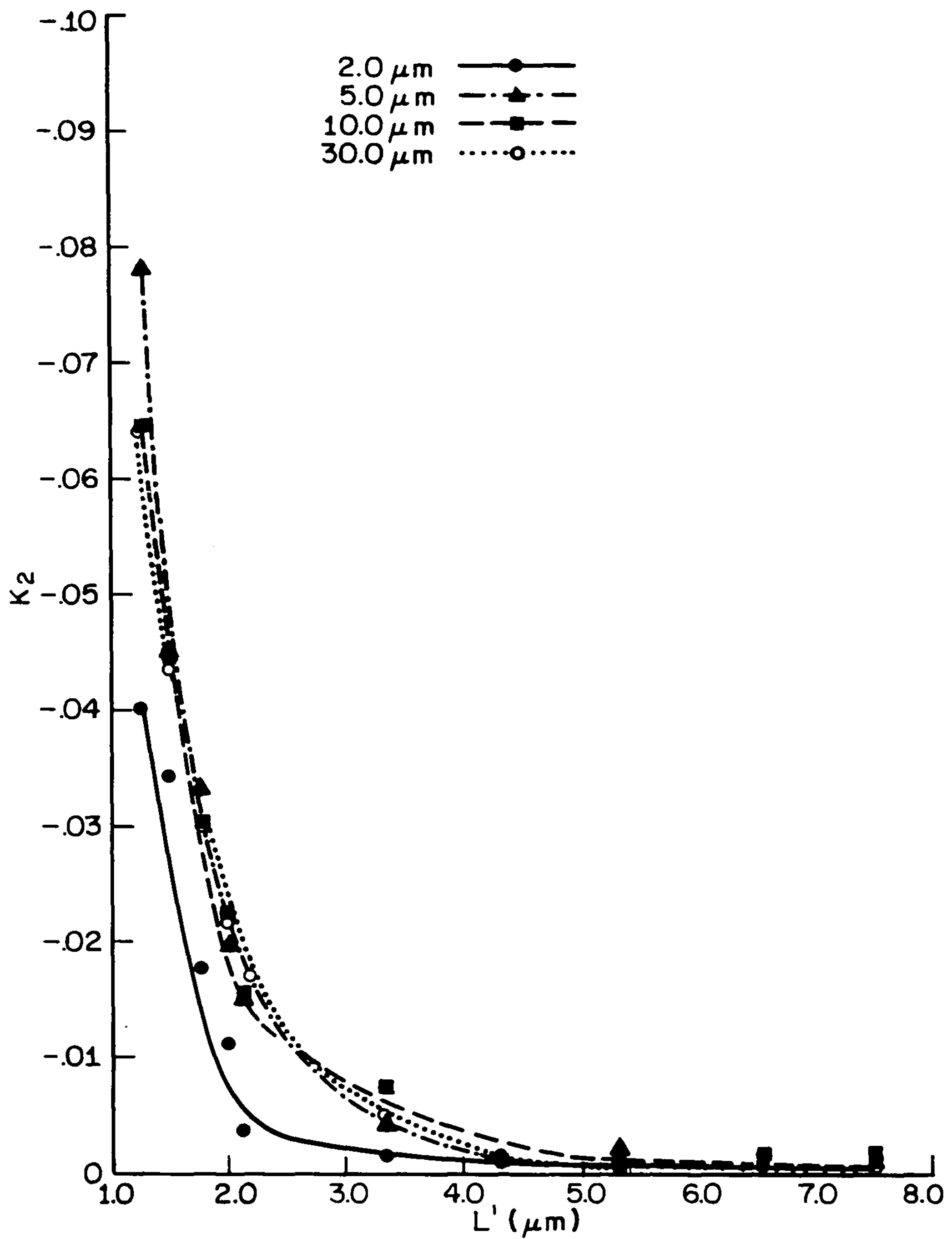
ETA VERSUS $L'^{(-1.5)}$ FOR VARIOUS WIDTHS FOR MASUDA'S MODEL

FIGURE 16



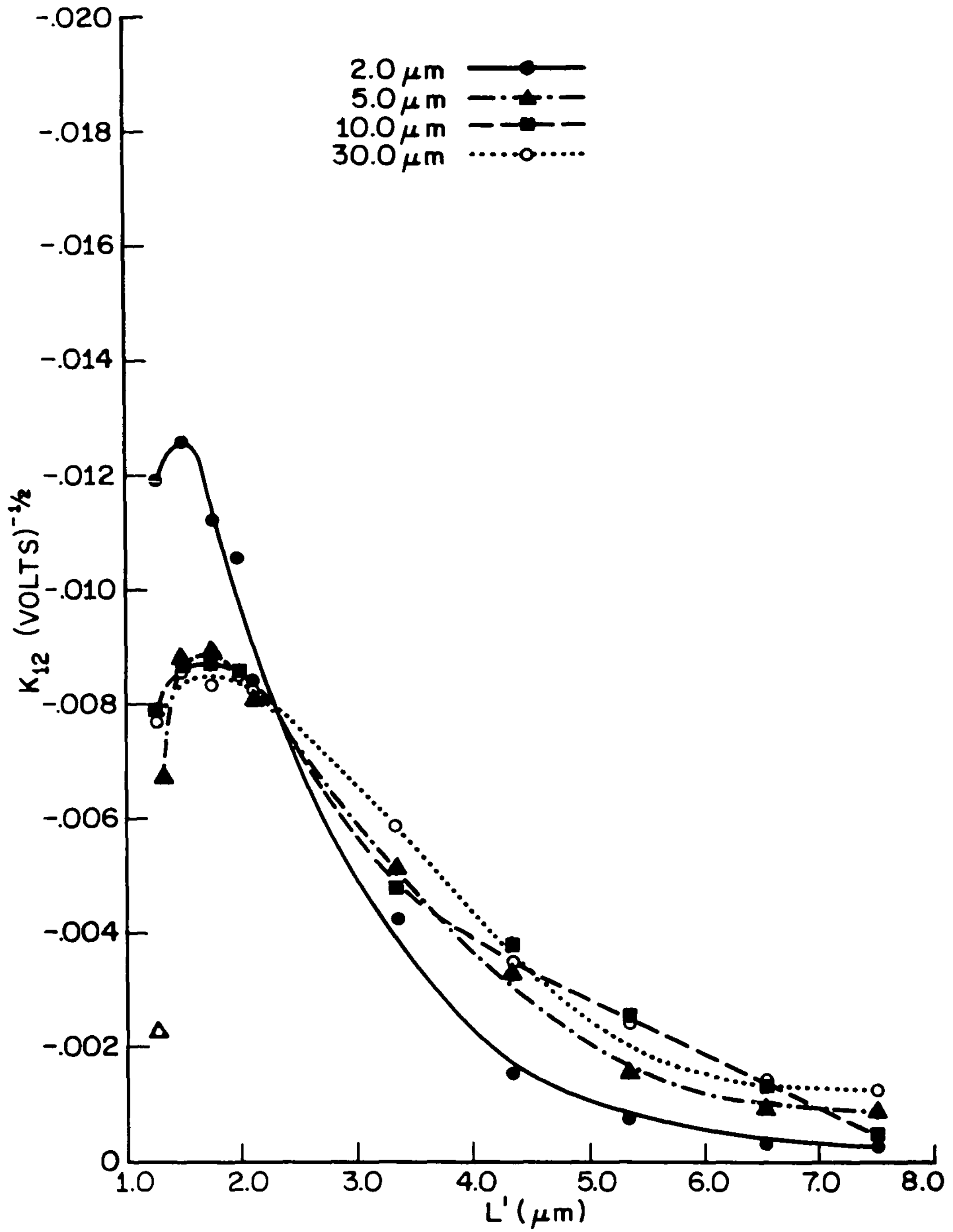
K_1 VERSUS L' FOR VARIOUS WIDTHS FOR THE CFSIM MODEL

FIGURE 17



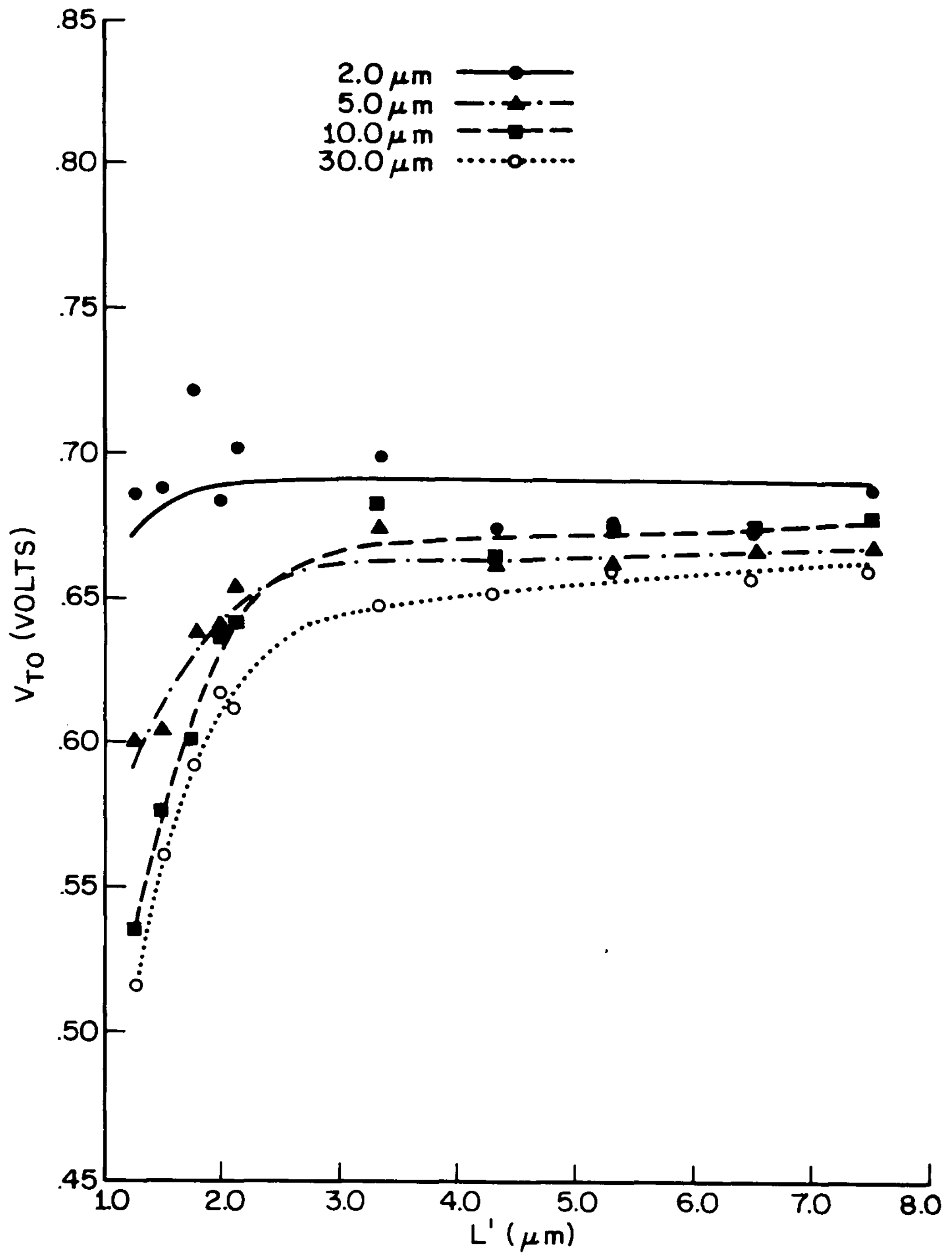
K_2 VERSUS L' FOR VARIOUS WIDTHS FOR THE CFSIM MODEL

FIGURE 18



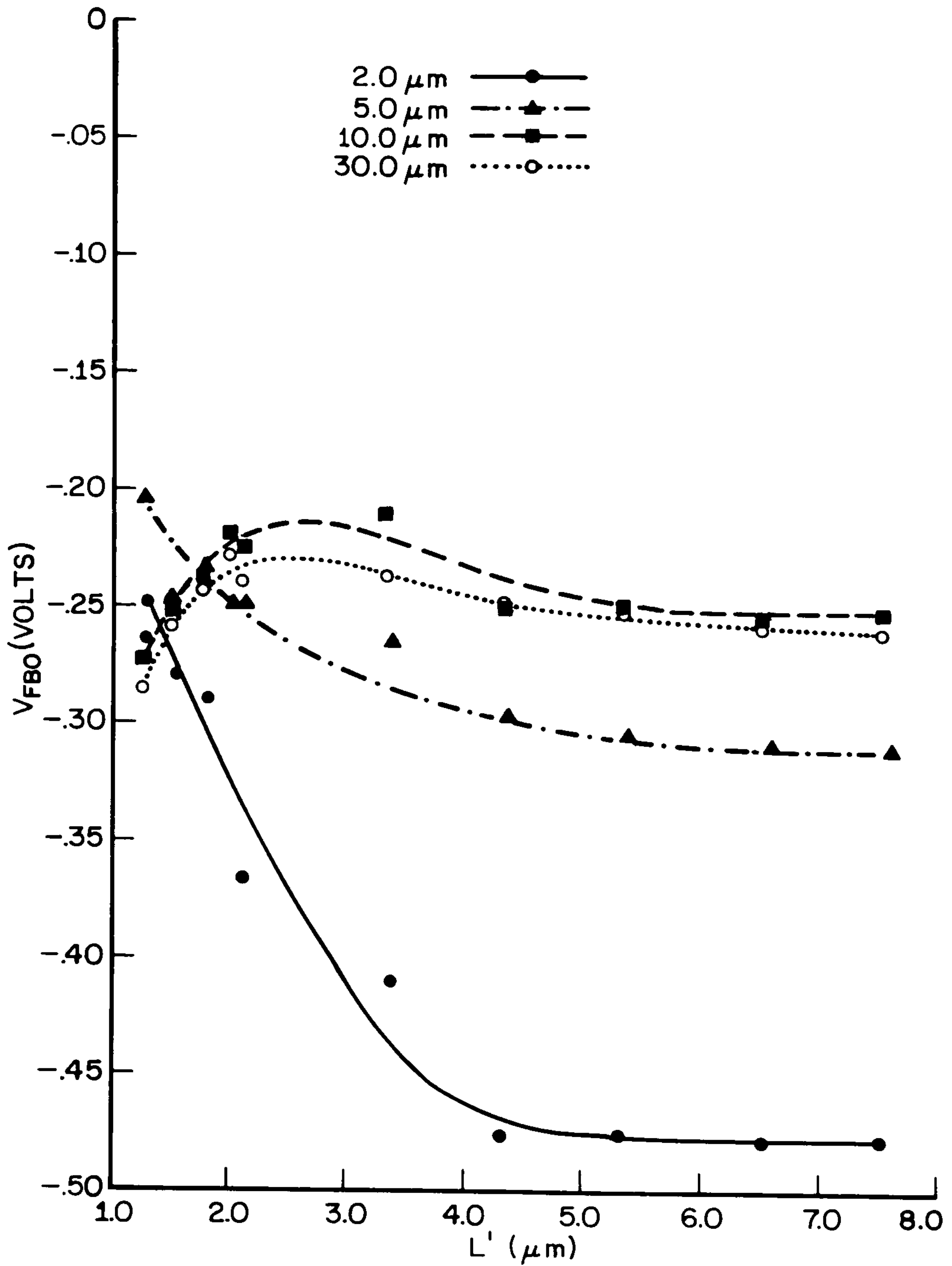
K_{12} VERSUS L' FOR VARIOUS WIDTHS FOR THE CFSIM MODEL

FIGURE 19



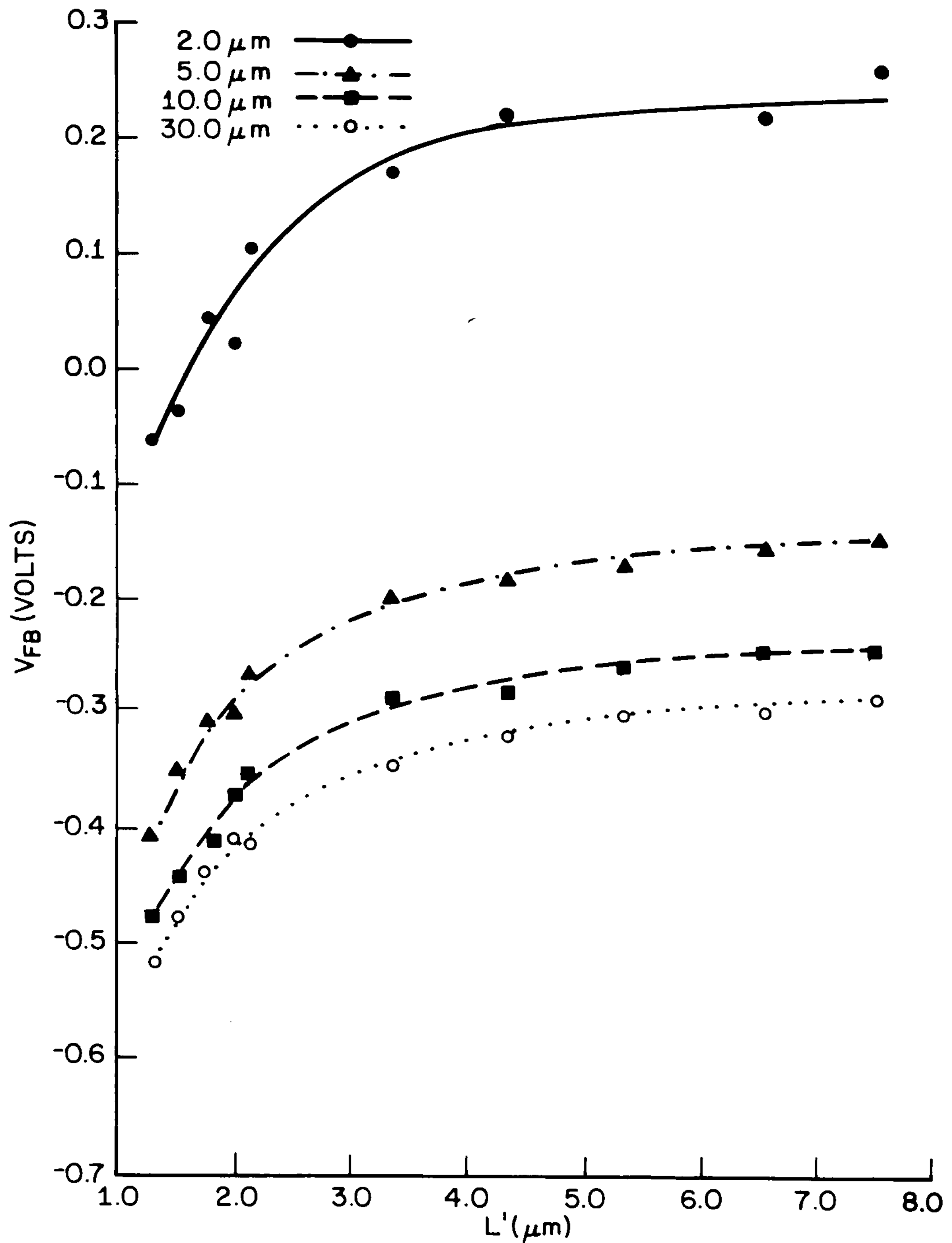
V_{TO} VERSUS L' FOR VARIOUS WIDTHS FOR THE CFSIM MODEL

FIGURE 20



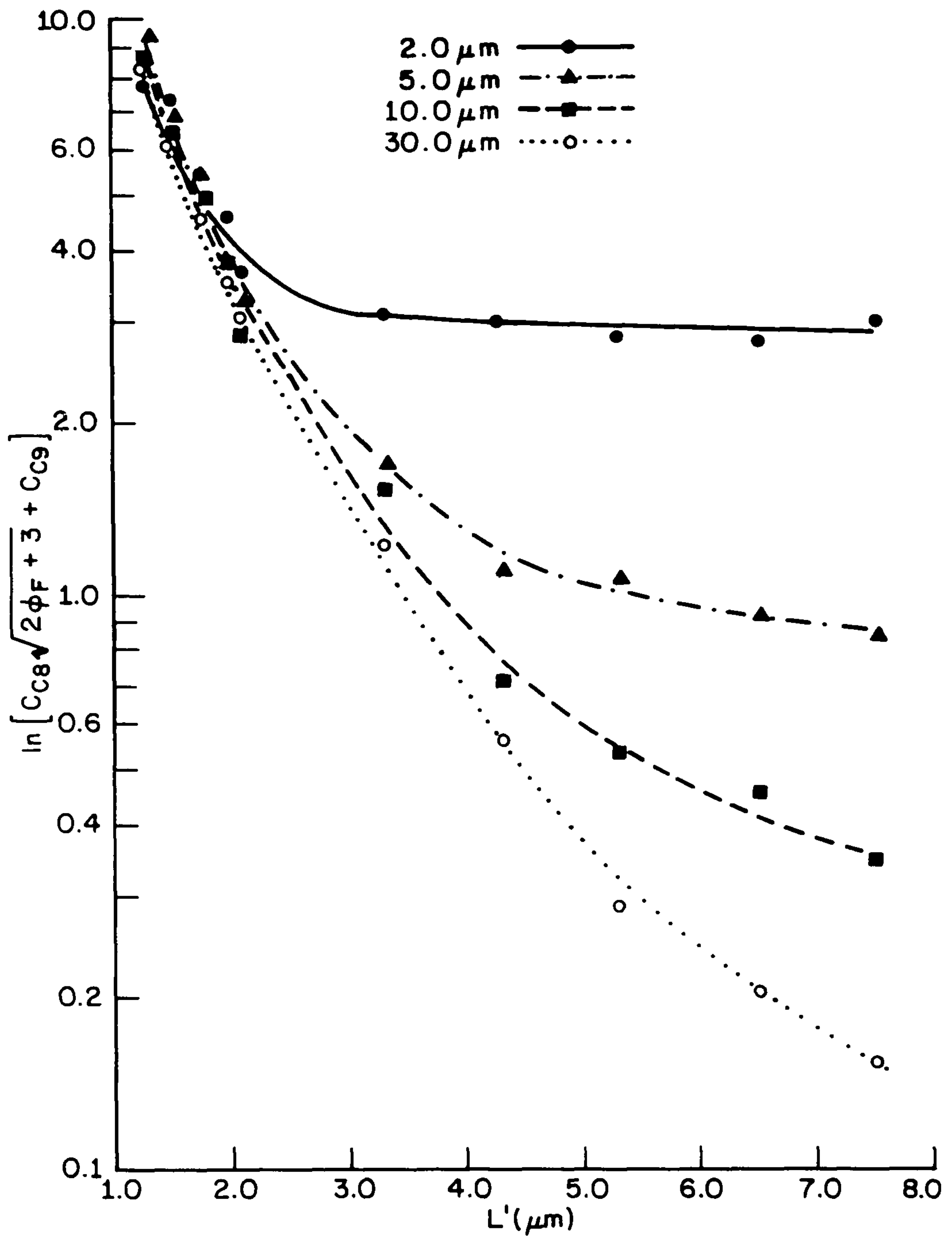
V_{FBO} VERSUS L' FOR VARIOUS WIDTHS FOR THE CFSIM MODEL

FIGURE 21



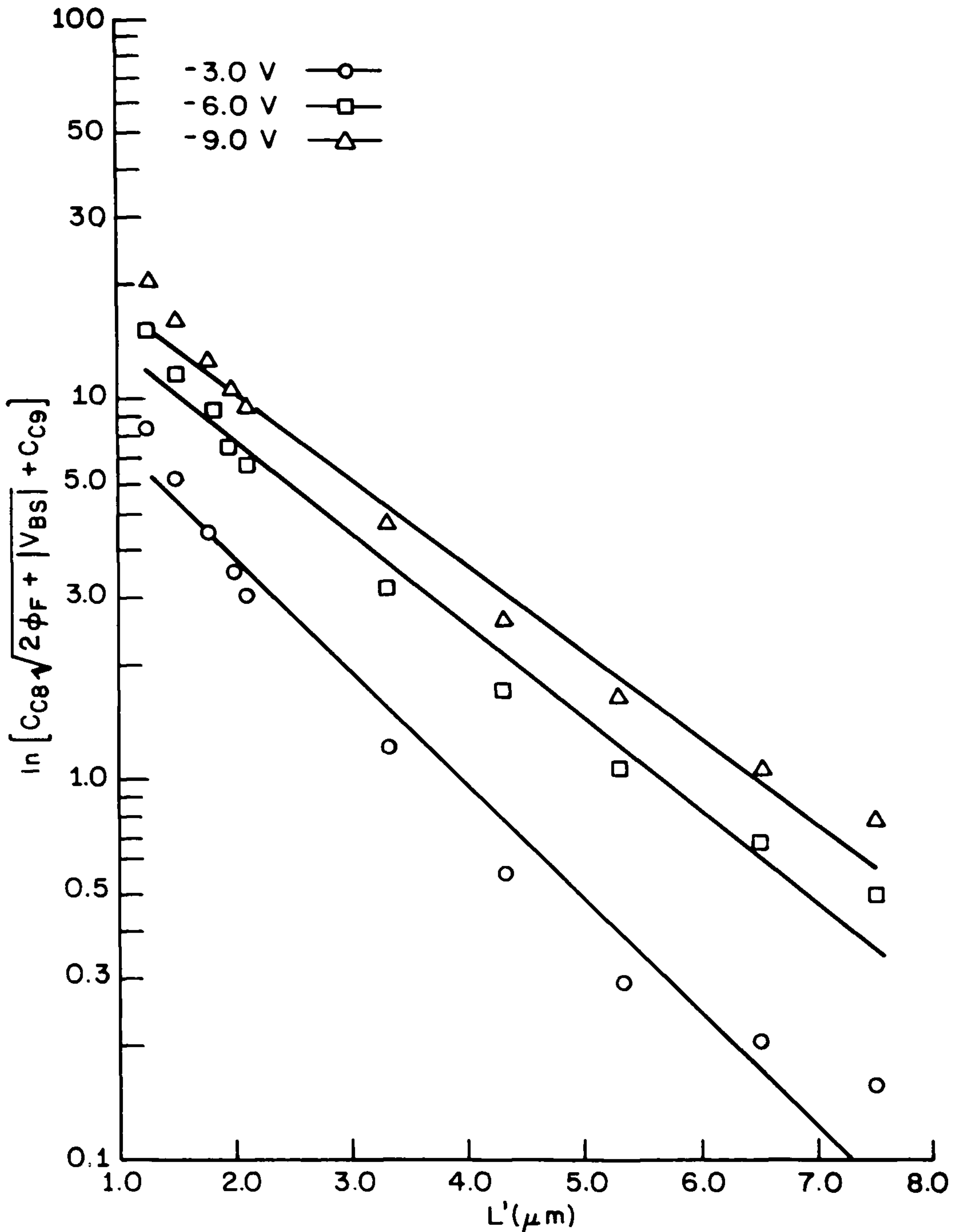
V_{FB} VERSUS L' FOR VARIOUS WIDTHS FOR TOYABE'S MODEL

FIGURE 22



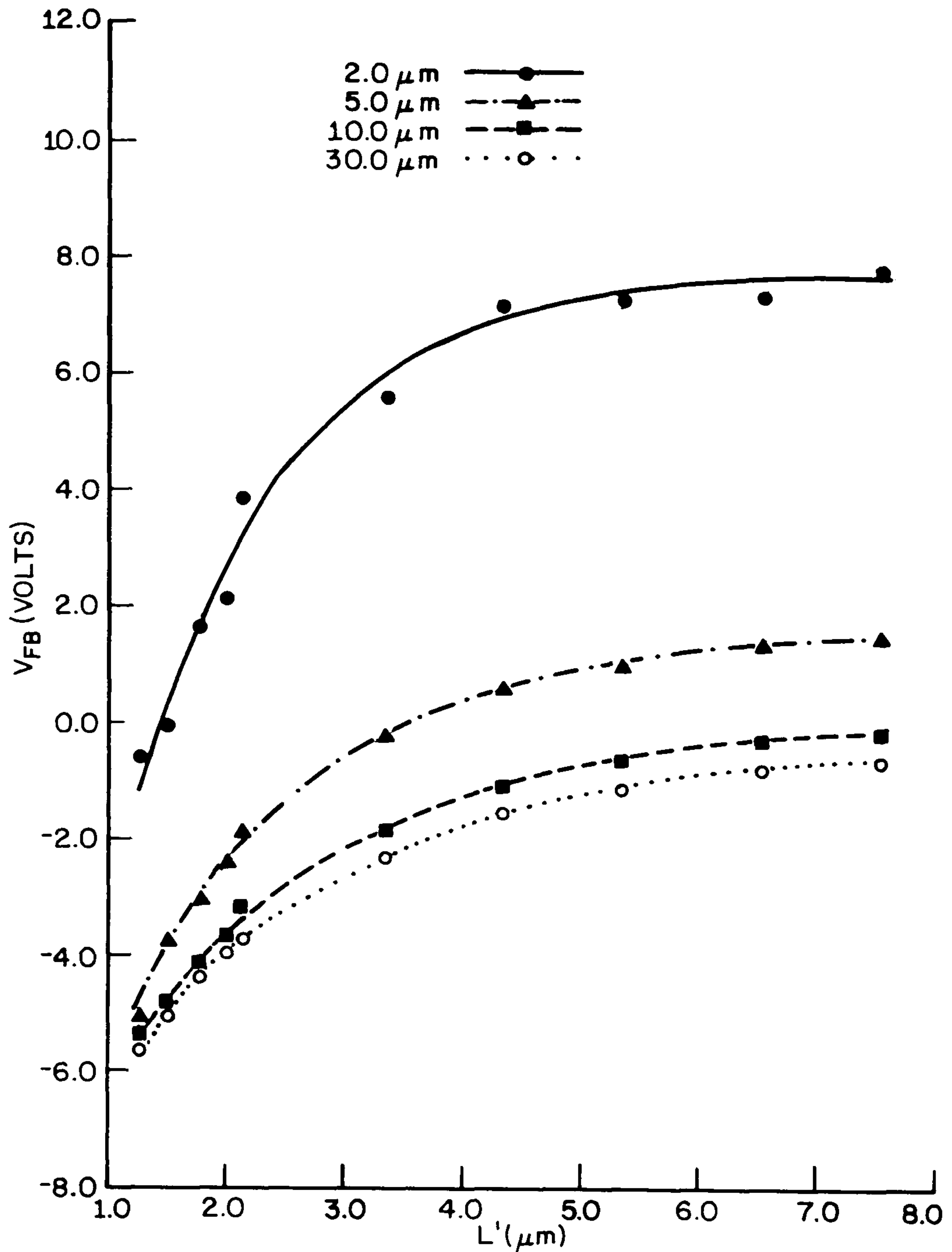
$\mathrm{Ln}\left[C_{C8}\sqrt{2\phi_F+3}+C_{C9}\right]$ VERSUS L' AT VBS EQUAL TO -3 VOLTS FOR VARIOUS WIDTHS FOR TOYABE'S MODEL

FIGURE 23



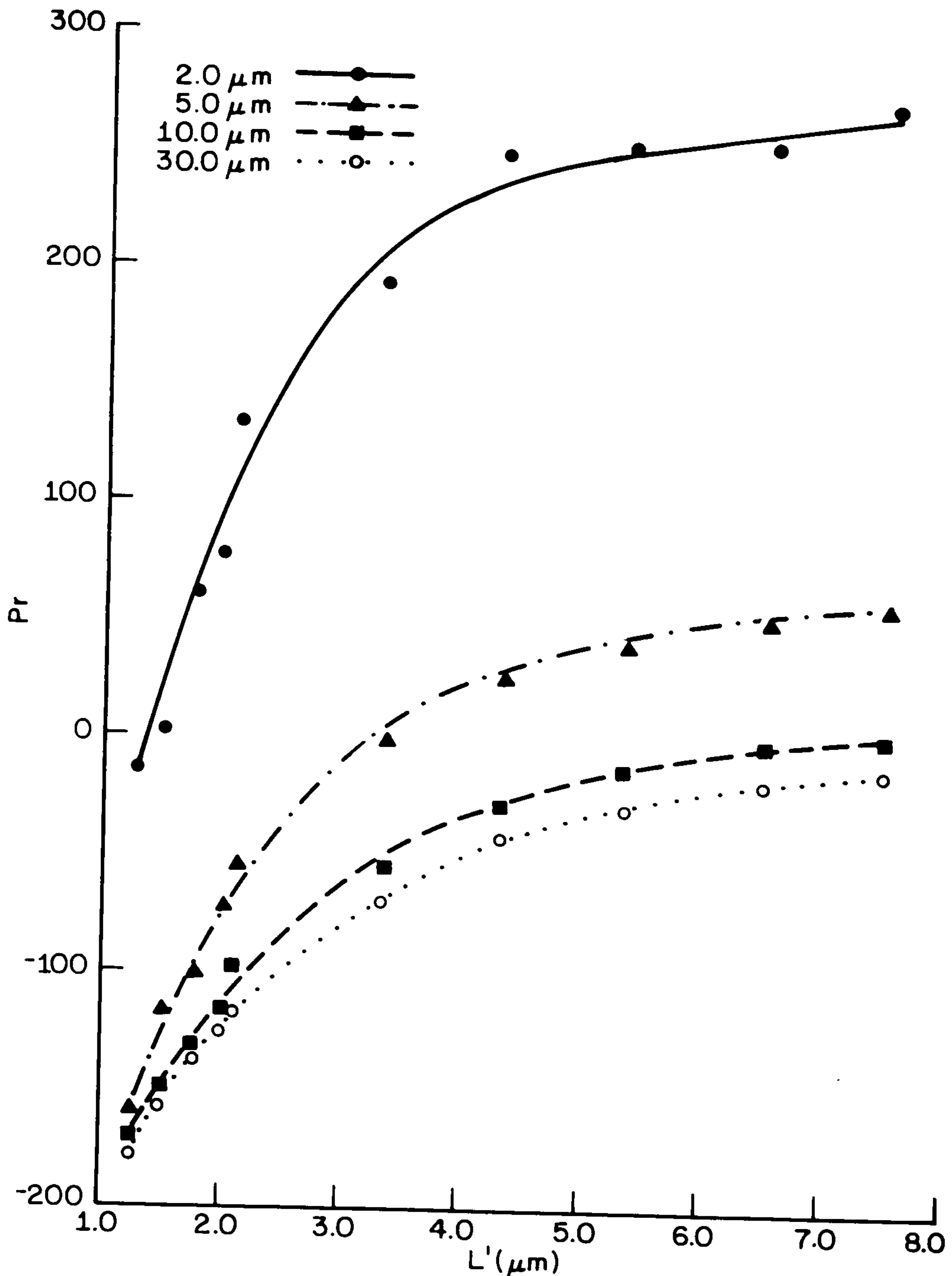
$Ln\left[C_{C8}\sqrt{2\phi_F + |V_{BS}|} + C_{C9}\right]$ VERSUS L' FOR W EQUAL TO 30μm AT VARIOUS VALUES OF V_{BS} FOR TOYABE'S MODEL

FIGURE 24



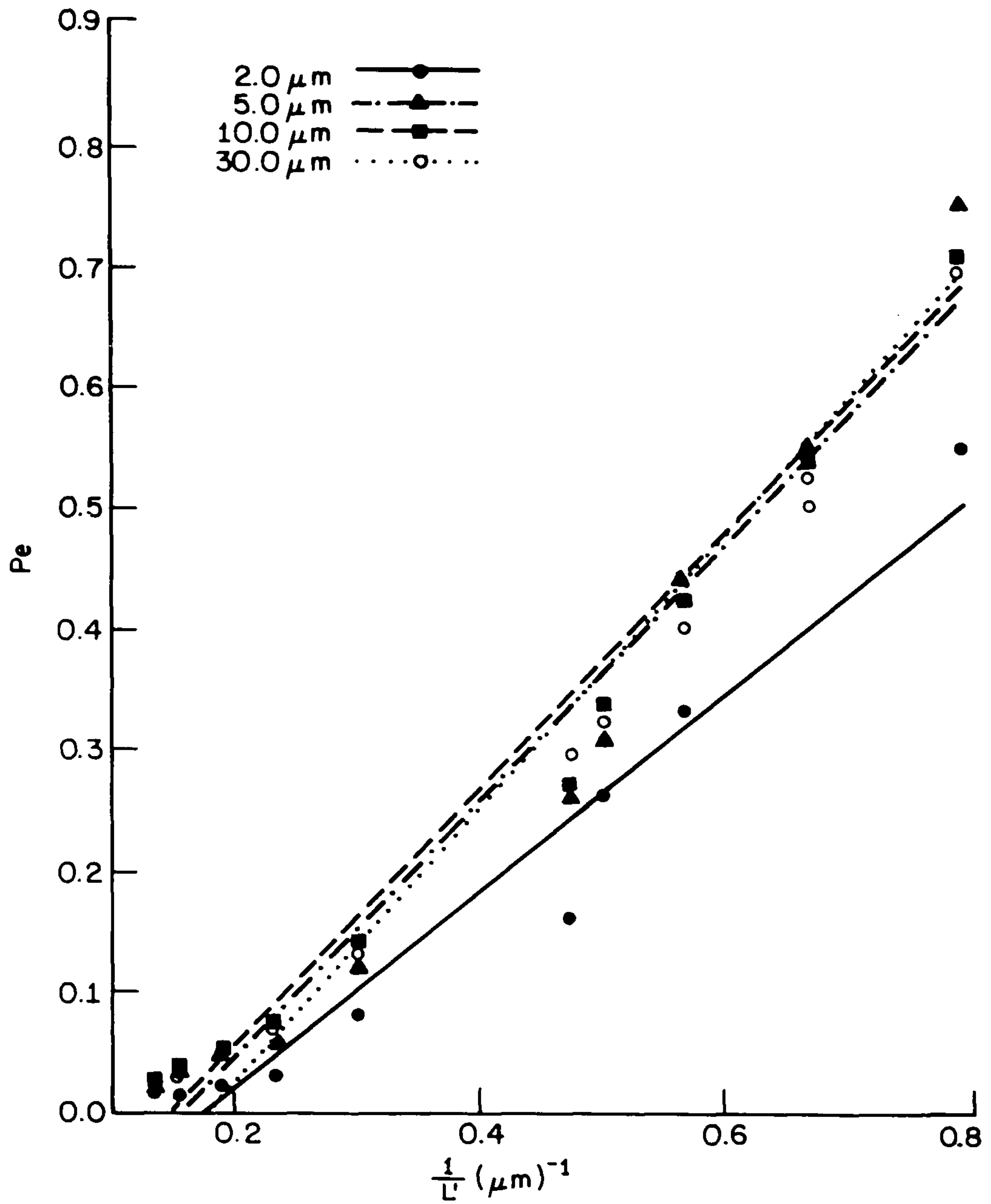
V_{FB} VERSUS L' FOR VARIOUS WIDTHS FOR TROUTMAN'S MODEL

FIGURE 25



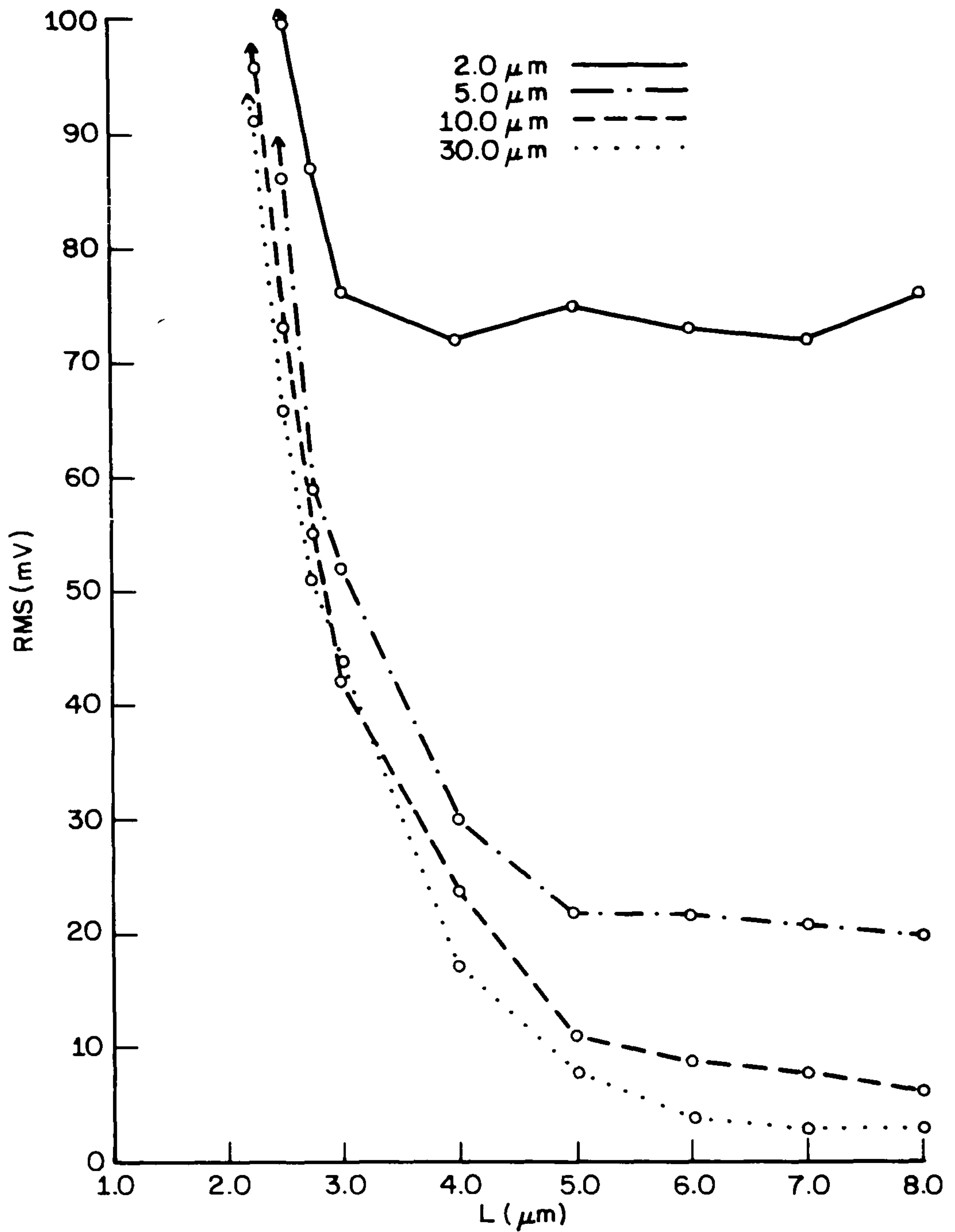
Pr VERSUS L' FOR VARIOUS WIDTHS FOR TROUTMAN'S MODEL

FIGURE 26



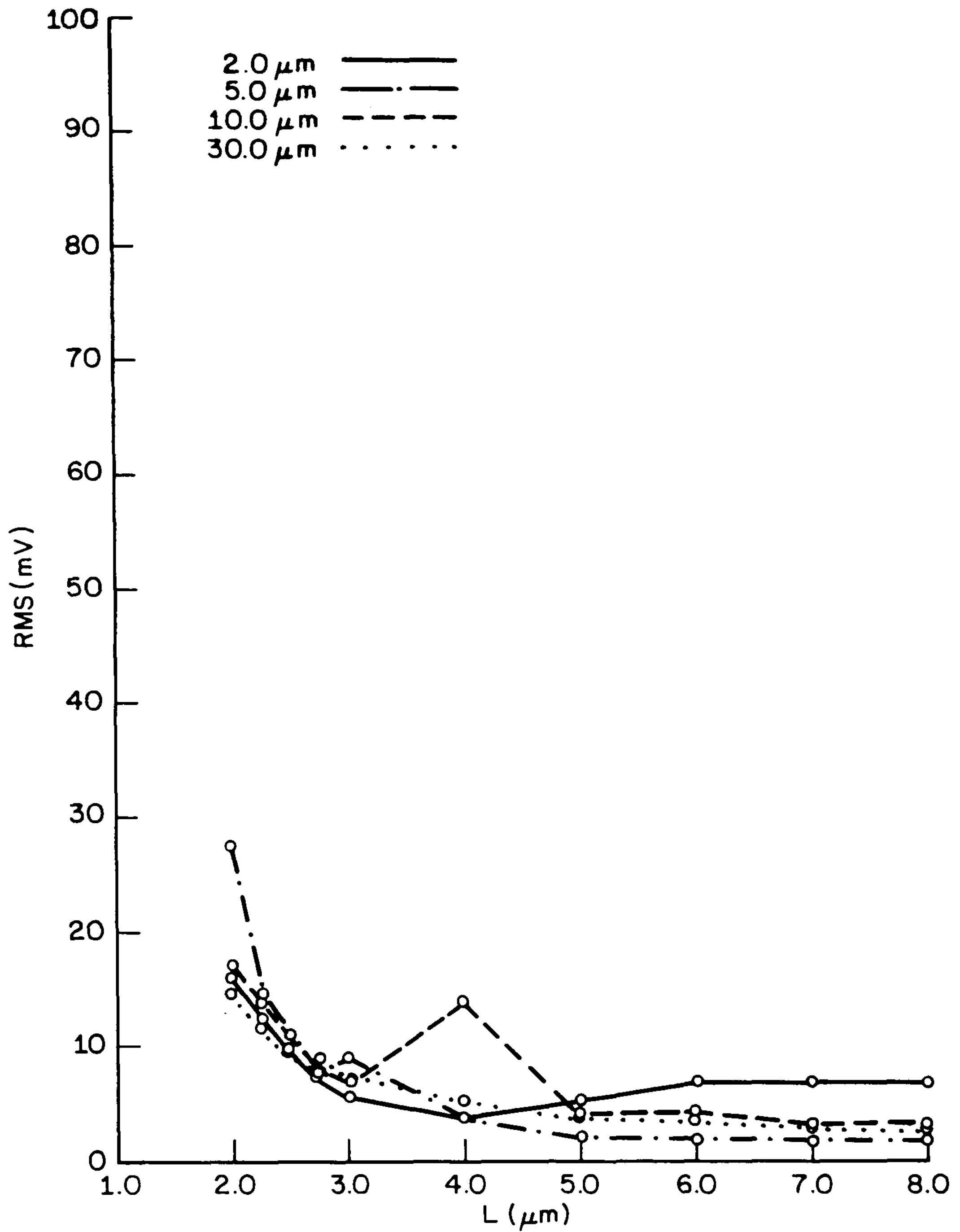
Pe VERSUS L' FOR VARIOUS WIDTHS FOR TROUTMAN'S MODEL

FIGURE 27

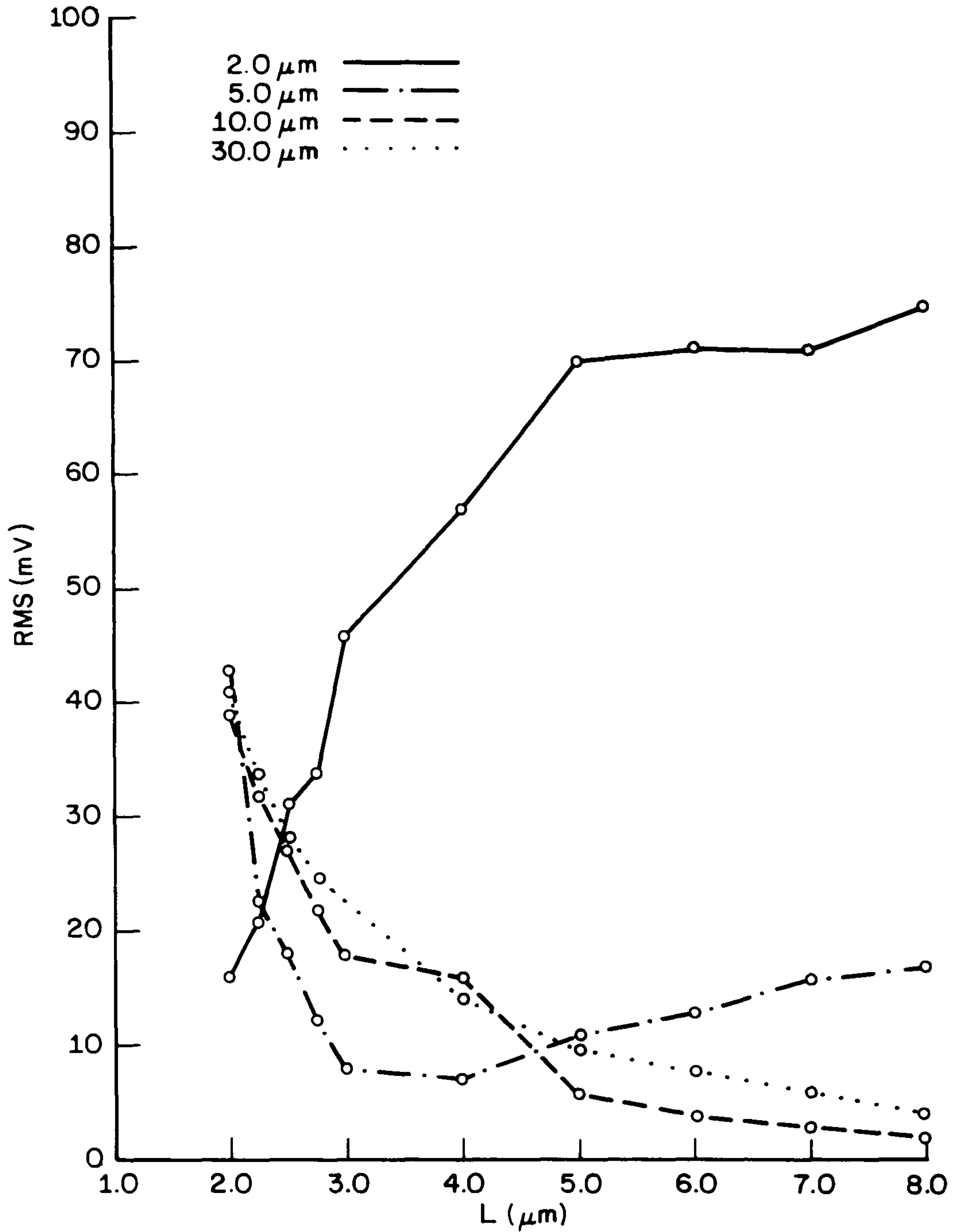


THE RMS DEVIATIONS VERSUS L FOR VARIOUS WIDTHS FOR MASUDA'S MODEL

FIGURE 28

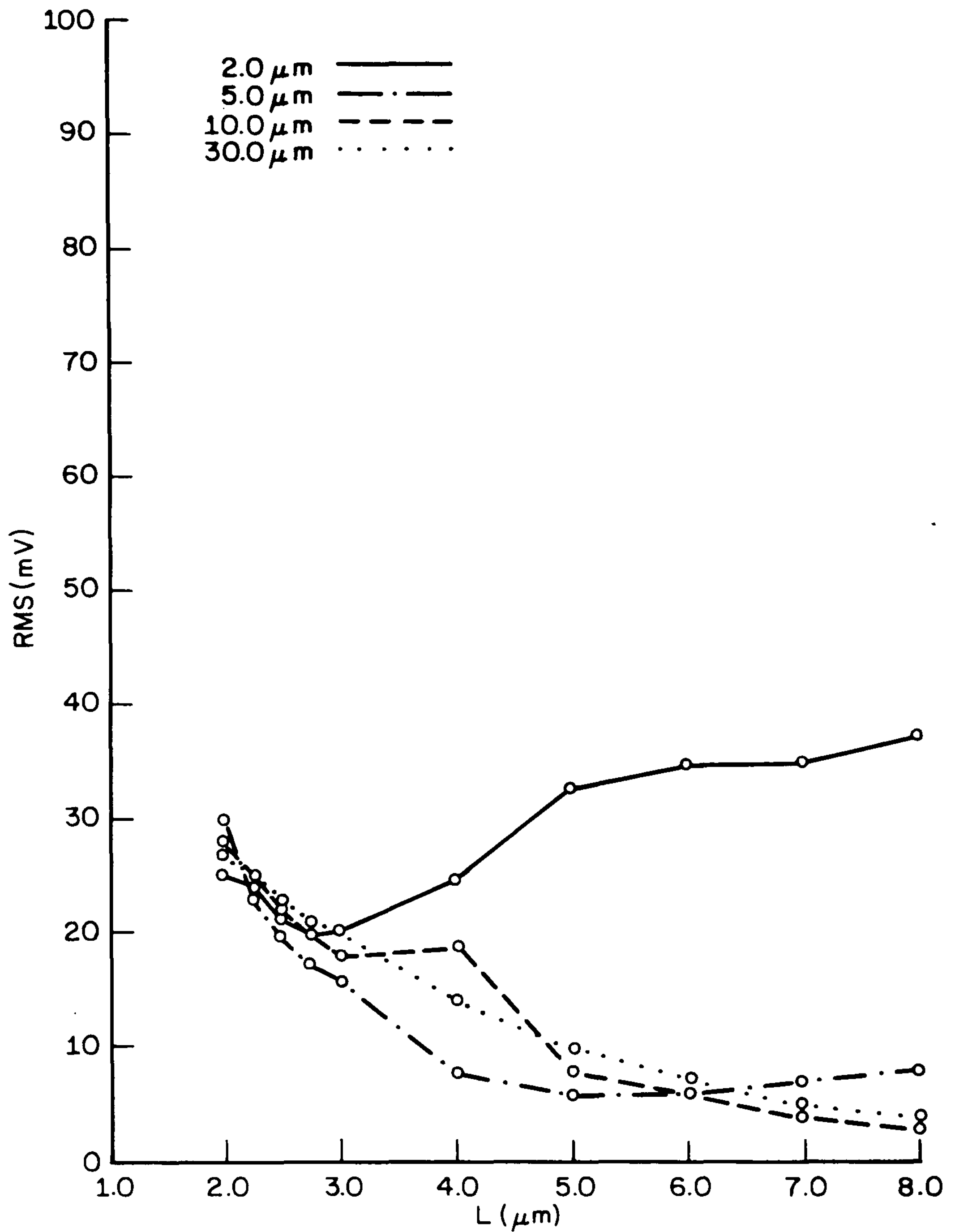


THE RMS DEVIATIONS VERSUS L FOR VARIOUS WIDTHS
FOR THE CFSIM MODEL
FIGURE 29



THE RMS DEVIATIONS VERSUS L FOR VARIOUS WIDTHS FOR TOYABE'S MODEL

FIGURE 30



THE RMS DEVIATIONS VERSUS L FOR VARIOUS WIDTHS FOR TROUTMAN'S MODEL
FIGURE 31

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Troutman, R. R. and Fortino, A. G., "Simple Model for Threshold Voltage in a Short-Channel IGFET." IEEE Transactions on Electron Devices, Vol. ED-24, No. 10 (October 1977): 1266-1268.

BIOGRAPHY

Janet C. Montgomery, daughter of Mr. and Mrs. Henry D. Cassard, Jr., was born November 19, 1955 in Baltimore, Md. She received a B.S. degree in physics from Muhlenberg College in 1978. In 1977 she received the Clifford R. Moyer Memorial Prize.

She joined Bell Laboratories in 1978 where she investigated the oxidation kinetics of Ni-Zn ferrites. Since 1979 she has been involved in device modeling and the design of the 256K dynamic RAM.