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A VIDEO DISPLAY - GRAPHICS TERMINAL FOR USE WITH AN S-100 BASED MICROCOMPUTER

by

Thomas L. Carpenter, III

A Thesis
Presented to the Graduate Committee
of Lehigh University
in Candidacy for the Degree of
Master of Science
in
Electrical Engineering

Lehigh University
1979

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This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

April 13, 1979
(date)

Professor in Charge

Chairman of Department

ACKNOWLEDGEMENTS

I wish to express my appreciation to Professor A. I. Larky who was the major advisor for this thesis.

I further wish to acknowledge the total support of my family during all phases of this project. My wife Carol, my daughter Becky, and my son Timothy, all relinquished a great deal of time so that I could devote my full attention to this thesis.

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ABSTRACT

This paper describes a Video Display/Graphics Terminal(VDGT)- a system for intermixing alphanumerics and dot graphics on a single TV monitor. The VDGT board plugs directly into an S-100 Bus Microcomputer and occupies 8K bytes of memory space divided into two separate memory sections - a 1K byte section for storing the alphanumeric characters and a 7K bytes section for storing a 256 X 224 dot matrix.

Custom devices are incorporated into the VDGT to provide the synchronization signals, to generate the DMA addresses, and to convert the data into characters for display. These devices also provide the VDGT with four modes of operation and such attributes as Underline, Reverse Video, Character Blank, etc. The four modes are the Alphanumeric mode, the Wide Graphic mode, the External Data (dot matrix) mode, and the Thin Graphics mode.

This thesis describes an augmentation of these modes, Mixed Mode, which is the major distinguishing feature between this system and other hobby systems. This Mixed Mode allows all of the modes and attributes

to be intermixed on a character-by-character basis. This Mixed Mode includes displaying all or any portion of the 256 X 224 dot matrix intermixed with the other modes.

The VDGT was constructed and interfaced to a SOL-20 microcomputer (which uses an Intel 8080 CPU and is organized around an S-100 bus). The detailed description of the system design and implementation is the basis for this thesis.

INTRODUCTION

The introduction of the ALTAIR 8800 microcomputer in Popular Electronics in 1975 [1,2], can be credited with creating the home computing market. This system, comprised of an Intel 8080 microprocessor; a front panel with toggle switches and light emitting diodes; a memory board with 256 bytes of read/write random access memory (RAM); a power supply; and a cabinet; offered an easily expandable computer system at a price, an order of magnitude, lower than commercial systems. It soon became apparent to many Altair owners that the human interface to such a powerful machine should consist of more than red lights and toggle switches; furthermore, input/output devices operating at Teletype speeds (10 characters per second) were not well matched to the CPU speed of 2 MHz. The DECWRITER terminal, with a speed of 30 characters per second, is neither fast enough nor inexpensive enough for the hobby market.

Another new device also emerging at this time was the Video-Keyboard Terminal (VKT). The VKT, which can accept input at rates up to 9600 baud and display its output on a Cathode Ray Tube (CRT), was adopted rapidly in the

minicomputer world by such manufacturers as Hewelett-Packard, Tektronix and Honeywell; but it too had the disadvantage of having a price comparable to that of the microcomputer itself.

Nevertheless, the VKT stirred many to consider what minimum circuitry was necessary to implement its functions [3]. The CRT was, in many cases, an ordinary TV monitor built into the same cabinet as the keyboard; with electronics to decode the keys and send the data to a local memory where it would be converted into the dot patterns needed to display the character. A video mixing circuit would combine the video synchronization information with the dot patterns and send the composite signal to the TV monitor.

It was not long before the microcomputer enthusiasts published designs showing how to implement the VKT with an ordinary home TV set used for the monitor. These designs usually placed the character memory in the processor's address space and eliminated the need to send the data to a separate device. This allowed writing characters on the TV screen as fast as the program could read them and store them into memory. A full screen of 1024 characters could be updated in only 6 milliseconds!

BYTE Magazine and others published articles [4,5]

showing the necessary circuitry needed to construct a TV Typewriter (VKT). Small companies started offering hardware to interface directly to the ALTAIR Bus (now known as the S-100 Bus) to generate the VKT functions internally to the microcomputer. One such company, Processor Technology, Inc., offered a Video Display Module (VDM-1), which provided all the necessary functions to display alphanumerics directly on a TV monitor. The character memory was a 1K RAM located on the VDM-1 board itself. The software that was provided with the VDM-1 took care of all the housekeeping needed to organize the memory into lines of text; to provide scrolling; and to enable reverse video.

As time passed, it became apparent that the power of this microcomputer, just as its bigger brother the minicomputer, was in its ability to manipulate and display data. The VDM-1 could be used to display only alphanumeric characters; tabular data; or, at best, a rather crude graph. Since the VDM-1 page format was 64 characters per row and 16 rows per page, only a 64 X 16 matrix could be utilized for graphics. This left a great deal of machine capability unutilized.

A dot plotter could be used to generate the output needed to display data in a graphic format. Dot matrix

plotters and line (vector) plotters are common throughout industry to produce just the kind of graphic representation of data that the microcomputer is capable of generating; however, as with a commercial VKT, the cost is prohibitive.

A study of the VDM-1 showed [6] that there was actually a very fine dot matrix being generated on the TV screen. The dot matrix that was required to display a single character was 9 dots wide by 13 dots high, and even though there were only 16 lines of 64 characters, the VDM-1 was generating a 576 X 208 dot matrix to display the 1024 characters per frame. Although these dots are not individually addressable in the VDM-1, it seemed possible to construct circuitry to create a display in which each dot (or pixel) would be individually controllable and stored in a single bit in memory; they would then be displayed as a dot matrix on the TV screen. Using the VDM-1 format, this would require the storing of 119,808 bits of information and take 14,976 bytes of memory. This is certainly feasible, but not absolutely required, since a dot matrix of 256 X 256 would give an acceptable resolution and would require only 8K of memory to store the entire image.

Even with all the capability of the VDM-1 and the added dot matrix, one additional capability seemed to be needed

- the ability to mix them together on a TV screen. While the 256 X 256 dot matrix gives good resolution to graphic representations of data, it is not well suited to the alphanumerics needed to dimension, title, or augment the graph. When a 256 dot line is divided to define characters, it produces only 32 characters per line as compared to the 64 characters that are generated by a character generator and its associated electronics. On the other hand, if the dot matrix information and the alphanumerics were generated separately and selectable on a character-by-character basis, a composite video picture could be constructed. This would allow full graphic capabilities and high density textual information to be displayed together.

This paper describes a Video Display/Graphics Terminal (VDGT) - a system for intermixing graphics and alphanumerics on a single video monitor. This system was implemented using custom LSI devices recently making their appearance on the consumer market and is presented as an example of a design using state-of-the art devices.

Chapter 1

Functional Description

The VDGT plugs directly into one slot of an S-100 bus microcomputer and occupies 8K bytes of the CPU memory space. Figure 1 shows the block diagram of the overall system. When the CPU is addressing the memory contained in the VDGT, a Board Select line goes active. This gives control of the address lines and the data lines to the CPU and corresponds to the normal operation of all microcomputer memory boards.

When the Board Select is not active, there is a DMA address that is gated onto the internal address lines. This activates a data read from the VDGT memory. The data that is read is sent to the character generator ROM to begin processing at the next Character Clock pulse. The processing is determined by one of the four modes selected in the character generator. The modes that are available process the data as either characters, wide graphics, thin graphics, or dot graphics.

The Character Clock, which loads the data, attributes, and mode information into the character ROM; also advances the DMA address generator to the next character address

and initiates another read cycle. This clock is generated from the fundamental dot clock frequency, and creates the character format timing required to generate the Retrace Blanking and the Composite Sync signals. These signals are then combined in the video mixer with the output of the character ROM to create the Composite Video signal needed to drive the TV monitor.

The 8K memory in the VDGT is actually divided into two sections (Figure 2). A 1K byte section is used to store the 1024 characters that define a page of text. Since the characters are stored in ASCII format, only 1K is needed to store the entire page; the remaining 7K of memory is used to store the dot matrix information. Both memory sections are read simultaneously, so that the data selected for processing will be available on a continuous basis at the data MUX.

The choice of the data for processing is controlled by the information held in the Mode Latch (a two bit latch loaded by an I/O instruction from the CPU). When the Alphanumerics mode or the Wide Graphics mode is selected, the data from the 1K section is sent to the character ROM. The data is then processed into either an alphanumeric character or a graphic character. When the Dot Graphics mode is selected, the data from the 7K section is shifted

through the character ROM without further processing, creating a serial image of the memory data.

The character ROM has attribute options which may be added to each character. These attributes include strike-through and underline for alphanumeric characters and reverse video for any mode selected. There is also a "Character Blank" input that will disable the output. These attributes are held in a latch and loaded with each character clock pulse along with the character data.

Chapter 2

Custom Devices

In implementing the design of a display system, it is necessary to generate all the synchronization signals needed to drive a standard TV monitor. There are devices available that will create the needed synchronization signals from a high frequency clock; some of these devices are classified as CRT controllers. One such device is the CRT 5027 manufactured by Standard Microsystems Corporation (SMC).

The CRT 5027 is a completely software programmable CRT controller containing the logic required to generate all the timing signals for the presentation of video data on a TV monitor when clocked at the desired character rate (see Table 1). All character formats, synchronization information, and character matrix information may be programmed into the CRT 5027 on initialization via seven registers within the device. These registers store the information for horizontal sync, vertical sync, characters per row, rows per frame, raster scans per row, and raster scans per frame. Figure 3 shows the resulting VDGT screen format. In addition to these seven registers, two other registers

are provided in the CRT 5027 to store the cursor position (the position of the last character entered). These two registers can be read and updated by the CPU as desired.

After the CRT 5027 is programmed and a start sequence is initiated, it generates, without further intervention from the CPU, all the DMA address signals needed to sequentially read the memory and present the data to a character generator. The display system requires a crystal oscillator and a dot counter to drive and synchronize the timing.

The dot counter is used to divide the dot clock by a divisor (N) which is set for the total horizontal dots in a character. Therefore, the carry out of the dot counter pulses once per character (creating the Character Clock) and is fed to the CRT 5027 to signal the start of a new character period. This enables the CRT 5027 to keep track of the character positions and generate the entire video timing chain. Detailed timing for the VDGT is discussed in Chapter 7.

The companion device to the CRT 5027 is the CRT 8002 Video Display-Controller Video Generator also made by SMC (see Table 2). The CRT 8002 is a custom character generator ROM that contains an internal shift register and is capable of operating in the four modes previously

discussed. These modes are the Character mode, the External Data mode, the Wide Graphics mode, and the Thin Graphics mode.

The Character mode addresses the internal ROM that contains the information to generate 128 different ASCII characters (see Figure 4). The External mode accepts the 8 bit data as the dot information and presents it to the output shift register without further processing. Tne Wide Graphics mode produces an eight part graphic character that occupies the same space as an ASCII character. This provides a selection of 256 unique graphic characters (See Figure 5). The fourth mode, Thin Graphics, also implements graphics in the same space as an ASCII character. It defines lines within the character space wnich are intended to be used to draw wire figures. (See Figure 6).

The combination of the CRT 8002 Character Generator and the CRT 5027 Controller, provides all the timing and character generating circuitry required for the display portion of a CRT video terminal system.

Chapter 3

The Mode and Attribute Control

The mode of operation of the VDGT is controlled by an externally-set Mode Latch. This latch is 2 bits wide and selects one of the four modes of operation - Alphanumeric, Wide Graphics, External Data (dot matrix), or Thin Graphics. This latch controls the display format as follows:

Bit 1 MS1	Bit 0 MS0	
1	1	ALPHANUMERIC (MIXED) MODE
0	1	EXTERNAL (DOT MATRIX)
1	0	THIN GRAPHICS
0	0	WIDE GRAPHICS

In the Alphanumeric Mode, the data (from the 1K memory section) is converted into alphanumeric characters and displayed. Since these characters are stored in ASCII format and require only 7 bits, the eighth bit is used to create a new mode of operation. This new mode, called Mixed Mode, uses bit 8 to override the Mode Latch data. It is important to note that the override can only take place if the Mode Latch is set for the Alphanumeric mode.

In this Mixed Mode, it is possible to intermix all

modes on a character-by-character basis. A "Character Blank" signal is sent to the CRT 8002 whenever this 8th bit is set and inhibits having extraneous data displayed during a mode or attribute change. The format of the 1K section used for control of the modes and attributes is as follows:

Data Bit Number

bit 8 : Enable latches (Mixed Mode Only)
bit 7 : Mode bit 1 (MS1)
bit 6 : Mode bit 0 (MS0)
bit 5 : Select reverse video
bit 4 : Select strike-through
bit 3 : Select underline
bit 2 : Blank remainder of line
bit 1 : Blank remainder of frame

Figure 7 shows the circuitry that has been added to that normally associated with the CRT 5027 and the CRT 8002 to create the Mixed Mode of operation. This Mixed Mode of operation is the major distinguishing factor between this system and previously described alphanumeric and/or graphics display systems.

Some examples of the sorts of special effects that can be obtained are:

1. Windowing (Viewing graphics through an area open in the alphanumerics)

2. Scrolling Windows
3. Titling with Wide Graphics characters
4. Reverse video character areas around graphics
5. Graphics (dot) characters added to text

Figures 8, 9, and 10 show examples of full alphanumerics, full graphics, and Mixed Mode, respectively. The Mixed Mode figure is shown with Wide Graphics characters at the top and Alphanumeric characters defining a window revealing a Dot Graphics area. There is also underlining and strike-through shown in both straight and reverse video.

Chapter 4

The Character Formats

The horizontal display is divided into 64 eight-bit bytes, which produces a horizontal count of 512 pixels per sweep, and is selected to insure a match with the 256 dot matrix (graphics) that will be generated (each graphic dot occupies two pixel positions). The CRT 8002 generates its alphanumeric characters in a 7 X 11 pixel matrix. The characters are displayed in a 8 X 12 matrix; this leaves one pixel between characters.

The number of horizontal sweeps used to define the character matrix is selectable from a minimum of 12 to a maximum of 16 sweeps. For the purpose of compatibility with the dot graphics, either 12 or 14 should be selected. The wider vertical spacing (14 sweeps per character) gives a very pleasing line spacing to the alphanumerics on a 9 inch monitor - especially when the underline attribute (reverse video on sweep line R11) is selected. This also produces 224 scans per frame which exactly overlays the area produced by the dot graphics stored in the 7K memory (7168 bytes).

When the 12 sweep format is selected, less vertical

spacing is generated between character rows. This has an advantage when selecting the Wide Graphics mode by eliminating false underlining (see Figure 5, "14 RASTER FORMAT"). All pixels outside the 8 X 13 Wide Graphics matrix are always in the reverse video state. This creates a false underlining effect when more than 13 sweeps per character are used. Therefore, an 8 X 12 character matrix is recommended when using the Wide Graphics option. This establishes the active display area of the screen at 192 lines; rather than the 224 lines computed above. This reduction is a reasonable trade-off, however, when the advantage of being able to mix all of the modes together on a single screen is considered.

In some applications, Wide Graphics may not need to be intermixed with the other modes. These applications are better met with 14 sweeps per character space. This restores the 256 X 224 dot matrix capability of the graphics display.

Chapter 5

The Address Bus

The CPU and the DMA circuitry have independent access to memory through four 2-to-1 multiplexers. Figure 11 shows the block diagram of the internal address bus. A board enable signal is generated whenever the CPU is addressing the memory, giving foreground control to the CPU. When the board enable signal is not active, the multiplexers are returned to the standard position of selecting the DMA address for memory reading. Although the DMA circuitry only has background control, the memory contents appear to be constantly displayed under normal operation.

Scrolling is accomplished by changing the starting address for a frame scan. The starting address for a scan is held in an internal register in the CRT 5027 which can be loaded by an I/O instruction from the processor. Changing this register starts the frame scan at a new memory position. Thus, the screen can be scrolled up as in a conventional typewriter.

This feature of scrolling lines is not desirable, however, for graphics. It is not very useful to shift an entire picture in an attempt to simulate motion, and even

if this were useful, the scrolling address shifts in character row units (12 or 14 horizontal sweeps) and not by single sweeps that would be required to generate smooth motion. Therefore, the graphics address bus in the VDGT remains fixed with respect to the vertical frame.

To keep the graphics fixed and in sync with the character display, the graphics DMA address is generated by following the least significant bit of the alphanumeric address bus. The lower half of the graphics address is generated directly by the character position counter and the least significant, R0, bit of the character row counter in the CRT 5027. Row counter bit R0 is fed also to a separate binary counter which increments one count every horizontal sweep. This produces the higher order bits needed to address the entire 7K memory section and read the dot matrix data. The binary counter is initialized at every vertical sync pulse to point to the first word of the graphics memory. This fixes the graphic representation on the screen independent of the scrolling.

Chapter 6

The Data Bus

The data bus, like the address bus, is split into sections. This permits read/write control by the CPU when desired and allows the DMA circuitry to read both sections of the memory simultaneously for video display. Figure 12 is the block diagram of the data bus system.

For CPU writes, the read/write control logic (R/W CONT) enables the data-in buffer and presents the CPU data to both the memory sections. Address decoding selects the appropriate memory section. The data buffer also drives the data-in lines when the CPU is loading registers in the CRT 5027.

For CPU reads, data may come from either memory section. A multiplexer (MUX) controlled by board enable ANDed with other control signals (SINP, SOUT, PDBIN, A12, and A11), selects the proper data path and drives the CPU data-in bus.

When the CPU reads internal registers of the CRT 5027, another data buffer is enabled. This buffer, as well as the data MUX, has tri-state outputs and will drive the data-in bus when signaled by the R/W CONT logic.

When the CPU is not addressing the VDGT, the internal data bus presents data to the CRT 8002 for display. The MODE DATA LATCH selects the memory section that is to be displayed as directed by the mode select logic.

The data bus is also used to expand the graphics dot to two pixels per dot. This is accomplished by presenting the 7K data to a 2-to-1 MUX. This MUX has 16 input lines and 8 output lines. One 7K data bit is wired to two input lines so that only 4 bits are needed to drive the outputs during a character time. The MUX is controlled by the least significant bit of the CRT 5027 character position counter (H0). This selects the bottom half of a data byte during one character time and then the other half of the same data byte the next character time. This produces 256 dots of graphics data in the same space as the 512 pixels of alphanumeric information.

The graphics data is read at half speed to maintain sync with the alphanumeric data. The DMA address that reads the 7K memory section is shifted one position to the left with respect to the 1K memory section. This produces 32 read cycles for each horizontal sweep of the display instead of the 64 read cycles required for the display of a single row of alphanumeric characters.

Chapter 7

Clocks and Character Timing

The dot clock frequency is determined from the characters per row, the RS-170 requirements, and the dots required to produce a character. The standard video signals require that each horizontal sweep be 63.5 microseconds long with 262 sweeps per vertical frame. Since 512 dots are required for the 64 characters on a line and the total horizontal retrace time is 12.5 microseconds, this leaves 51 ns for the 512 pixels. This computes to just over 10 MHz for the dot clock. Since the amount of overscan on any particular monitor is somewhat unpredictable, a slightly higher dot frequency was used to make a shorter display line and give more latitude to the retrace control. Also, the dot matrix has been selected to give the programmer an aspect ratio as near as possible to 1:1 for symmetry in graphic representations and a clock frequency that would maintain this ratio is desirable. A 12.906 MHz crystal yielded a 1:1.05 aspect ratio on a SANYO 4209 TV monitor.

The dot clock is divided by eight to produces the Character Rate clock; a short, truncated pulse of less than a

full dot width. This less than full width pulse is sent to the CRT 8002 as a character latch pulse to load the next datum.

The dot clock is also decoded into Count One and Count Seven. Figure 13 shows the timing diagram produced by this decoding. On Count One, a pulse is sent to the CRT 5027 indicating that the previous data is latched and that the DMA address counter can be incremented to the next count. Count Seven is ANDed with the alphanumeric bit 8 and is used in Mixed Mode to latch the temporary mode information and the character attributes.

Chapter 8

Special Attributes and Other Funnies

When Mixed Mode is selected, the attributes that are available include Line Blank and Frame Blank. These are special attributes augmenting the Character Blank capability in the CRT 8002. Setting bit 8 AND bit 2 in a 1K memory location loads the Attribute Latch and selects the Line Blank attribute. When this character is encountered, the Character Blank line is held high until cleared by Horizontal Sync; thus the remainder of the line is blanked.

A Frame Blank is created in a similar manner - if bit 6 AND bit 1 are set in a byte in the 1K memory, Character Blank remains high until cleared by Vertical Sync; thus blanking the remainder of the screen.

Both of these added attributes, like all the CRT 8002 attributes, may be turned off by a subsequent character. Any character that has bit 8 set and does not set the blanking bits, will terminate the blanking. This allows any part of a line or any part of a frame to be blanked. Similarly, any part of a line may be put in reverse video, have an underline added to it, or use the strike through

attribute.

The temporary mode selections operate in the same manner as the attribute selections. During Mixed Mode, whenever bit 8 is set in a 1K data word, bit 6 and bit 7 are interpreted and select a temporary mode. This temporary mode remains in effect until another data word is encountered with bit 8 set or until Horizontal Sync. This means that all or any part of a line may be placed in any mode - with one exception. The exception to multiple modes on a single line is Wide Graphics. This mode uses bit 8 to generate a section of the graphics character; therefore, bit 8 is not available for mode selection after Wide Graphics is enabled. Once invoked, Wide Graphics can not be cleared until Horizontal Sync, which clears all temporary modes. Wide Graphics may start at any character location, but must remain until the end of the line.

CONCLUSIONS

The VDGT was built and interfaced to a SOL-20 system and has proven to be very effective as both a Video Terminal and as a Graphics Display system. The alphanumeric portion has all the usual features associated with a Video Terminal. The Graphics Display portion, with its 256 X 224 dot resolution, is useful for line drawings and special effects not available on most microcomputer terminals.

The ability to intermix alphanumerics and graphics on a single screen, and even within a single line, gives the user a capability not found in other hobby display systems, and, with a total cost of about $350, this system is well within the reach of the home computer user.

TABLE 1

The CRT 5027 has the following capabilities:

A. Fully programmable Display Format
   1. 1-200 characters per row
   2. 1-64 row per frame
   3. 1-16 raster scans per row

B. Programmable monitor synchronization format
   1. 256-1023 scans per frame
   2. Programmable vertical and horizontal "Front Porch"
   3. Programmable horizontal synchronization width
   4. Programmable vertical and horizontal "Back Porch"
   5. Selectable interlaced or non-interlaced format
   6. Horizontal and vertical blanking

C. Multiple outputs
   1. Horizontal synchronization
   2. Vertical synchronization
   3. Composite synchronization
   4. Composite blanking
   5. Cursor position coincidence

D. Three programming positions
   1. CPU data bus
   2. Self-reading external ROM
   3. Mask option internal ROM

E. Compatible with different Monitors
   1. Standard RS-170 Monitors
   2. Non-Standard Monitors
      up to the Specifications under B above

F. Externally Controlled Scrolling of Data rows
   1. Single line
   2. Multiple Lines

G. Cursor Registers
   1. Read/Write Cursor Character Position
   2. Read/Write Cursor Line

H. Programmable Character Formats
   1. Compatible with 5x7 character ROMS
   2. Compatible with 7x9 character ROMS
   3. Character format only limited by specifications of A

I. All inputs/outputs are TTL compatible

J. Bus oriented
   1. Tri-stated 8-bit read/write register bus

K. High speed operation
   1. Typical character rate up to 4MHz

L. Companion device to CRT 8002 Character Generator

TABLE 2

The CRT 8002 has the following capabilities:

A. On chip character generator
   1. 128 Alpha-numeric characters
   2. 256 Graphic characters
   3. 7x11 Dot matrix character block (minimum)

B. On chip video shift register
   1. Access time is 400ns
   2. Shift frequency
      a) CRT 8002A 20MHz
      b) CRT 8002B 15MHz
      c) CRT 8002C 10MHz

C. On chip retrace blanking control

D. Four modes of operation
   1. Internal characters (ROM)
   2. Wide graphics (8 blocks per character)
   3. Thin graphics (3 lines per character)
   4. External inputs (dot graphics)

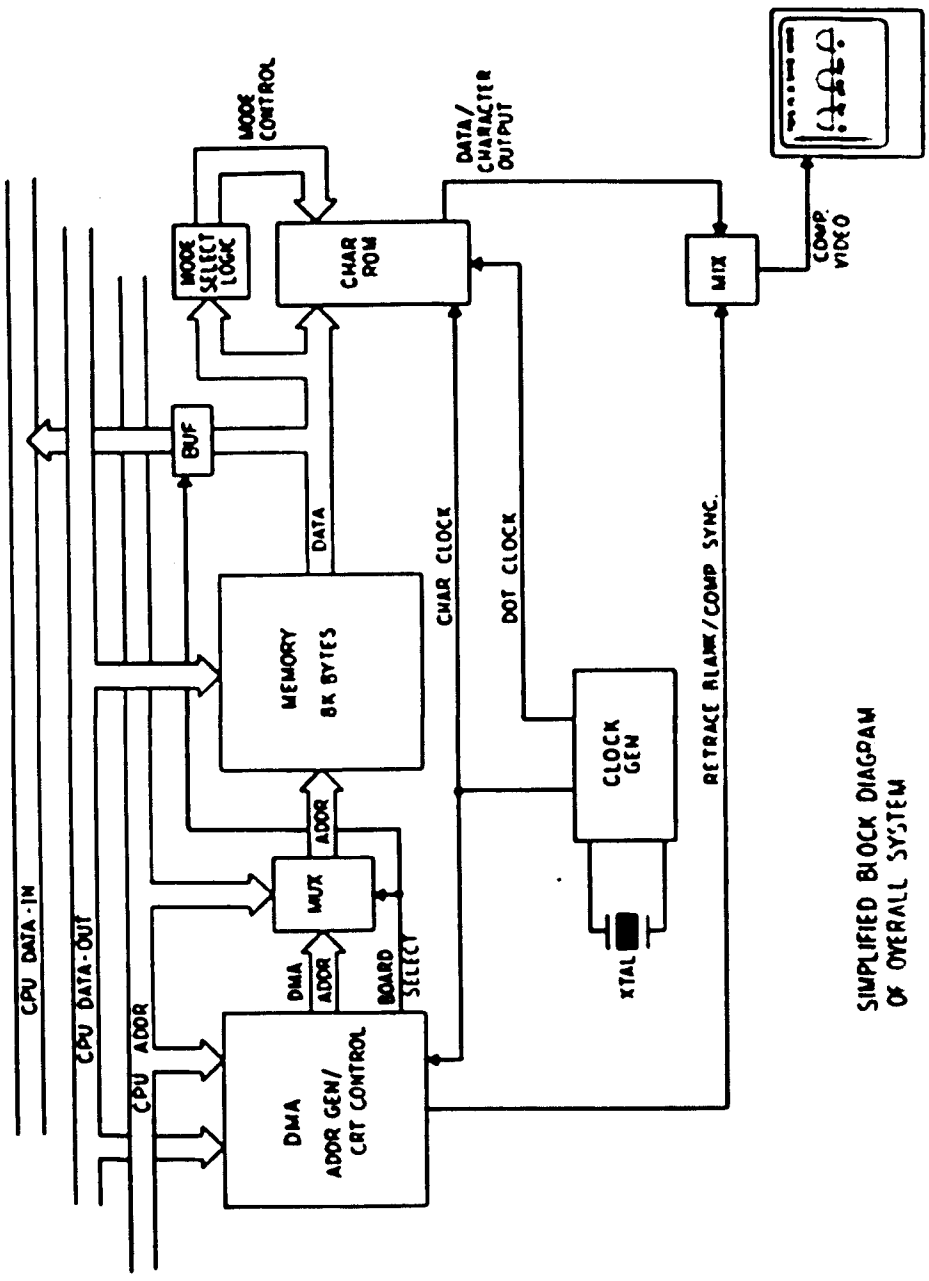
E. On chip attribute logic
   1. Reverse video
   2. Character blink
   3. Character underline
   4. Character strike-thru
   5. Character blank

F. Four on chip cursor modes
   1. Underline
   2. Blinking underline
   3. Reverse video
   4. Blinking reverse video

G. On chip address buffer/latch

H. On chip attribute buffer/latch

I. Other mask programmable options
   1. Blink rates
   2. Cursor types
   3. Character fonts



SIMPLIFIED BLOCK DIAGRAM OF OVERALL SYSTEM

Figure 1

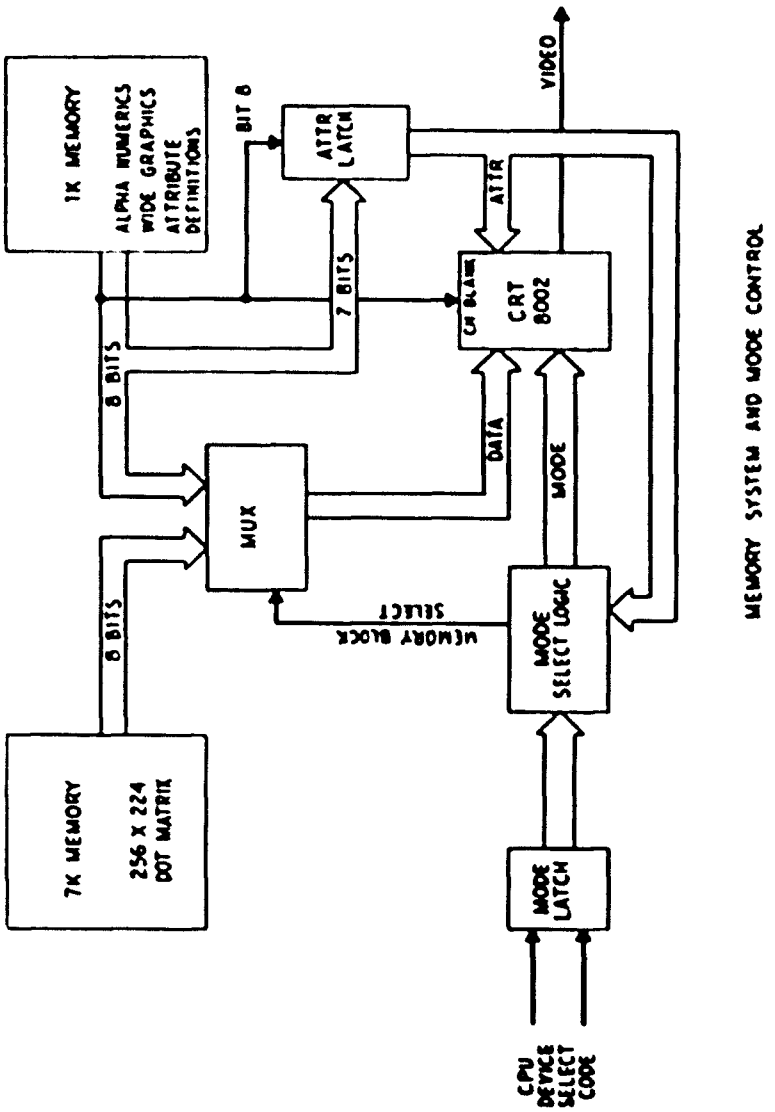
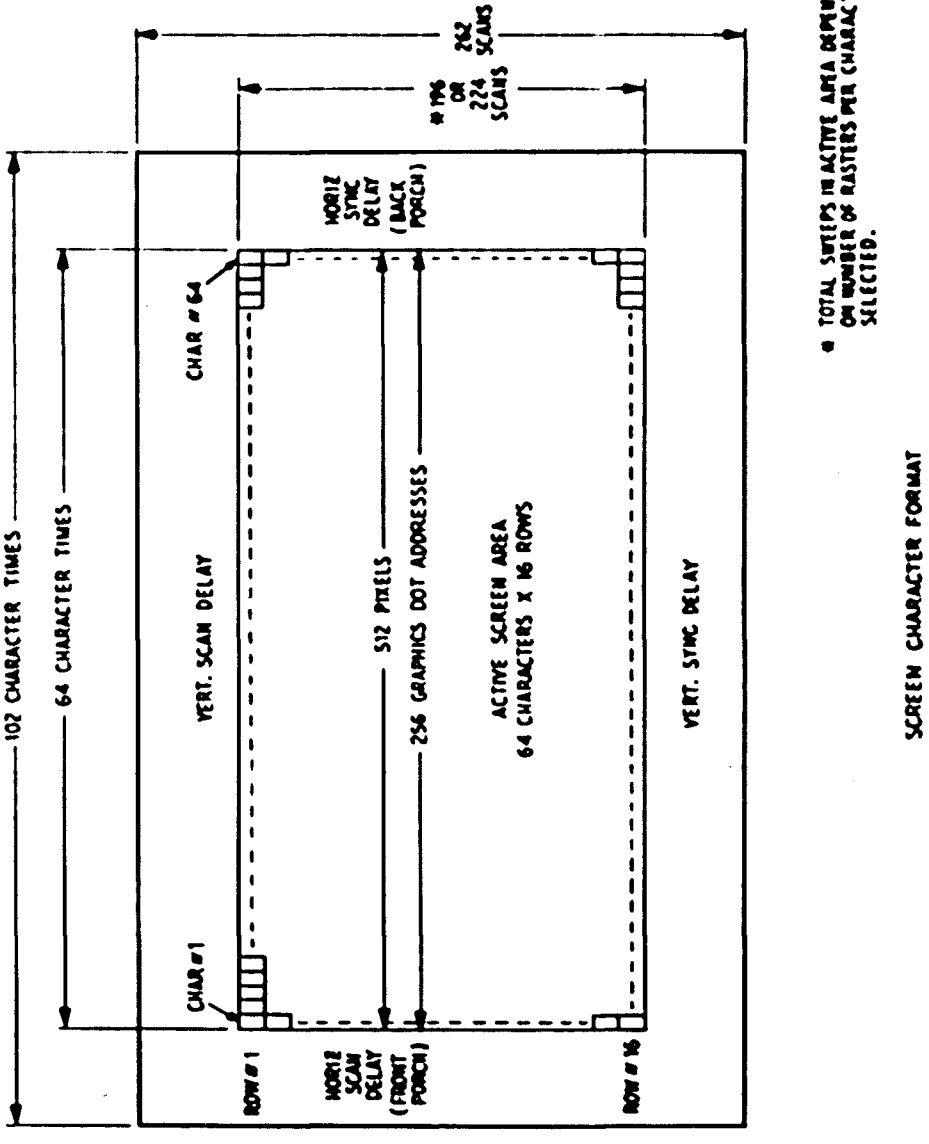
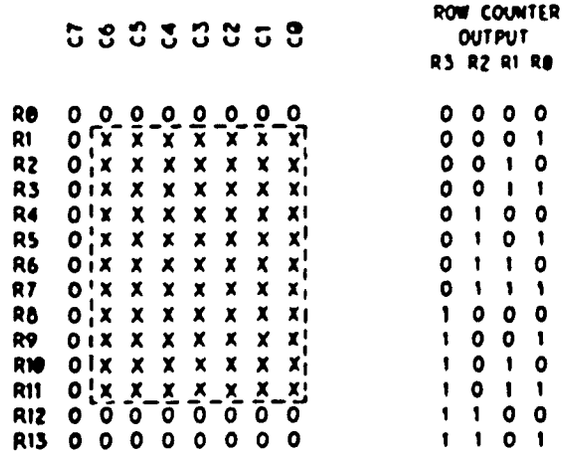

1K MEMORY
ALPHA NUMERICS
WIDE GRAPHICS
ATTRIBUTE
DEFINITIONS
BIT 6
ATTR LATCH
VIDEO
ATTR
7 BITS
CRT 8002
8 BITS
DATA
MUX
MODE
MEMORY BLOCK SELECT
MODE SELECT LOGIC
8 BITS
7K MEMORY
256 X 224
DOT MATRIX
MODE LATCH
CPU DEVICE SELECT CODE
MEMORY SYSTEM AND MODE CONTROL

Figure 2



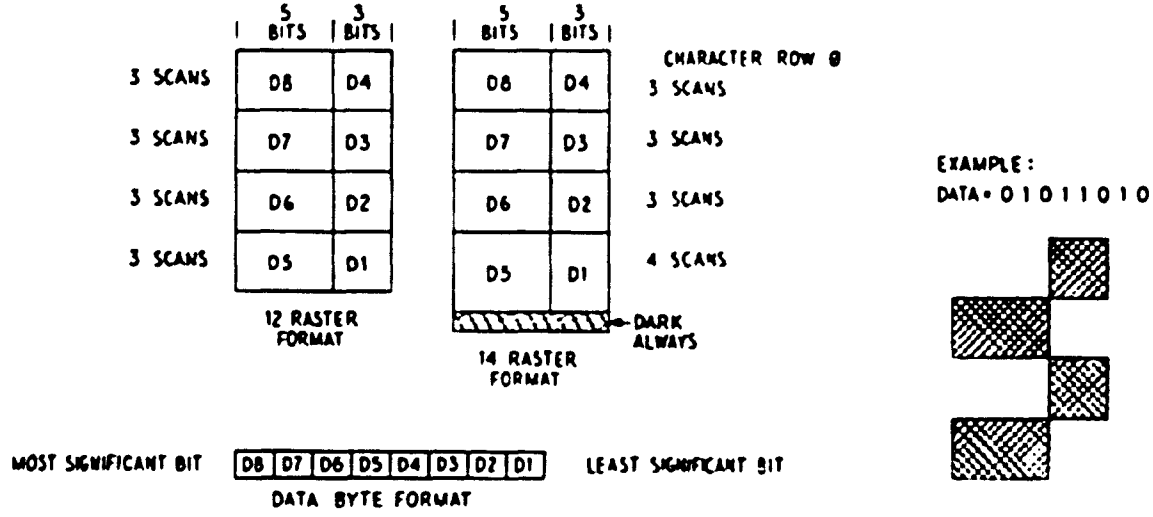
SCREEN CHARACTER FORMAT

Figure 3



ROW CHARACTER BLOCK FORMAT

Figure 4



WIDE GRAPHICS MODE
IN THE CRT 8002
(MS1:1 MS0=0)

Figure 5

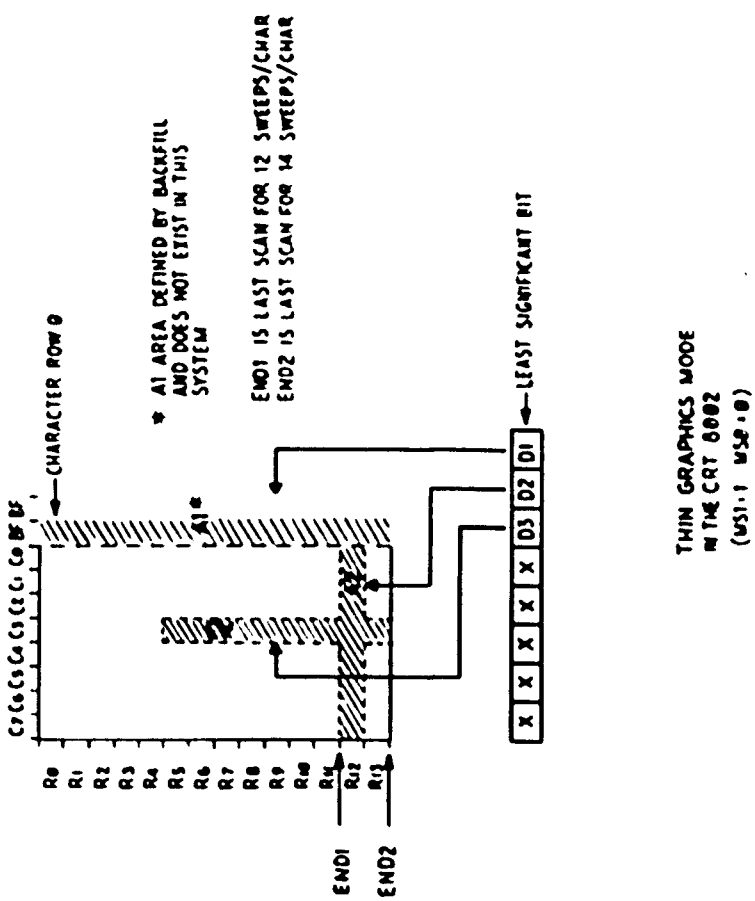
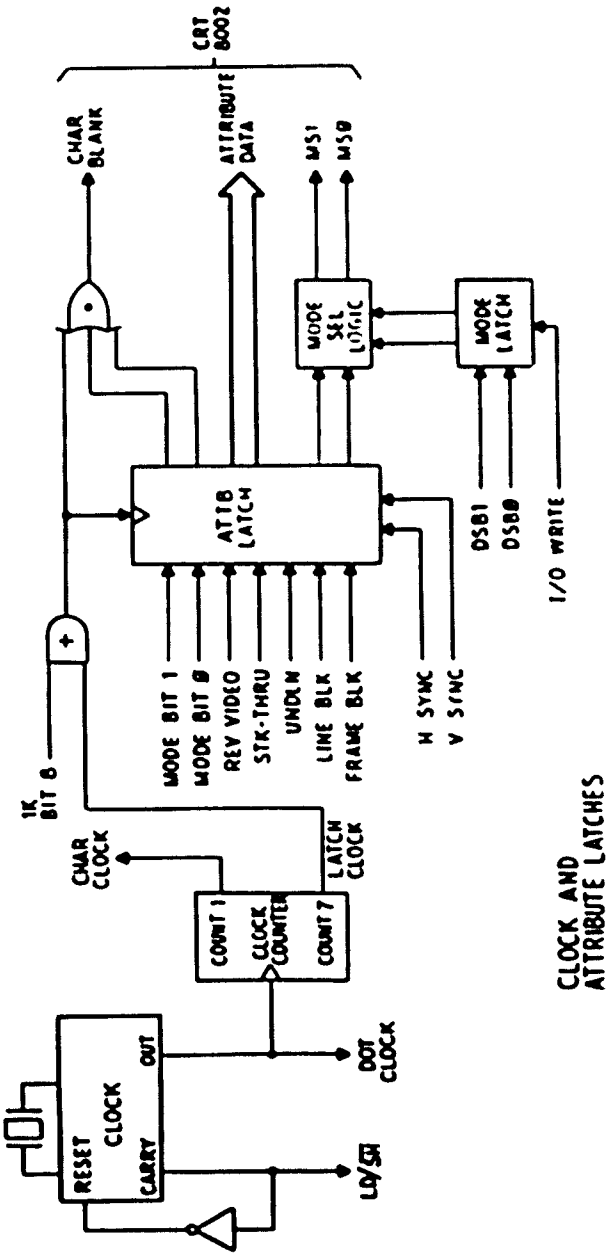

CHARACTER ROW 0
* A1 AREA DEFINED BY BACKFILL AND DOES NOT EXIST IN THIS SYSTEM
END1 IS LAST SCAN FOR 12 SWEEPS/CHAR
END2 IS LAST SCAN FOR 14 SWEEPS/CHAR
LEAST SIGNIFICANT BIT
X X X X D3 D2 D1
R0 R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13
END1
END2
THIN GRAPHICS MODE
IN THE CRT 8002

Figure 6



CLOCK AND ATTRIBUTE LATCHES

Figure 7

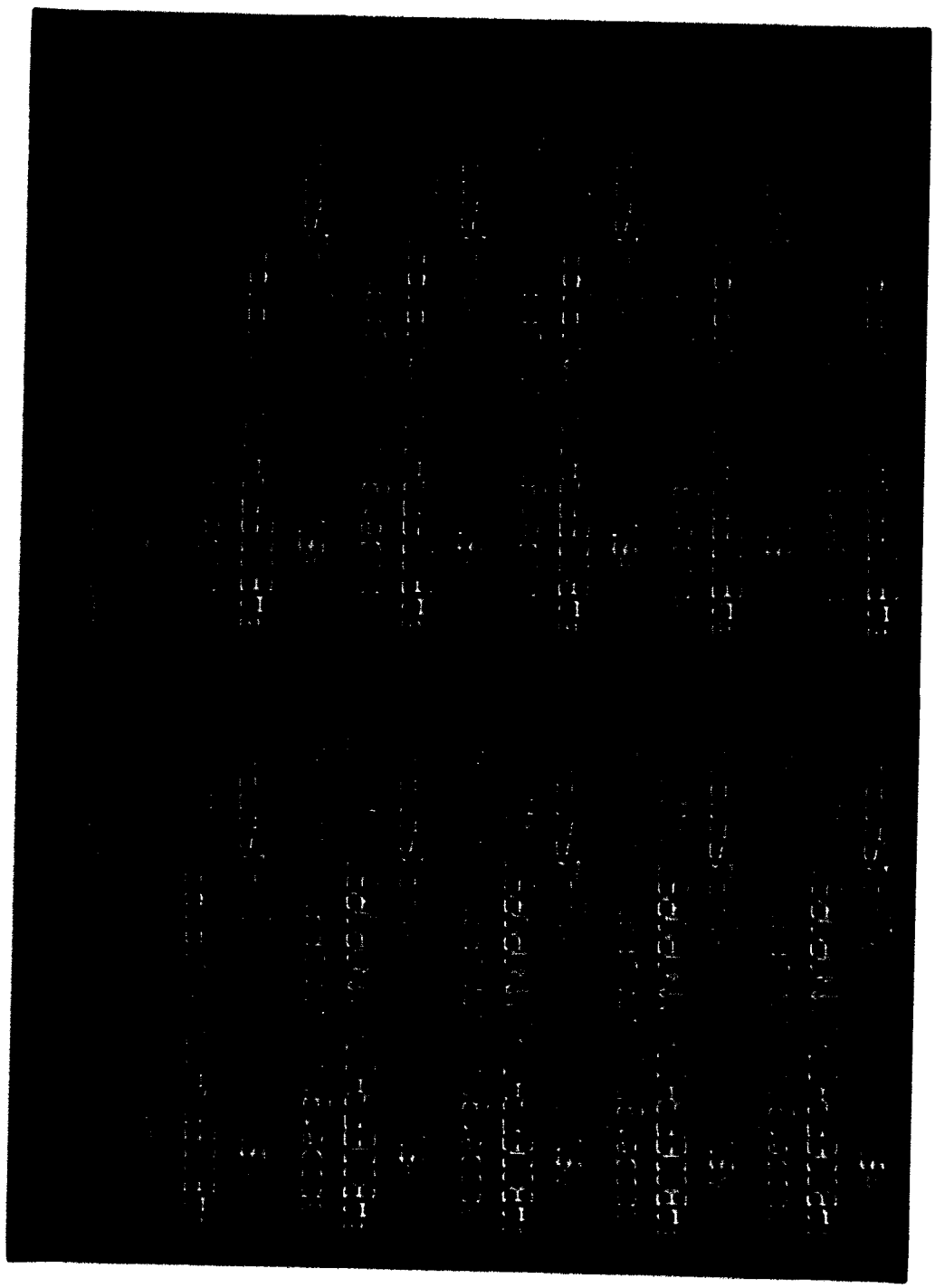


Figure 8

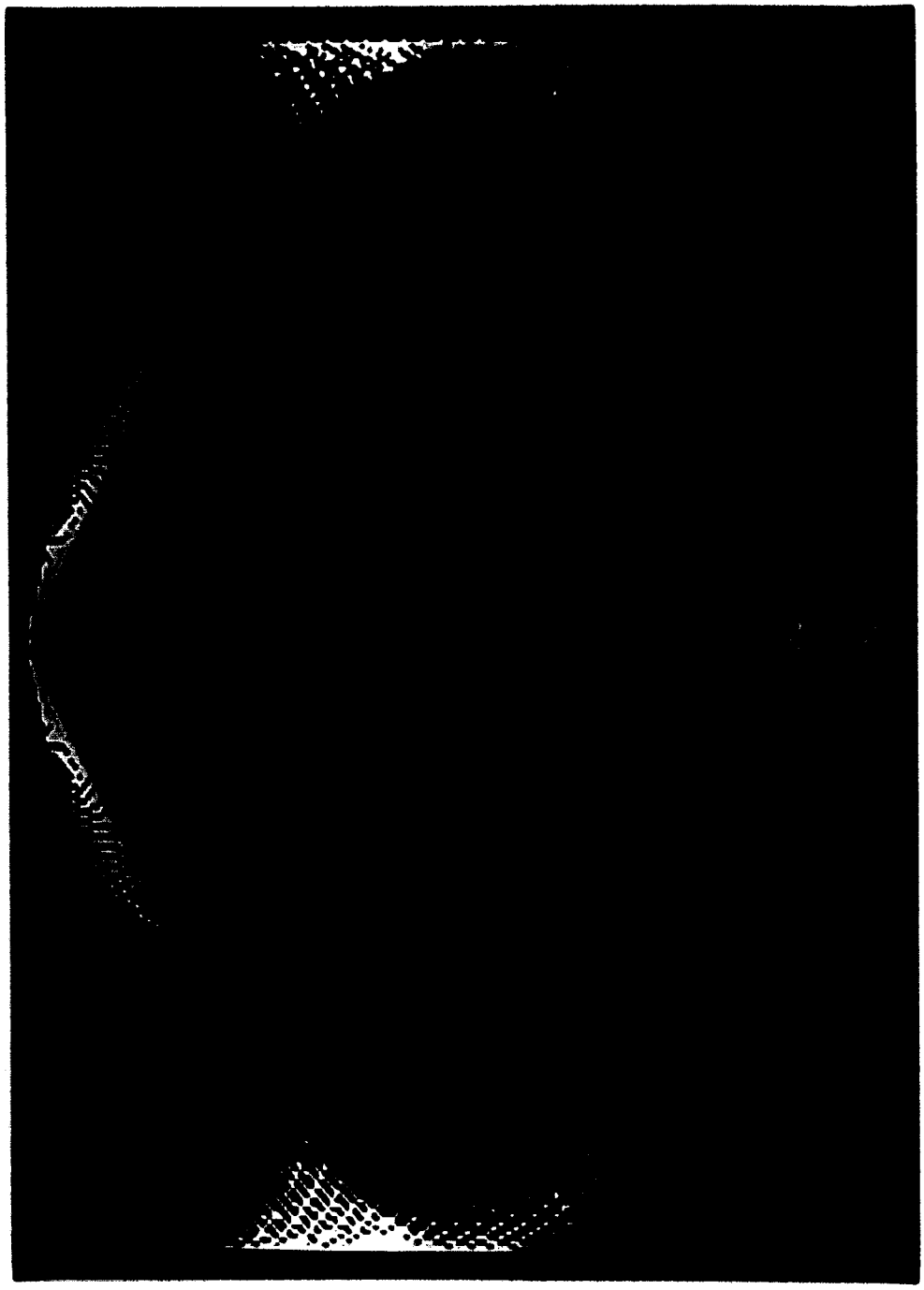


Figure 9

Figure 10

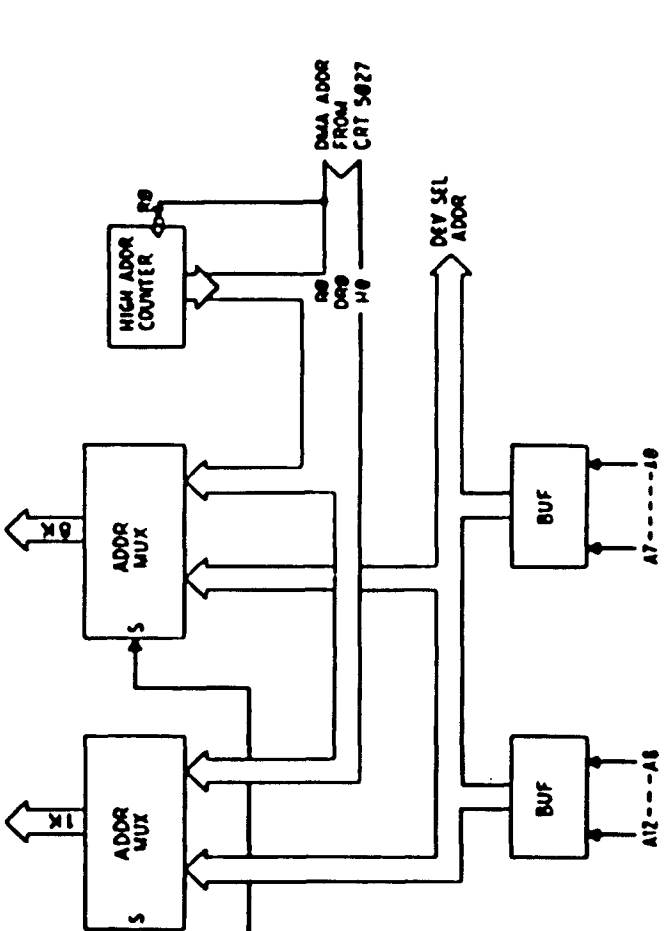

DMA ADDR FROM CAT 5027
HIGH ADDR COUNTER
DEV SEL ADDR
ADDR MUX
ADDR MUX
BUF
BUF
BOARD SELECT
A15 A14 A13 SHIP SORT

Figure 11

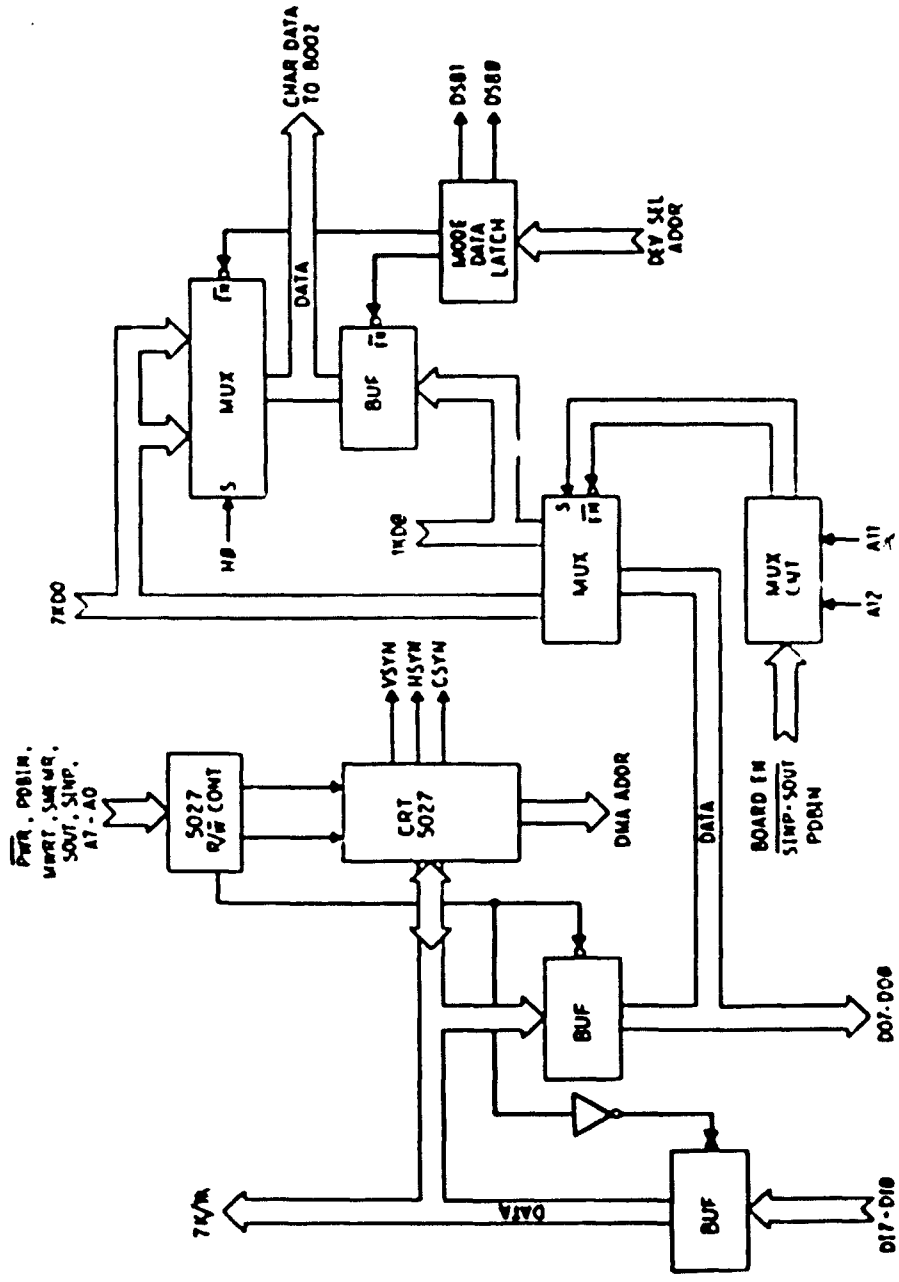
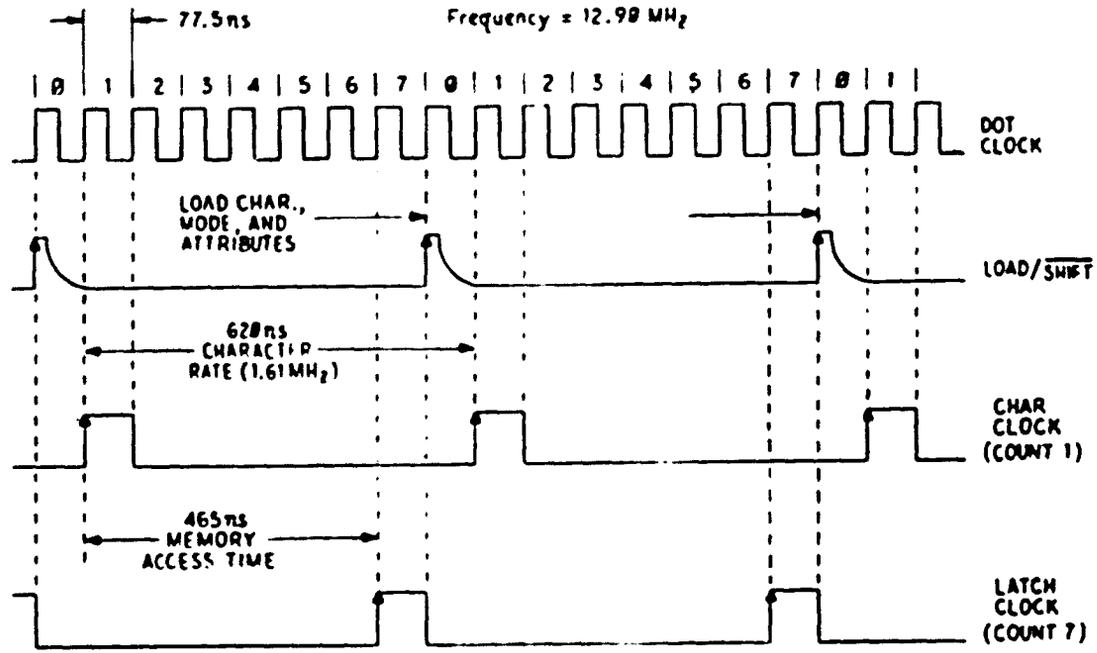

CHAR DATA TO 8002
DS81
DS80
MODE DATA LATCH
KEY SEL ADDR
DATA
MUX
BUF
MB
7KDO
MUX
MUX CNT
A11
A12
VSYN
HSYN
CSYN
5027 R/W CONT
CRT 5027
DMA ADDR
BOARD EN
SIMP-SOUT
PDBIN
DATA
BUF
D07-D00
BUF
D17-D10

Figure 12



TIMING DIAGRAM

Figure 13

SH. 16

REFERENCES

[1] Roberts, H. E., and Yates, W. "ALTAIR 8800 Minicomputer, Part 1" Popular Electronics, Vol. 7, No. 1, January 1975, pps. 33-38.

[2] Roberts, H. E., and Yates, W. "Build the ALTAIR 8800 Minicomputer, Part 2" Popular Electronics, Vol. 7, No. 2, February 1975, pps. 56-58.

[3] Lancaster, D., TV TYPEWRITER COOKBOOK, H. W. Sams & Co., Inc., New York, First Edition, 1976.

[4] Suding, R., "Build a TV Readout Device for Your Microprocessor", BYTE Magazine, Issue 12, Aug 1976, pgs. 66-73.

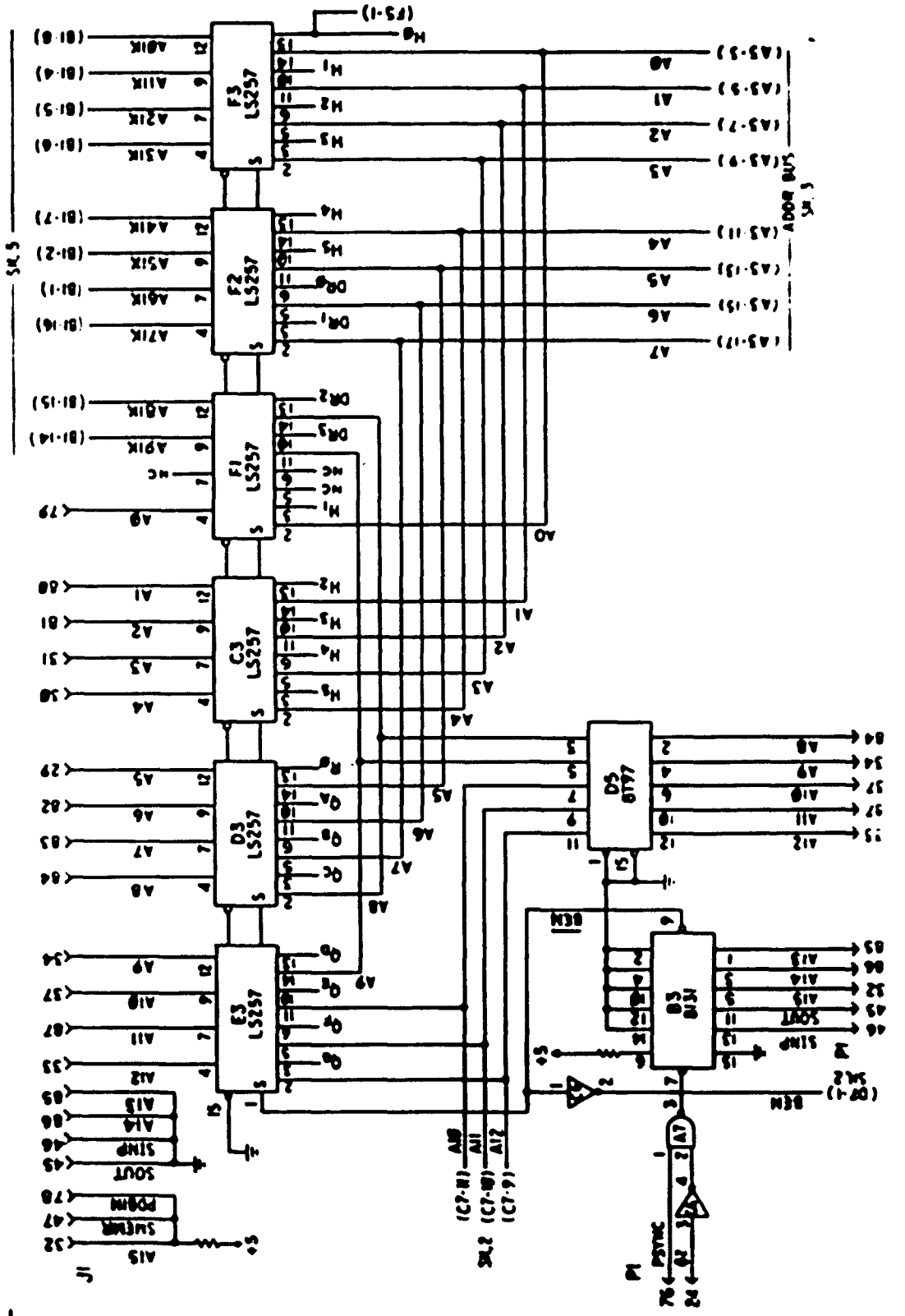
[5] Gantt, C. W., "Build a Television Display", BYTE Magazine, Issue 10, June 1976, pgs. 16-21.

[6] Processor Technology, Emeryville, CA. VDM-1 VIDEO DISPLAY MODULE ASSEMBLY and TEST INSTRUCTIONS, Supplied with VDM-1 Video Interface Kit, purchased June 1976.

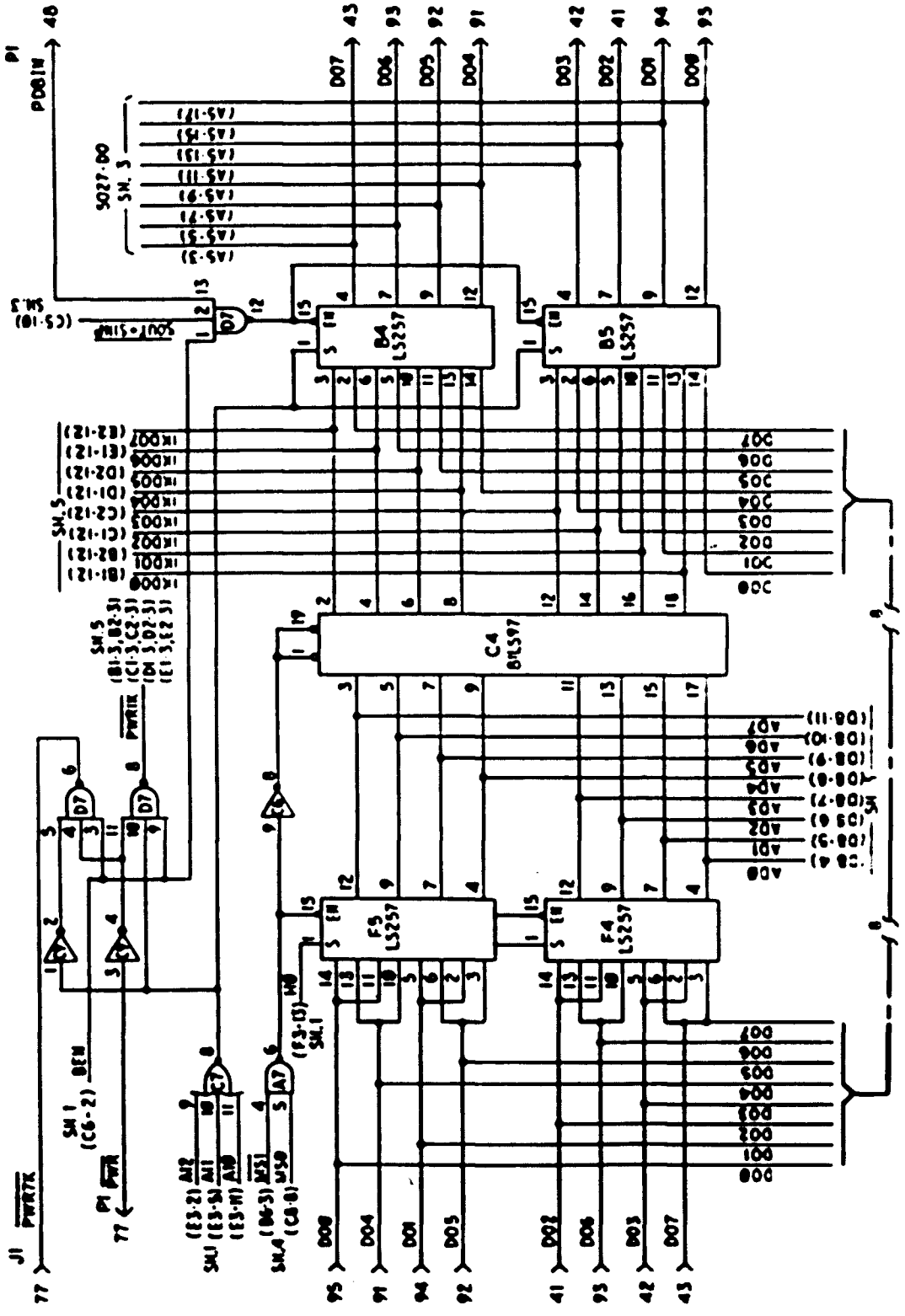
APPENDIX

SYSTEM

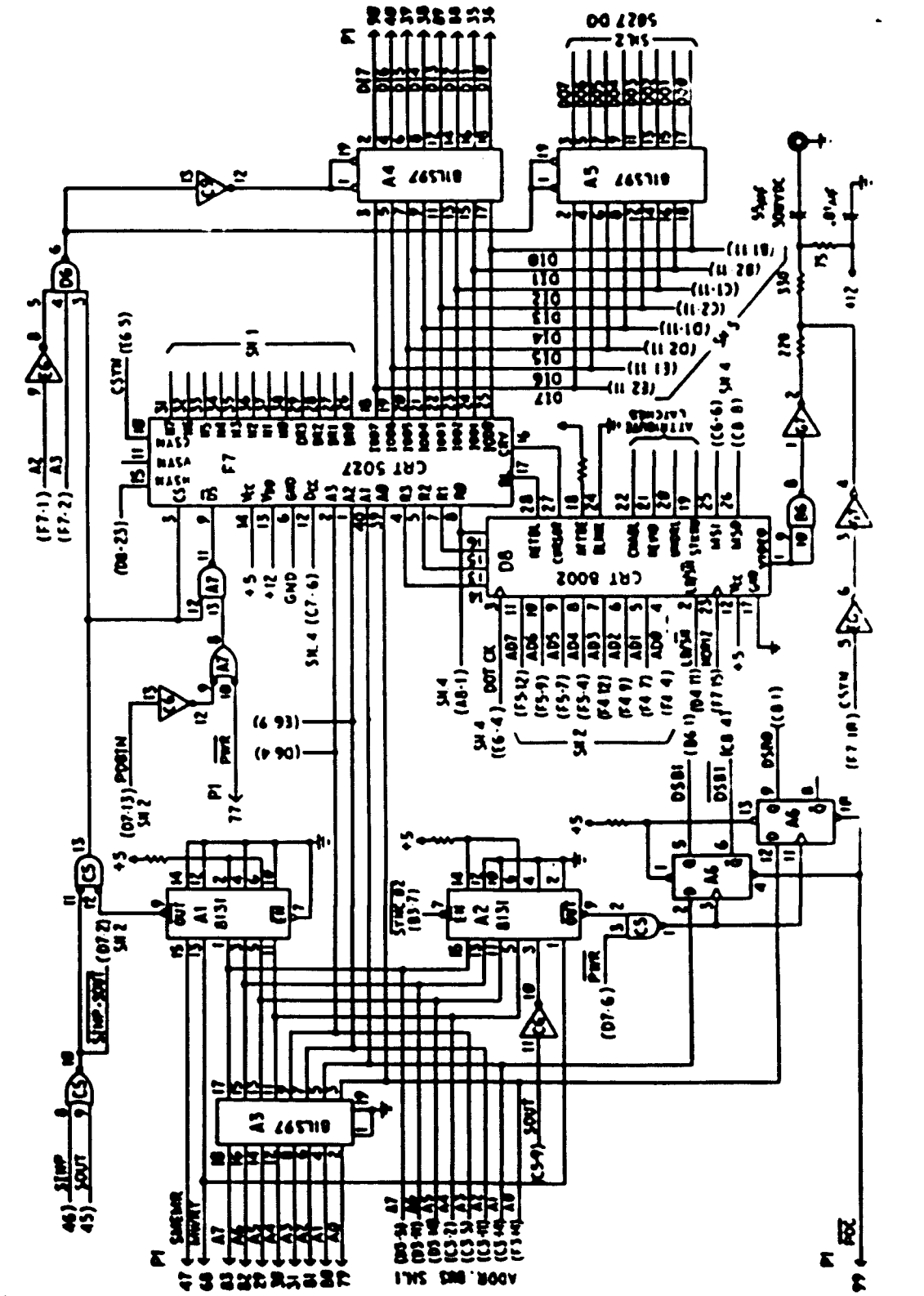
SCHEMATICS



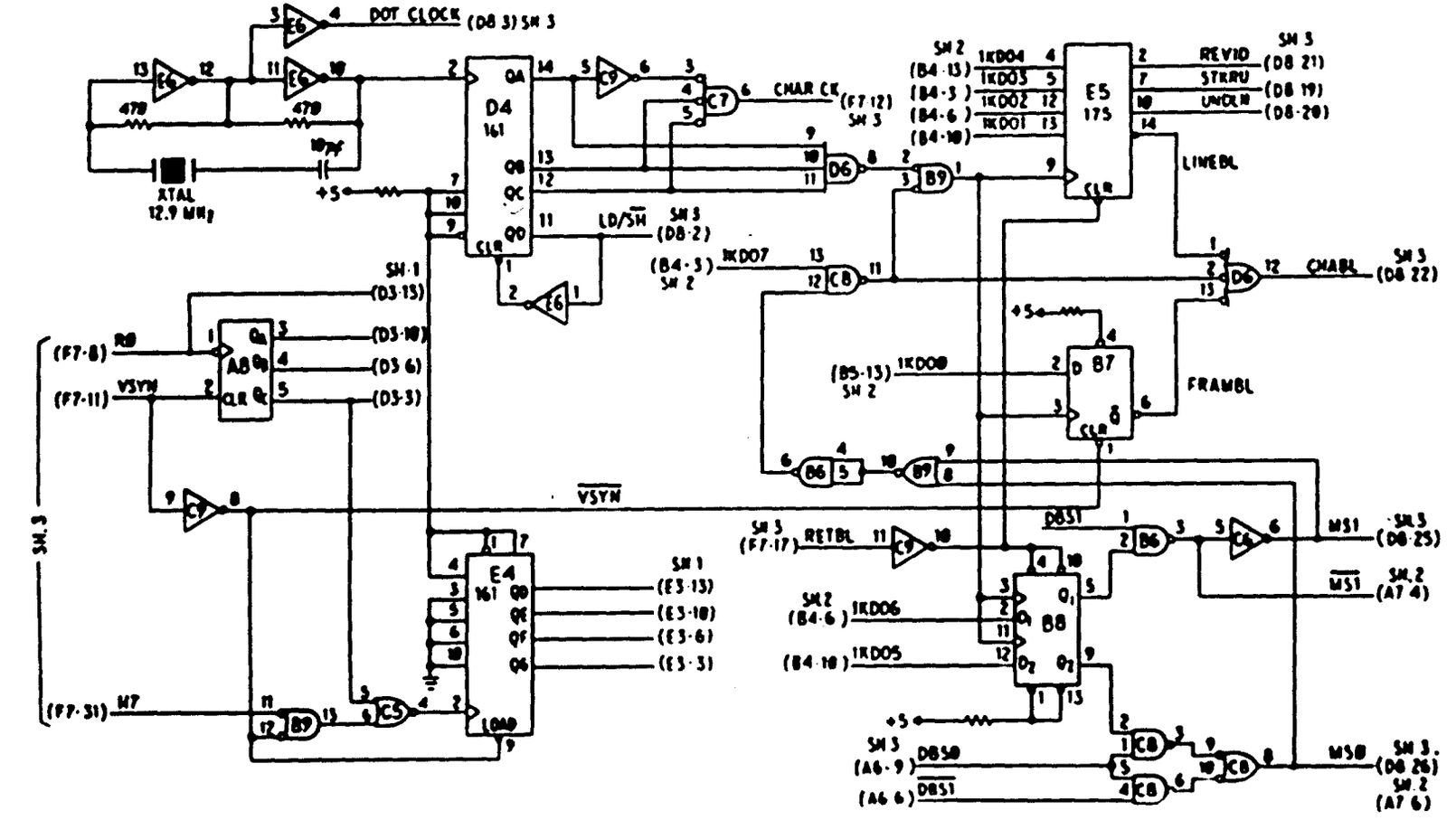
The Address Bus



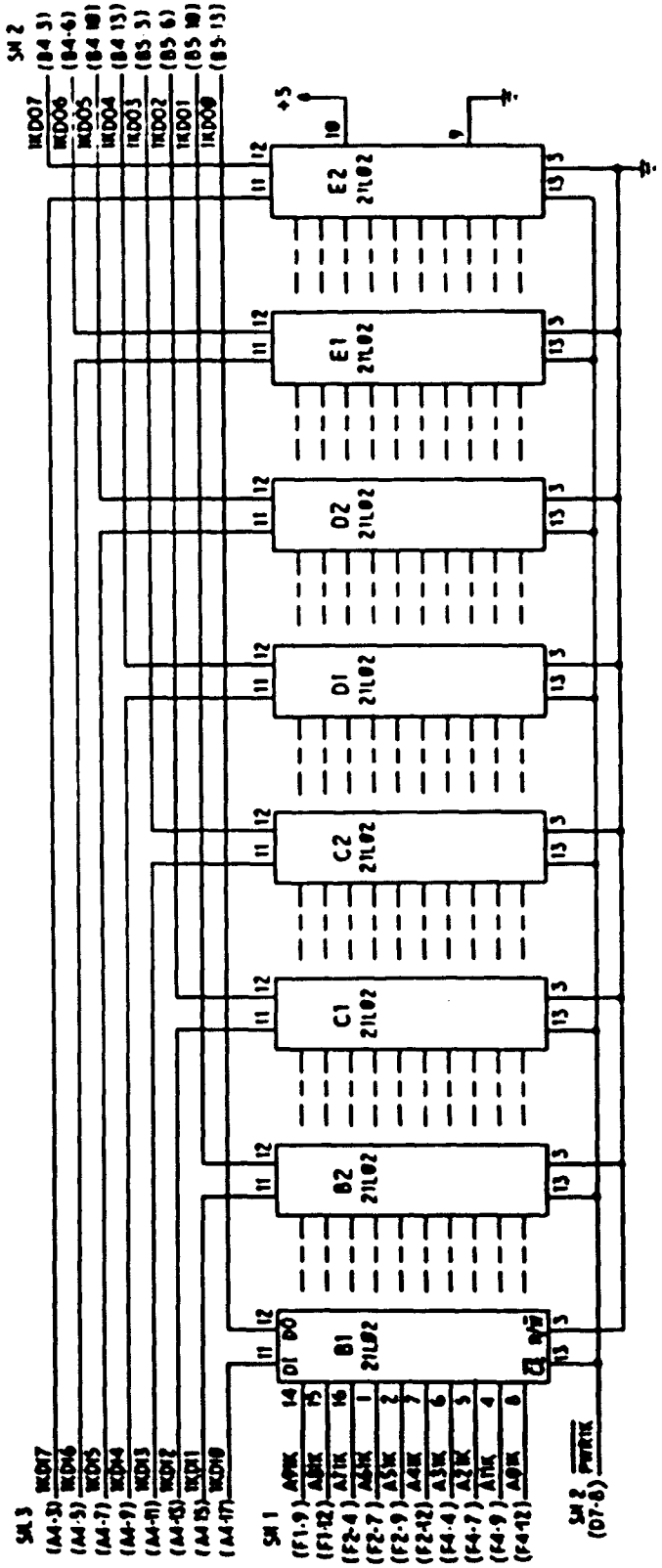
The Data Bus
-46-



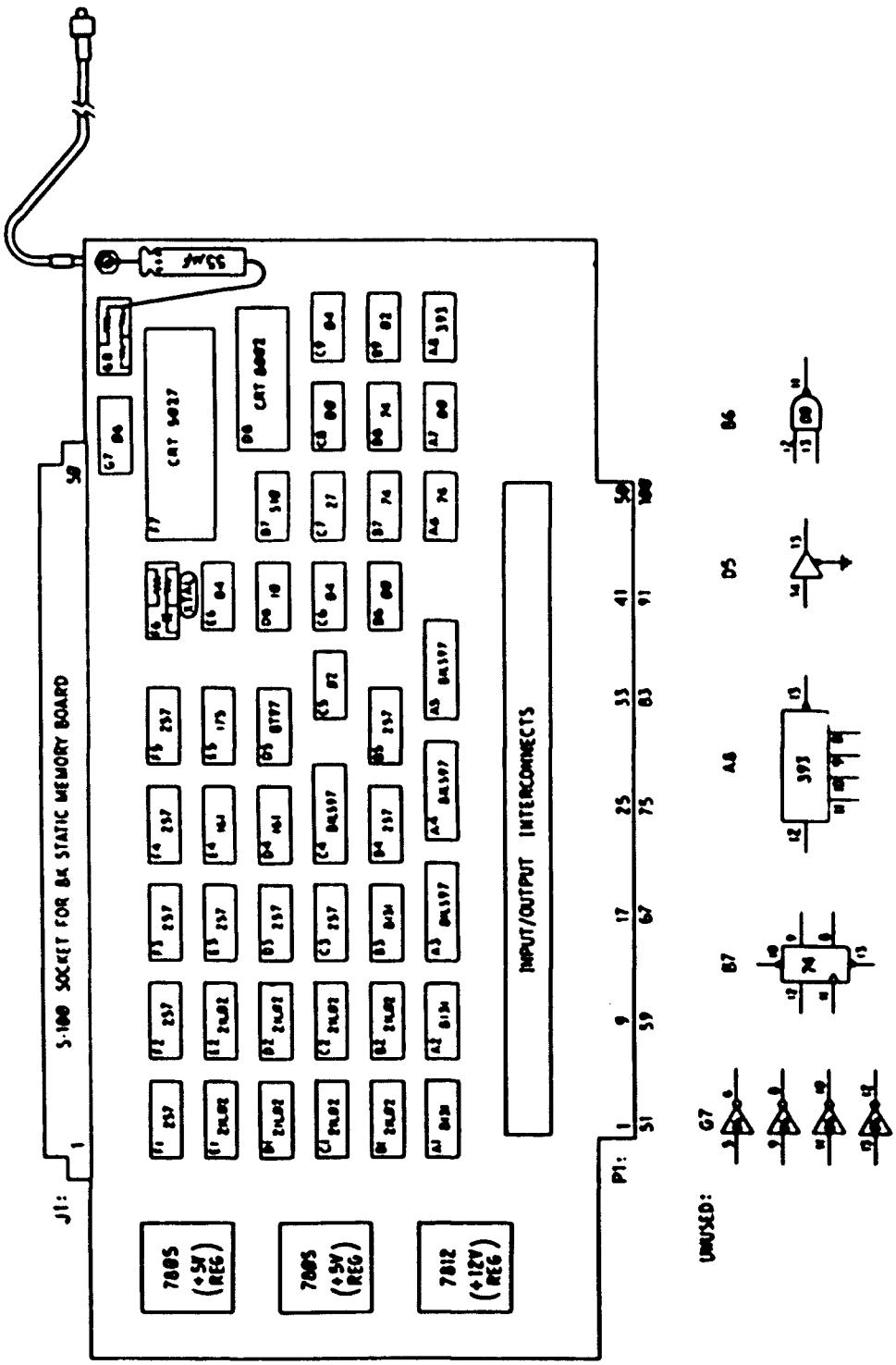
CRT Control Circuitry



Clocks and Mode Control



1K Memory Section



VDGT Circuit Board Layout

Thomas L. Carpenter, III, was born in Wilmington, Delaware, on January 31, 1943. He is the son of T. Leslie Carpenter, Jr., and Sadie (Ehart) Carpenter, both of Wilmington, Delaware. He married Carol Lee Crews, also of Wilmington, on January 9, 1965.

He attended the University of Delaware where he received a Bachelors Degree in Electrical Engineering in 1969. He then joined Western Electric Company, Inc., as a Test Engineer in the Test Planning and Design Engineering Department. He was assigned to a temporary position with Bell Telephone Laboratories in June, 1978. On January 1, 1979, he took a permanent position with Bell Laboratories as a Member of the Technical Staff in the SIC Test Group.

His hobbies include tennis, golf, and personal computing.