Spring 4-1-2007

Chalcogenide glass memory: Applications and issues

Sean Jong Lee
Intel

Memory Industry Perspective of Chalcogenide Glass Uses and Issues

New NVM Technology is Rare

1967 → First Floating Gate Structure

1971 → FAMOS

1977 → EPROM

1980 → EEPROM

1985 → 1T EEPROM (Flash)

1988 → NOR Flash

1989 → NAND Flash

1995 →MLC Flash

Floating-Gate Concept

- ~ 40yr Old
- Evolutionary Changes
  EPROM → E^2PROM → Flash

Memory Scaling is Increasingly Challenged

- Critically Dependent on Fine Line/Space Pattering
- Storage/Stability Hindering Dielectric/Voltage Scaling

"Explosion" of "New" Memory Concepts

- New Storage Materials, New Storage Concepts
- Many Ideas, Varying Functionality/Cost, All Unproven

Alternative NVM Success Criteria

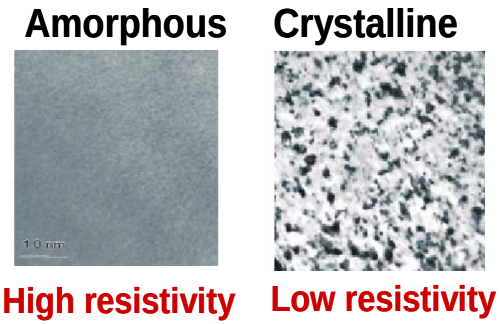
		Code	Data Performance	Data Density
Cell Size		~<4λ^2	~<4λ^2	~<2λ^2
Write	Latency	~0.1µs	~10µs	~100µs
	Throughput	~5MB/s	~100MB/s	~20MB/s
	Granularity	~16Byte	~1kB	~10kB
Read	Latency	~0.1µs	~10µs	~100µs
	Throughput	~500MB/s	~100MB/s	~50MB/s
	Dynamic	1,000x	100x	100x
Endurance	Read	~10^{15}	~10^{12}	~10^{12}
	Write	~10^{5}	~10^{6}	~10^{5}
Retention		10yr	3yr	3yr

In All Cases: Theoretical scalability of storage mechanism to <10nm is a primary requirement

Phase Change Memory Concepts

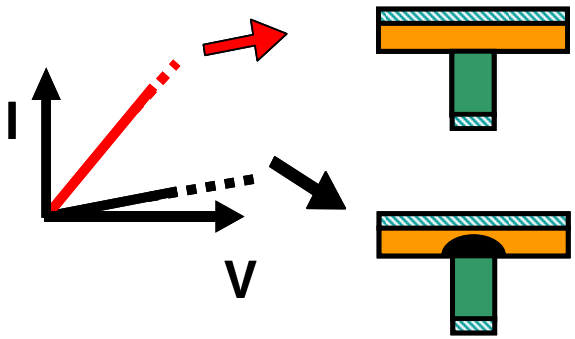
Storing Mechanism

- amorphous / poly-crystal phases of a chalcogenide alloy, usually $Ge_2Sb_2Te_5$ (GST)



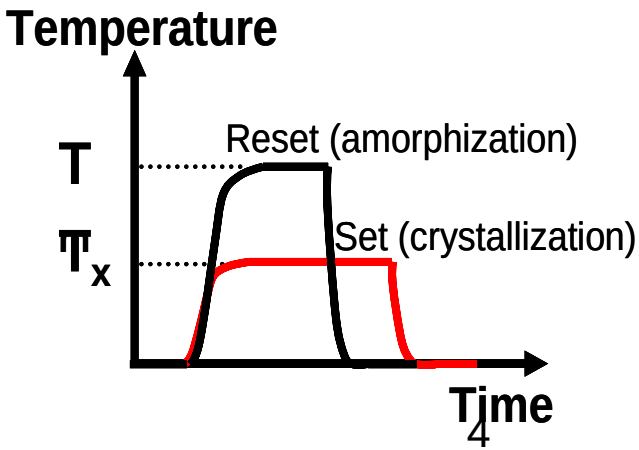
Reading Mechanism

- resistance change of the GST



Writing Mechanism

- self-heating due to current flow (Joule effect)



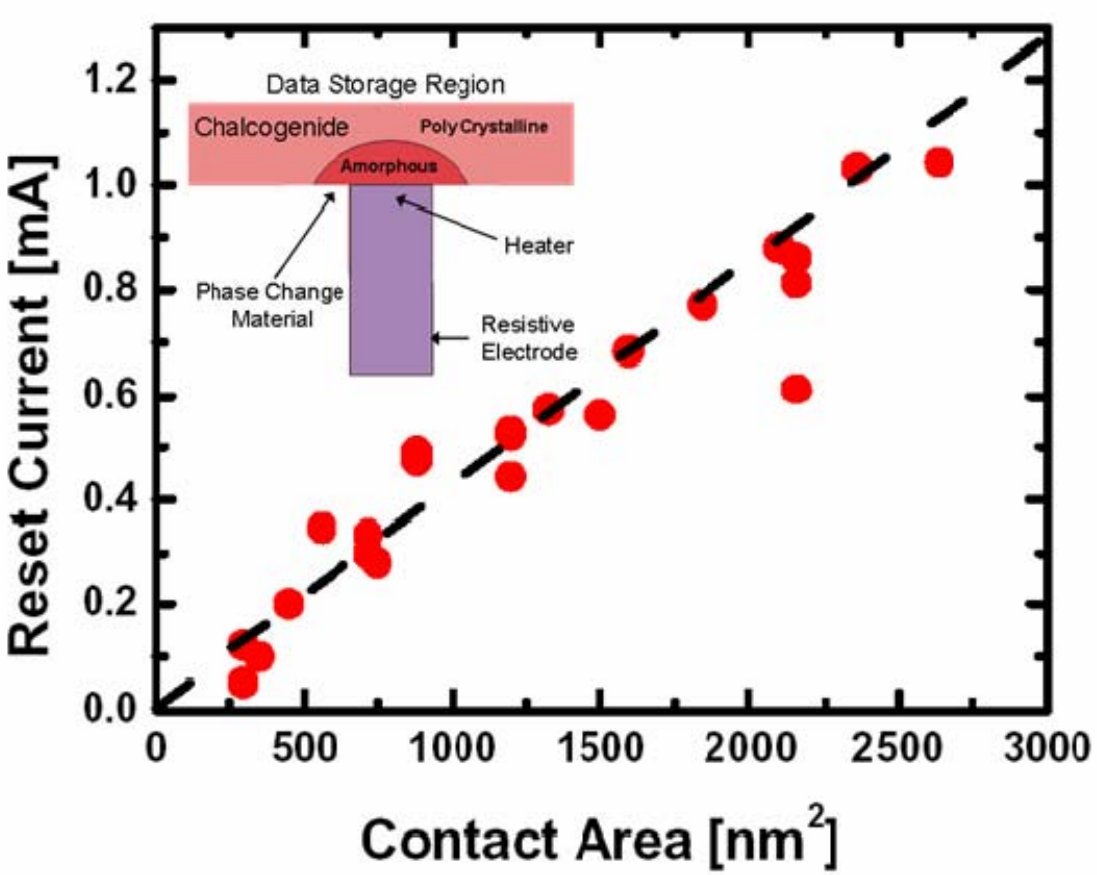
Cell Structure

- 1 transistor, 1 resistor (1T/1R)

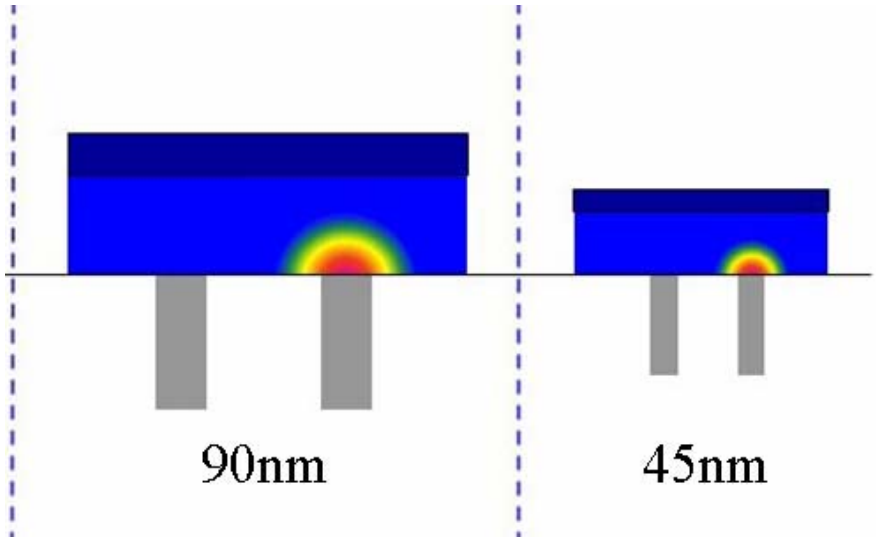
Scalability of PCM Storage

Programming Current and Thermal Disturbs Scale Well

Programming Current Scaling



Thermal "Disturb" Scaling



1. Contact area of heater / phase change scales with technology Node
2. Ireset/Iset reduces with scaling

→ Margin for thermal proximity disturb is constant through scaling

The Promise of PCM

Matches Today's Flash

- Cell size / Die size / Cost ~ Flash NOR
- Fast random read performance ~ 50 ns
- Unlimited read endurance
- Good data retention ~ 10 years
- Fast write performance ~ 100 ns
- CMOS compatible

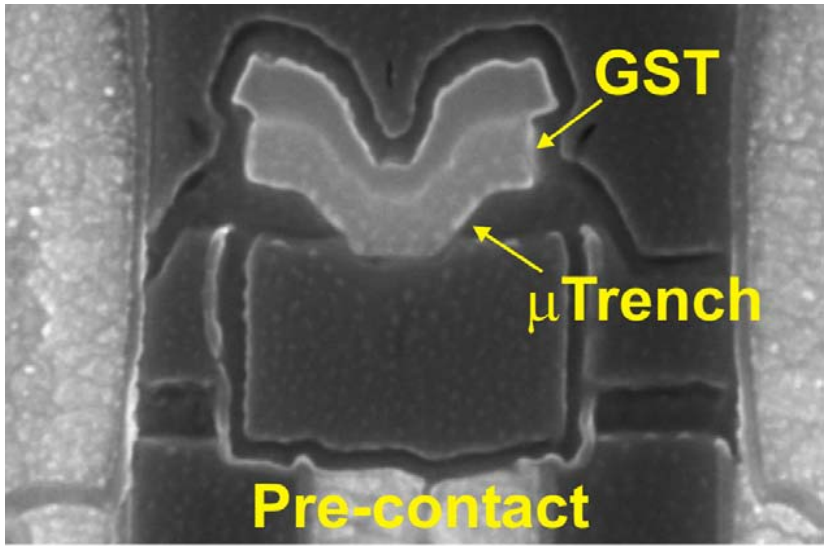
Exceeds Today's Flash

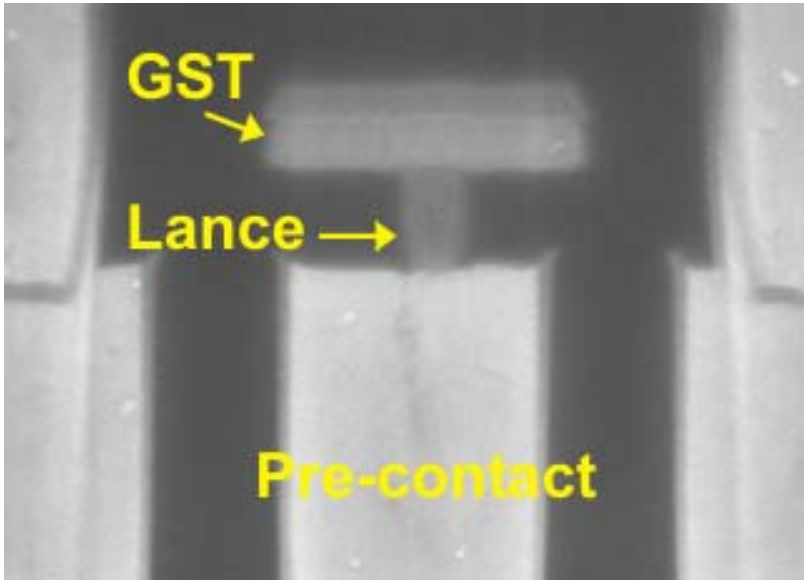
- Bit granularity
- Long endurance

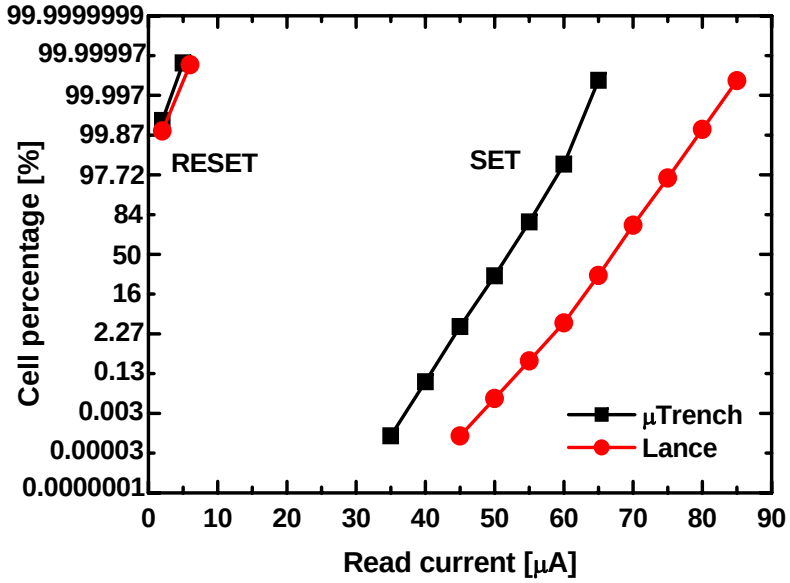
Long Term Roadmap

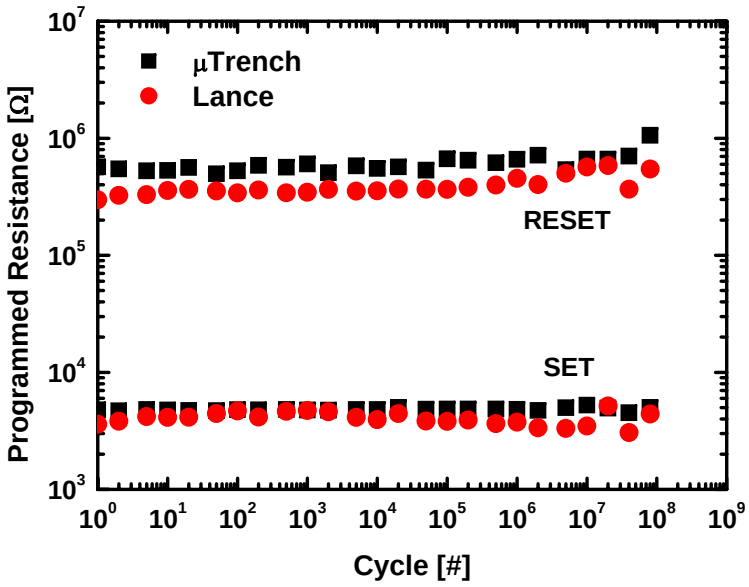
- Good scalability
- Multi-Level feasible

Multi-megabit Array From Intel-ST

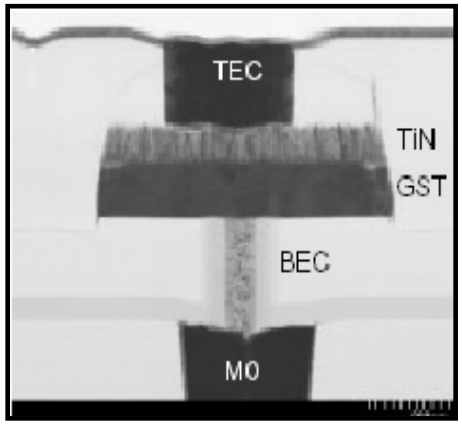




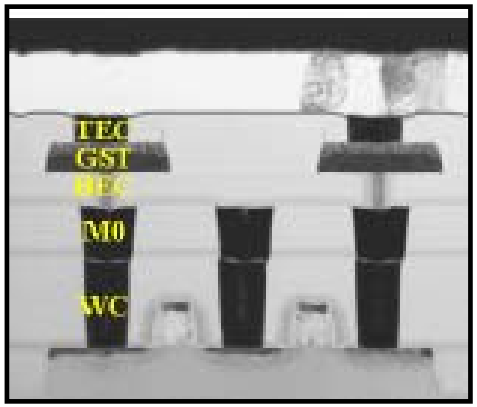


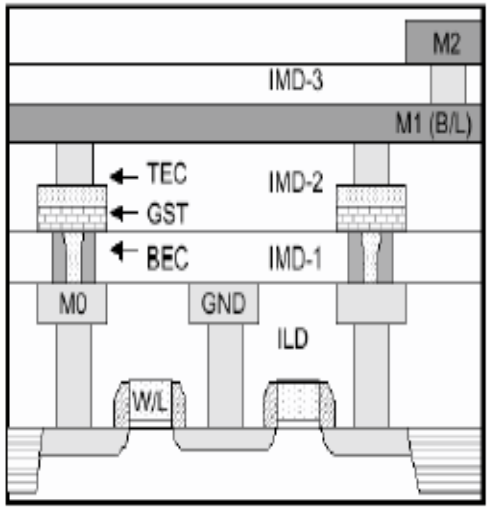


PCM Array from Samsung



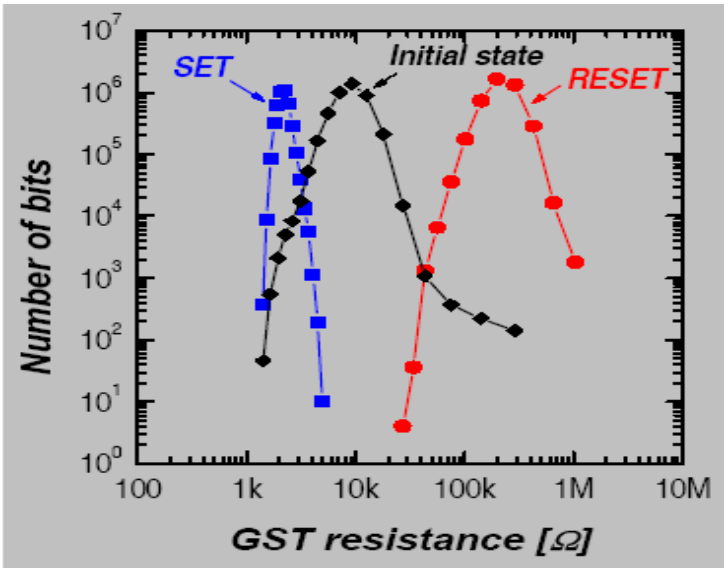
Memory Element



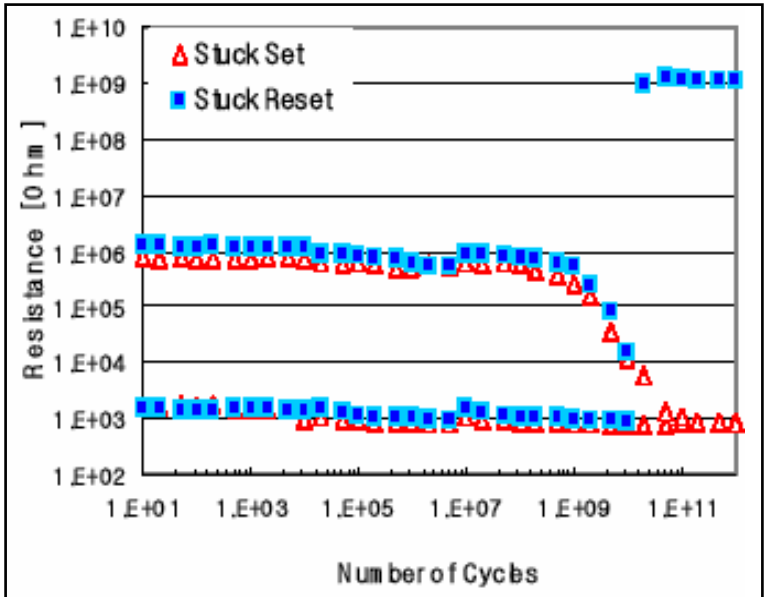


Cell Cross-Section with MOS Selector

GST to Heater Contact Area is Defined by a Spacer Reduced Contact



Array Distributions

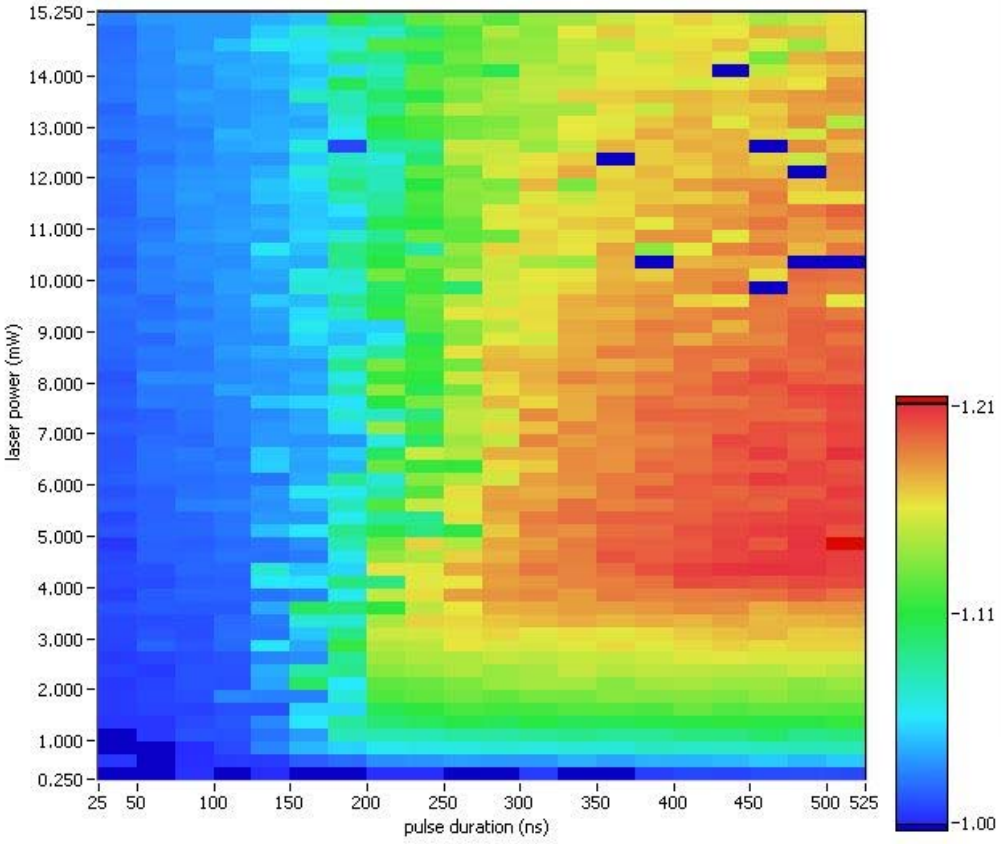


Cycling Endurance

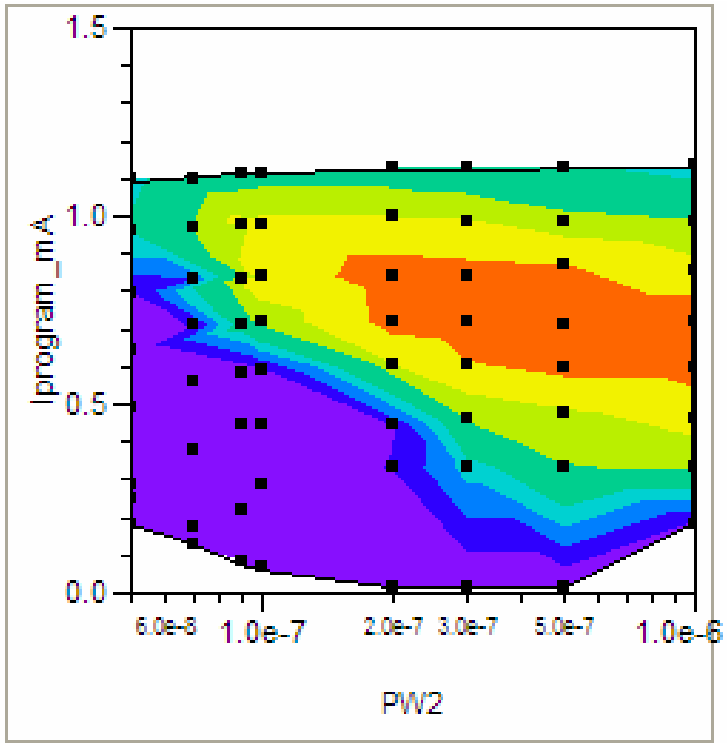
Good Cycle Life and Array Distribution Data Observed

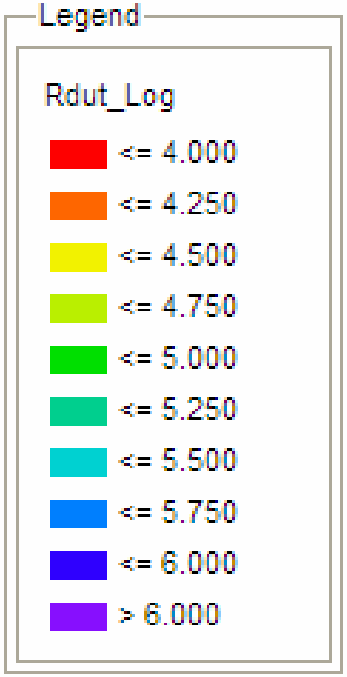
Characterization of Phase Change Kinetics of a Memory Device by Electrical Pumping

Optical 'media map'

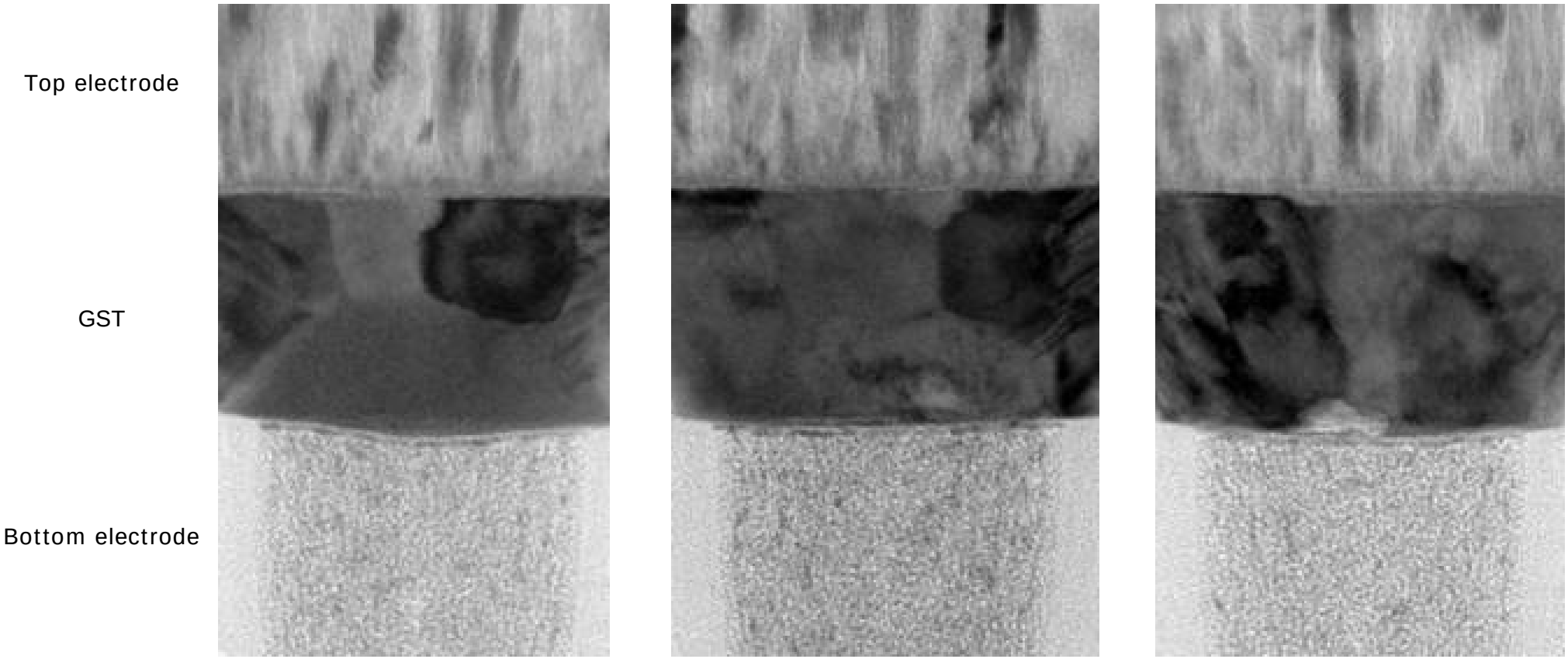


Electrical 'media map'





Characterization of Phase Change Kinetics of an Memory Device by Elecrical Pumping

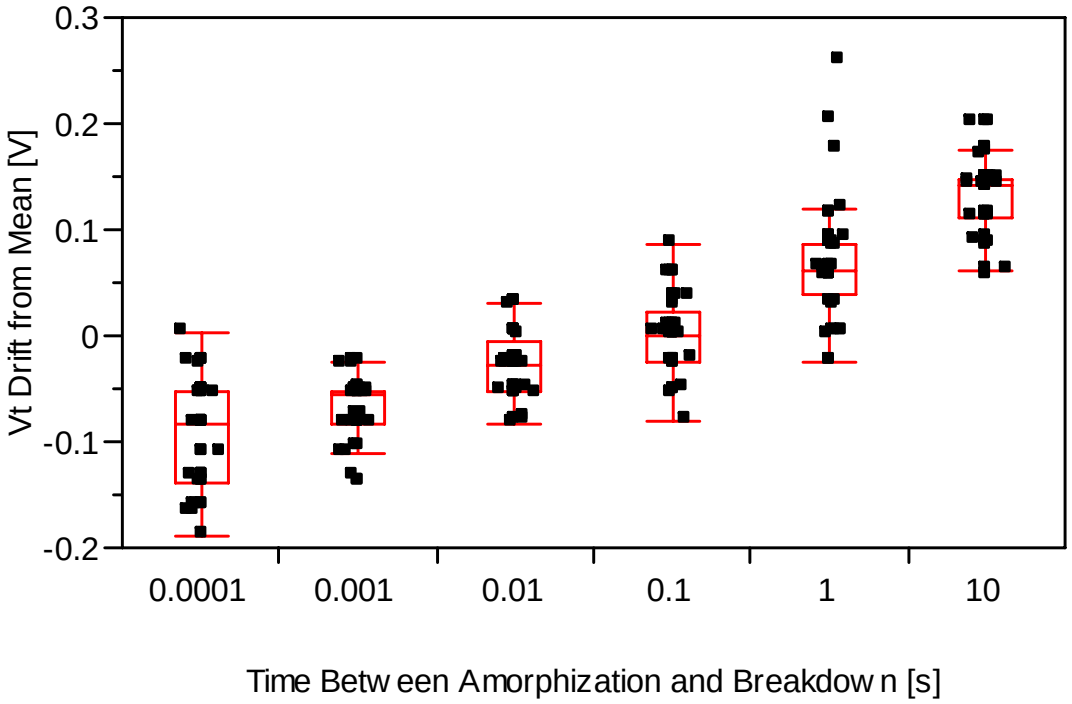


Fully amorphized

Partially crystallized

Fully crystallized

Drift of Chalcogenide Glass Dielectric Breakdown (Threshold) Voltage



PCM Technical Challenges

- Intrinsic chalcogenide stability
  - Glassy phase electrical conductivity change with time.
  - Ge2Sb2Te5 is not a thermodynamically stable alloy and segregation occurs with repeated program-erase cycles.
- Extrinsic chalcogenide stability
  - Impurities introduced during chalcogenide processing.
  - Chalcogenide-metal junction (contact) compatibility.
- Material performance
  - Programming current (current density) to melt chalcogenide
  - Slow crystallization speed (trade-off with data retention)